A comparative study of power converters for coupling a renewable source to an electrolyser

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PREFACE

This dissertation studies the common causes of switching device failure in power converters. The gained knowledge was then applied from a practical point of view to two different power converter topologies in order to study the waveform characteristics of each converter with the purpose of finding a suitable power converter for coupling a renewable energy source to an electrolyser. The most efficient converter was then coupled to a photovoltaic array and electrolyser stack and the microprocessor were then programmed to manage the system automatically. The gained knowledge will be used to upscale the converter to a higher capacity.

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ABSTRACT

Renewable energy sources are receiving much attention due to their clean and sustainable properties. The problem with these renewable energy sources is that they do not provide stable and constant power. Instead, they are only able to provide intermittent power when certain conditions are met. Therefore, to maximise the energy utilization from these renewable energy sources, the energy must be stored in such a way that no harmful by-products or gasses are formed [12]. Hydrogen gas, produced from water using electrolysis, can be used to store solar and wind energy. Photovoltaic panels are conventionally used to power an electrolyser using a power converter. This configuration is both simple to implement and very environmentally friendly. Transitioning to hydrogen as an energy source will also ensure a more secure source of energy as there is less risk of depletion and price volatility that can result in economic pressures. An LLC resonant converter is a kind of DC/DC power converter that is able to achieve zero voltage switching across a wide load range by utilizing the transformer leakage and magnetizing inductances in series with a capacitor, hence the term LLC. Therefore, these power converters are associated with very high efficiencies up to 97%. Presented here is the design, simulation, test and evaluation of an LLC resonant converter for coupling a photovoltaic array to a polymer electrolyte membrane water electrolyser (PEMWE). The resonant converter will be compared to a hard switched converter. A microprocessor is used to control the power converter to ensure that the solar panels are operating at their maximum power point which will result in optimal hydrogen production and maximum overall system efficiency.

SUMMARY

In this study, different power converter topologies and the common causes of switching device failure in them were studied and summarised in the literature. Two commonly used switching techniques were applied to one topology (full-bridge converter) namely hard-switching and resonant switching. The two converters were then simulated and practically implemented to measure the characteristic waveforms and verify them against the literature to find the most energy efficient and reliable converter. Reliability is determined by factors such as the efficiency which is associated with high heat dissipation and the degradation of electronic components as well as the characteristic waveforms that can put unnecessary stresses on the switching electronics. It can be seen in both the simulated waveforms as well as the measured waveforms that the resonant converter is able to achieve soft switching across a wide input voltage range while having a higher efficiency. The hard-switched converter generated more heat during measurements and had all the characteristics of a power converter associated with low efficiency. All waveforms are measured and the significance of each characteristic within the waveforms are documented and explained to show the significance of the switching technique used. Two different Maximum Power Point Tracking (MPPT) algorithms were implemented on the resonant converter and the comparison shows that the Variable-Step Incremental Conductance (VSINC) is able to track the maximum power point significantly quicker than the Perturb and Observe (P&O) method. The resonant converter has a high efficiency and it was shown that this type of switching technique is able to address all the common causes of switching device failure as seen in the hard-switched converter. Therefore, it is the preferred converter type for coupling a renewable energy source to an electrolyser for producing hydrogen gas.

Keywords: Maximum Power Point Tracking (MPPT), Zero Voltage Switching (ZVS), hard-switching, LLC resonant converter, renewable energy source, hydrogen, electrolyser

LIST OF ABBREVIATIONS

Abbreviation	Meaning
AC	Alternating Current
ADC	Analog-to-Digital Converter
BJT	Bipolar Junction Transistor
CCM	Continuous Conduction Mode
CPU	Central Processing Unit
DC	Direct Current
DCM	Discontinuous Conduction Mode
EMF	Electromotive Force
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FHA	First Harmonic Approximation
HF	High Frequency
Hz	Hertz
IGBT	Insulated-Gate Bipolar Transistor
LHV	Lower Heating Value
LLC	Inductor-Inductor-Capacitor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOV	Metal Oxide Varistor
MPPT	Maximum Power Point Tracking
nL	Normal Litres
nLPM	Normal Litres Per Minute
PCB	Printed Circuit Board
PEM	Polymer Electrolyte Membrane / Proton Exchange Membrane
PFM	Pulse Frequency Modulation
PSFB	Phase-Shifted Full Bridge
PV	Photovoltaic
PWM	Pulse Width Modulation
RC	Resistor-Capacitor
RCD	Resistor-Capacitor-Diode
RFI	Radio-Frequency Interference
RMS	Root Mean Square
SMPS	Switched Mode Power Supply
SNR	Signal-to-Noise Ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
TVS	Transient Voltage Suppressor
USB	Universal Serial Bus
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

LIST OF SYMBOLS

Symbol	Description
Ac	Cross Sectional Area
B	Flux Density (Tesla)
C	Capacitance (Farads)
D	Duty cycle (%)
d	Diameter
dI/dt	Current Ramp
dV/dt	Voltage Ramp
E	Energy (kWh)
f	Frequency (Hz)
F	Faraday Constant (s.A/mol)
g	Air-gap (in mm)
I	Current (A)
ṁ	Mol (unless stated otherwise)
M	Molar Mass (in grams, unless stated otherwise)
k	Termal Conductivity (°C/W)
L	Inductance (unless stated otherwise)
lc	Magnetic path-length (mm)
P	Power (W)
Q	Quality Factor / Charge (unless stated otherwise)
R	Resistance (ohm)
s	Distance (unless stated otherwise)
t	Time (s)
T	Temperature in °C (unless stated otherwise)
μ	Permeability
V	Voltage (V)
W	Watt (unless stated otherwise)
Wa	Windowing Area
δ	Skin Depth (in mm)
ρ	Resistivity (in Ω.m)
Ω	ohms

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CHAPTER 1: INTRODUCTION

1.1 Background

One of the most conventional methods for producing hydrogen gas from water is the use of a power converter that uses electricity obtained from crystalline photovoltaic panels. This is because this method exhibits a very high purity and is quite simple [12, 13]. It will also make a contribution in the reduction of air pollution and greenhouse gas emissions, especially when used as a fuel source, for providing electrical energy, in the transportation industry as it will reduce the global dependency on fossil fuels. Transitioning to hydrogen as an energy source will also ensure a more secure source of energy as there is less risk of depletion and price volatility that can result in economic pressures [14].

The effective and efficient storage of energy obtained from renewable energy sources is one of the biggest reasons why there is no mass-scale usage of renewable energy sources. The conversion of excess electrical power to hydrogen by means of electrolysis, the storage of the hydrogen and the conversion process involved in converting back the hydrogen to electricity are the main components involved in hydrogen-based electricity storage systems [15]. Each subsystem involved in the conversion process has an efficiency of its own, leading to an overall decrease in system efficiency. One such system involved in the conversion process is a DC/DC converter.

A DC/DC converter can be defined as an electronic device that can convert power by means of impedance conversion over a wide dynamic range. There are several topologies that can be used, depending on the characteristics of the source and the requirements of the load. In the case of a solar panel, it is required to control the DC/DC converter in a specific way so it can be able to utilize the photovoltaic panel at its optimum level to extract the maximum amount of power. Also, the DC/DC converter uses electronic components like MOSFETs for high speed switching. These three pin devices have some form of parasitic capacitance inside them that affects the speed at which the device can be switched on and off.

To get around this problem, a switching technique known as Zero Voltage Switching (ZVS) must be employed and taken into consideration during the design process. External capacitances may be added to enable the device to achieve ZVS during certain load conditions as the device may lose its ZVS capability when the load is greatly reduced.

An alternative method is to use a resonant converter, but there is a limited amount of research available that fully documents how the ZVS region shifts and how to deal with it, especially when the source is a photovoltaic panel and the load is an electrolyser. There is insufficient information available that documents how the ZVS capability of the power supply is affected when either the solar panels or the electrolyser is changed, or when the power supply or load demand requirements change as it is known that a power supply can lose its ZVS capability when the load is greatly reduced. In the case where a Polymer Electrolyte Membrane (PEM) electrolyser is used as the load and a photovoltaic array is used as the source, it is required that the power supply be efficient at a wide variety of loads and supply capacity.

1.2 Problem statement

The PEM electrolyser has the capability to operate at very high current densities. This reduces the operational costs as this kind of electrolyser allows a more dynamic coupling with systems that can provide intermittent power like renewable energy sources. Although PEM technology improves the dynamic range, it still isn't perfect as its dynamic range still has limits. The DC/DC converter is a dynamic power conversion device, but its efficiency changes as the load requirements change. This is highly dependent on the behaviour of the power source as well as the load. To counter this problem, current systems will charge a battery array and then supply power from the batteries to an electrolyser. This increases system cost and reduces the total efficiency of the system because multiple power converters are required.

This will require the implementation and evaluation of an application specific power conversion device that is optimized for the coupling of solar panels to an electrolyser. The system should then attempt to change the static behaviour of the direct coupling process to an optimized and more dynamic conversion process. To be able to do power conversion, a static system must be implemented that can convert power over a wide dynamic range. This kind of system is also referred to as a DC-DC converter because it dynamically converts one impedance to another [16]. This will involve the use of a microprocessor controlled DC-DC converter as the microprocessor can make real-time adjustments to keep the solar panels from operating below its MPP point. Figure 1-1 shows a system that uses a DC-DC converter with an MPPT algorithm to deliver direct power to a PEM electrolyser. The purpose of the research will be to determine and document the behaviour of two different DC/DC converter topologies specifically designed for solar to hydrogen conversion.

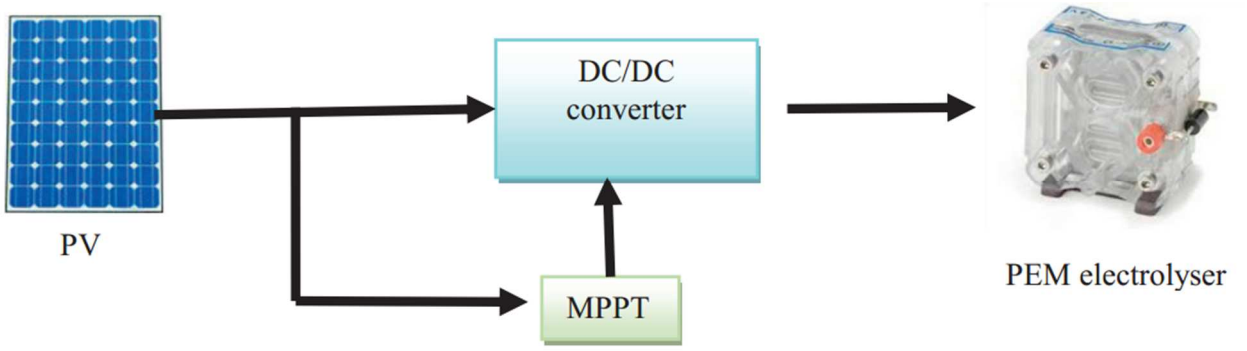


Figure 1-1: PV panel connected to a PEM electrolyser through a DC/DC converter

1.2.1 Purpose of Research

Connecting a DC/DC converter between a photovoltaic panel and an electrolyser is not a new strategy for optimizing the system efficiency, but a limited amount of research is available on the specifics of an application specific DC/DC converter that is used for this process. This includes the full documentation on how ZVS behaves across the MOSFET drain-source for the entire load range as the photovoltaic panel's maximum power point and capacity changes due to temperature changes and a shift in solar irradiance levels. There is also insufficient research to show how the drain-source waveforms will change as the photovoltaic (source) or electrolyser (load) configuration changes in terms of voltage and current. It is known that voltage ripple has a positive effect on the PEM electrolyser in terms of the hydrogen production rate. This will also be documented throughout the test and evaluation phase and compared to the converter efficiency.

The purpose of this research is to determine the efficiency increase or decrease of the implementation of an application specific DC/DC converter for use in solar to hydrogen production and to fully document its results over the entire load range. Most DC/DC converters are designed to do ZVS at a specific load range. Therefore, it is usually optimized to achieve ZVS at a certain payload. In the case where the source capacity changes drastically, the converter may lose its ZVS capability, leading to high amounts of losses. This study will therefore focus on the following list of items, while keeping the end goal and use of the device in mind:

- Design, simulate, test and validate the MOSFET waveforms of two different power converters and compare their performance in terms of efficiency and reliability;
- Test the power converters at different input voltages in the lab on a programmable load;
- Documenting the MOSFET waveforms over the entire load range;
- Implement two different kinds of MPPT on the best power converter and test it on a PV array;
- Connect the best power converter to an electrolyser and test it with the MPPT algorithms;
- Test and document the efficiency, hydrogen production and MPPT for the ZVS converter and

- Make recommendations to further improve the power converter for coupling a renewable energy source to an electrolyser.

1.2.2 Motivation for Research

The purpose of this research is not to just design another DC/DC converter, nor is it to evaluate or improve current DC/DC converter topologies. The purpose of this research, to start with, is to design at least two very different DC/DC converters to couple an electrolyser to a photovoltaic array and to use the converters to evaluate the converter efficiency with regards to MOSFET or other switching losses as well as the MPPT algorithm. There exists a limited amount of research on the use of phase shifted full bridge and resonant converter topologies for doing electrolysis from a photovoltaic panel. Most research is based on the push-pull or half-bridge design. Although this might seem obvious, it is not for the following reasons and this is what this research study aims to address. The PEM electrolyser's hydrogen production rate is directly affected not only by the converter efficiency, but also by the amount of ripple voltage present at the output of the converter. In most cases, DC/DC converters are designed in such a way as to reduce the ripple voltage at the output to within a certain limit, even if it requires sacrificing a small amount of converter efficiency. This is true for almost all DC/DC converters that can be purchased as a standard or “ready to go” unit. The ripple voltage has a positive effect on electrolysis in the sense that a higher ripple voltage at the output will produce a significantly higher amount of hydrogen. Too much ripple voltage (in the range of 1 ~ 2V) will however cause rapid electrolyser degradation, but it will accelerate the hydrogen production rate. Therefore, the research will focus on the design and evaluation of two application specific designs in order to document the following results:

1. Generate data for maximum power available at the photovoltaic panels throughout the day;
2. Log the converter efficiency ($\frac{Pout}{Pin}$);
3. Graph the amount of hydrogen produced in the conditions of (1) and (2) above and compare that against the known faradic efficiency for an electrolyser.

Because this converter will not do output regulation, it might be possible to exclude the need for PI control. It should also be noted that points (1), (2) and (3) is only the basis of the research and that other design factors such as the evaluation and effect of different MPPT algorithms will also be fully documented. Other good converter design practices will also be considered and fully documented throughout the research such as the methods used to achieve ZVS (where applicable). The choice of transformer and resonant tank circuit components will also be fully documented throughout the study.

The electrolyser acts like a battery in the sense that when it is first powered on, it will attempt to "charge". This can lead to a current surge that lasts a few seconds, which might harm the electrolyser. In the resonant and phase shifted full bridge converter, it will be easy to achieve a perfect "soft" and "slow" start to protect the power converter. Furthermore, because the voltage regulation requirements for the electrolyser differs greatly from that of a digital circuit which has certain maximum allowed ripple voltages, this will also ease the DC/DC converter design and will greatly reduce the converter design difficulty. This is especially true when the design is aimed for maximum efficiency without taking ripple voltage into account.

The study will also reveal the cost of such a system and will also make a contribution in understanding which converter topology will allow the highest efficiency while allowing a ripple voltage that enables a maximized hydrogen production rate. From this data, the possibility to upscale solar to hydrogen production systems will also become clear, although that is not the purpose of this study. The proposed research is not to predict if more hydrogen will be produced with an increased circuit efficiency, however this is documented in the final chapter.

1.3 Research Aims and Objectives

To be able to determine which converter topology will be the most suitable for directly converting solar energy to hydrogen and to determine which converter allows the electrolyser to produce more hydrogen, some objectives must be reached in order to achieve the final goal. The following objectives are evident from the purpose and motivation for the research:

- Literature survey on the different DC/DC converter topologies, their advantages, disadvantages and working principles;
- The integration of different MPPT algorithms in two different converters;
- Circuit design for two converters in using LTspice® and NI Multisim®;
- Writing equations in Matlab® to calculate circuit component values;
- Simulating the circuit behaviour in SPICE software as well as Simulink® in order to verify circuit behaviour;
- Implementing a prototype of the circuit and test it using a photovoltaic array and a PEM electrolyser;
- Conduct tests to verify the obtained data against the simulation software results and
- Validate the end result by measuring the amount of hydrogen produced for each converter.

The objectives must be met in order to achieve the goals as listed in the research methodology.

1.4 Research Methodology to Achieve Goals

1.4.1 Current technologies and literature study

A detailed literature study needs to be done to ensure that the problem is fully understood and that every possible solution to the problem with both their individual advantages and disadvantages are considered. This will focus on the different DC converter topologies as well as the different MPPT algorithms that can be applied to these topologies.

1.4.2 Conceptual and detailed design

After the literature study is completed, a conceptual design is implemented and evaluated to determine its suitability in addressing the problem. This will be part of the theoretical design which is developed from the knowledge obtained in the literature study. This involves the derivation of mathematical models to calculate the electronic component values. Then, the detailed design is implemented by using the conceptual design and applying the knowledge obtained from the literature study. Electronic circuit design is done by selecting an appropriate converter topology that worked best with the digital controller. LTspice® and NI Multisim® will be used to draw the circuit diagrams.

1.4.3 Control system design

The firmware employed on the embedded system for use in the DC-DC converter was implemented in different stages. Primary switching control was implemented first, followed by the MPPT algorithm which can be tested on a programmable power supply emulating the I-V curve of a solar panel array. A combination of analogue and digital circuits can be used. Matlab® was used to assist in simulating part of the circuit behaviour by means of mathematical modelling.

1.4.4 Construct a prototype

A basic prototype was built on a PCB to test the firmware implemented on the microcontroller. The same circuit is then modified to test and evaluate a different converter topologies in order to document and compare the results to the theoretical design.

1.4.5 Simulation and testing

To test the feasibility of the detail design, the electronic circuits are built in different stages and simulated to test their conceptual functioning principles. Circuit simulation is done in both LTspice® and NI Multisim®. Mathematical modelling of the circuit's Laplace transforms was done using Matlab® in order to determine the optimal component selection. Then the circuit is built on a Printed Circuit Board (PCB) in different stages and subjected to various different load conditions

to ensure minimal losses. Continuous firmware changes will be made to improve the system efficiency.

1.4.6 Evaluation

This is the stage where power output is compared to power input in order to verify the circuit efficiency. Results are compared to the amount of hydrogen that is produced as it is known that voltage ripple has an effect on the hydrogen production rate. A LeCroy® scope is used to measure the drain-source waveforms at each MOSFET to fully document the ZVS behaviour as the load and source changes their characteristics.

1.5 Contributions to be made by the study

The study focuses on developing an application specific DC/DC converter to be used exclusively for solar to electrolyser coupling with the end goal of producing hydrogen from the electrolysis of water. This will help to maintain efficient hydrogen production as the PEM electrolyser degrades and as the maximum power point changes on the photovoltaic panels. It will also help to maintain a high efficiency if the photovoltaic panels are substituted with differently branded panels or if the electrolyser is changed with another one.

A detailed comparison between two different converter topologies (used for solar to hydrogen generation) with regards to ZVS and other switching losses are made to be able to better understand the circuit behaviour as conditions change drastically. Usually DC/DC converters are designed in such a way that they have a very low ripple voltage at the output, but in this study, the converter will be optimized for high reliability and efficiency. This allows some changes to be made to the converter as MPPT algorithm can sometimes cause a voltage ripple as the algorithm continually adjust the circuit switching to keep the device operating at the solar array's MPP.

This will help to understand the possibility of upscaling the technology as it will document the behaviour of different MPPT algorithms, the ZVS range, the difficulty level in designing each converter type, the effect on cost and efficiency. The end goal is to determine which converter will be the most suitable for a maximized hydrogen production as it is known that ripple can increase the hydrogen production rate. South Africa is a country with plenty of sunlight and has more than 75 % of the world's platinum resources. It is therefore the ideal place to conduct such a study.

1.6 Validation and verification

Equations are derived and entered into a Matlab® script to assist in the calculation of component values. These values are then used in the circuit drawn in LTspice® and NI Multisim®. This serves as a platform to simulate and test the theoretical assumptions after which the circuit is built. The

actual circuit will undergo thorough testing using a LeCroy® scope to measure the actual real world MOSFET drain-source waveforms to verify them against what the mathematical models and simulated models show. Once it has been determined that the three models namely mathematical, simulated and prototyped models match, then the theoretical and simulated models are considered to be validated as the drain-source waveforms for a ZVS converter is very well known. A thermal camera is used to verify the surface temperatures of the individual components.

1.7 Overview of dissertation

Chapter 1 is the proposal to do research on the use of two different power converters for solar to hydrogen production using a PEM electrolyser.

Chapter 2 provides a detailed literature review on the different converter topologies and how they work. Terminology and working principles are discussed in detail throughout this chapter so the reader can understand the reason behind the design chapter. It will also help to assist in understanding the importance of zero voltage switching and how it affects the reliability of a circuit.

Chapter 3 is the design chapter of the chosen two converter topologies and explains the mathematical models used to calculate the required component values. It will combine the knowledge obtained in Chapter 2 with the requirements of the research project in order to develop the two power converters, which are the platforms of the research.

Chapter 4 is the chapter in which the circuits are simulated in software to verify the behaviour of the two power converters. This is the verification chapter and the resulting simulations should match that of the literature study.

Chapter 5 will validate the simulated results of Chapter 4 by measuring the waveforms on the actual circuit. Both power converters are built and tested up to a power level of 1 kW and the resulting waveforms are documented and discussed.

In Chapter 6, the best power converter is used to couple a PV array to an electrolyser and document the MPPT results. The amount of hydrogen produced is also documented in this chapter.

Chapter 7 provides a summary and conclusion of the dissertation such as which MPPT algorithm was the most suitable and what its impact was on the output power and current of the power converter.

1.8 Conclusion & Chapter 1 Summary

This study focuses on coupling a renewable energy source to an electrolyser, therefore a suitable power converter needs to be implemented. It is preferred to use a converter that has a soft-switching capability for maximum efficiency and reliability. Therefore, two different topologies are designed, simulated, built and tested. The corresponding waveforms for each converter is measured and validated against the simulated results. The converter with the highest efficiency will be tested on a PV array and electrolyser and the results will be documented. An electrolyser test-station will be used to verify the amount of hydrogen the system is producing.

CHAPTER 2: LITERATURE STUDY

2.1 Literature Study

2.1.1 Power converter topologies

A Switched Mode Power Supply (SMPS) is a type of DC-DC power converter that can dynamically transform one impedance to another [6]. These converters make use small ferrite core transformers to increase or decrease voltage that is switched at high frequencies (usually 50-100 kHz). Shown in Figure 2-1 is a typical DC/DC converter topology. The first stage that converts the DC to AC (since transformers can only work with alternating current) is usually referred to as the primary side or high-voltage side in a step-down application. Voltage waveforms are generated by a controller and are fed to the switches, denoted as S1 through S4 in Figure 2-1, which amplifies the signal based on feedback from the output to adjust the duty cycle (waveforms explained in description of Figure 2-2) of the Pulse-Width Modulation (PWM) signal that is fed into the switches. If the load requires more power, the controller will adjust the duty cycle of the PWM signal and the transistors will switch currents over the transformer for a longer period of time thus increasing the output power. The part denoted as Tx in Figure 2-1 [7] refers to the high-frequency transformer that electrically isolates the primary and secondary (low-voltage) sides. Finally, the rectifier stage converts the high-frequency AC back into DC (D1 through D4). This stage also involves a capacitor, C_0, to filter out any ripple voltage present in the output.

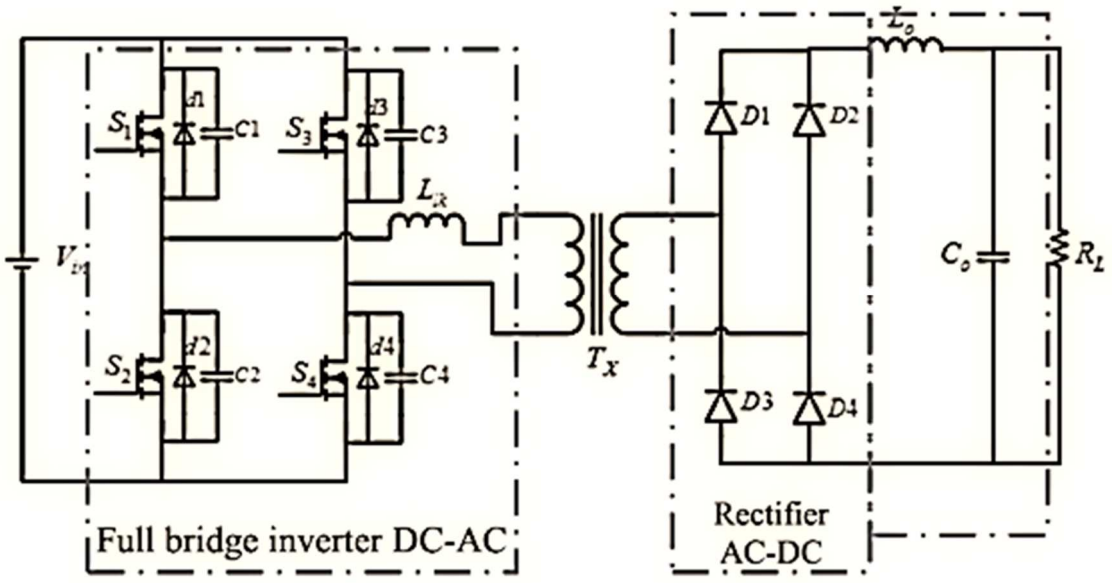


Figure 2-1: Typical DC/DC converter [7]

Shown in Figure 2-2 [1] is the equivalent PWM waveforms for the circuit shown in Figure 2-1. It can be seen that in this example the PWMs also makes use of a phase shift in between switches (sometimes also referred to as dead-time).

The equivalent duty cycle (D_{s1}) percentage for switch 1 (S1) in Figure 2-2 can be calculated as follow (t indicates timestep):

$$D_{s1} = \frac{t4 - t0}{t10 - t0} \times 100 \tag{2.1}$$

This is the percentage of time for which switch 1 is turned on. The output voltage (dependent on the PWM duty cycle) of a power converter be calculated as follow:

$$V_o = V_{in} \times \left(\frac{N_s}{N_p}\right) \times D_{eff} \tag{2.2}$$

Where N_s is the number of windings on the secondary side of the transformer and N_p is the number of windings on the primary side of the transformer. The input and output voltage is denoted as V_{in} and V_o while D_{eff} is the effective duty cycle – the time duration the voltage is switched over the transformer primary side to achieve the wanted output voltage at the output winding. V_p is the voltage waveform applied to the transformer, I_p is the equivalent current waveform and V_s is the voltage waveform at the secondary side of the transformer.

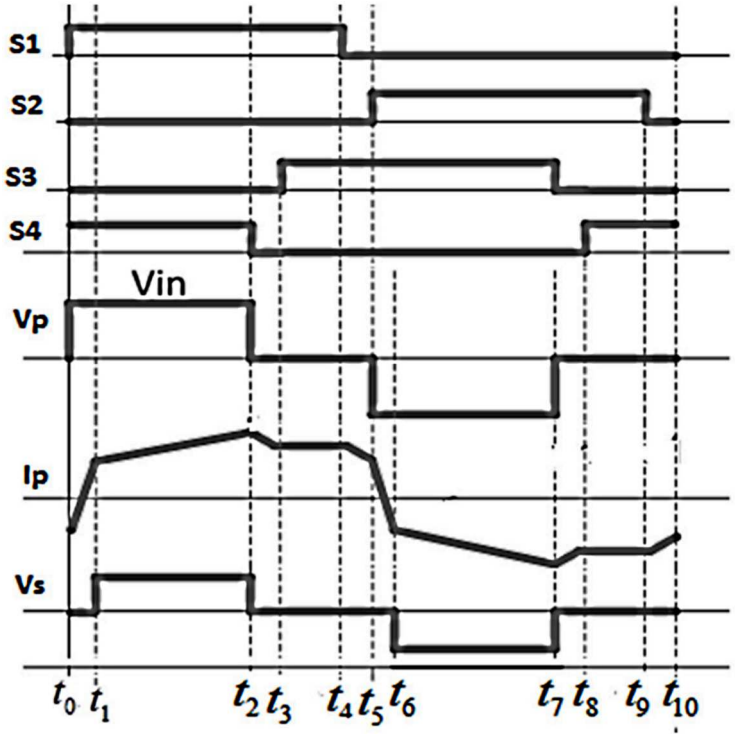


Figure 2-2: Equivalent waveforms [1]

SMPS topologies may vary between buck (step-down), boost (step-up) or buck-boost (both step-up and step-down). A flyback transformer topology is also used for high power requirements and can be used in a full bridge, half bridge or push-pull configurations. Efficiencies can be further improved by using resonant topologies that is able to utilize Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS).

2.1.1.1 Push-Pull

This power supply topology requires a center-tapped transformer at the primary side, commonly referred to as a dual drive winding as shown in Figure 2-3 [8], which is essentially two inductors that is magnetically coupled to the output inductor. This utilizes the core of the transformer much more efficiently [17], in contrast to a single stage flyback converter that uses only a single MOSFET, and requires a smaller sized transformer. The advantage of this kind of topology is that it can be easily scaled up to higher power levels. Precise control of the switching components are required since the two primary transistors, referred to as Q1 and Q2 in Figure 2-3, cannot be turned on at the same time as this will cause a short circuit. When this occurs, equal but opposite flux levels will occur in the transformer core, which will lower the input impedance to a very low level, causing a very high current to flow which will result in component damage. The disadvantage is that stresses are very high on the switching components as the primary transistors must perform hard switching due to the stress voltages, which are twice the input voltage. Another disadvantage is the inductance imbalance in the two primary windings [18]. This is due to the two windings, referred to as Np in Figure 2-3, being wound on the same core, the outer winding is wound over the inner winding and therefore has a larger diameter. It also means the outer winding is longer in length than the inner winding, even though they both have the same number of turns.

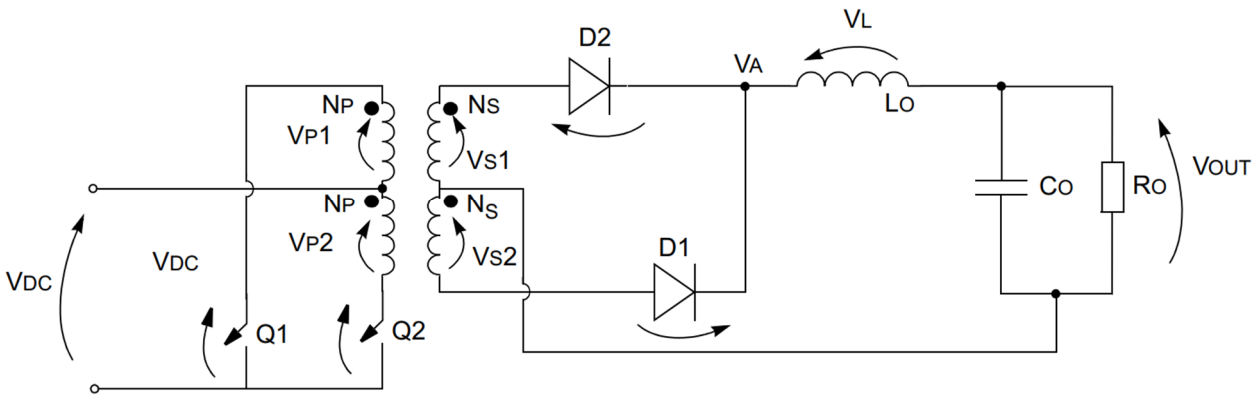
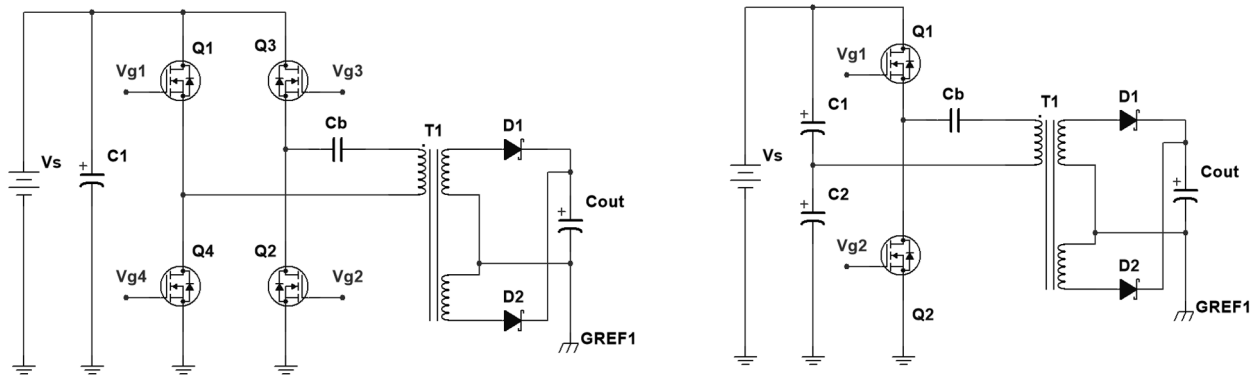


Figure 2-3: Push-Pull topology [8]

2.1.1.2 Full Bridge

The full bridge topology requires four switching transistors and is able to utilize the transformer better because the voltage reverses polarity, causing a magnetic flux that is equal in magnitude in both directions. This topology has the advantage of being converted to a much more efficient and higher power output device. Depending on the switching technique used, the topology can be used for both hard and soft-switching. Phase-Shifted switching can be applied to achieve ZVS, but it has the disadvantage of no ZVS during light load conditions [19]. Therefore Phase-Shifted Full-Bridge (PSFB) converters have conditional ZVS and the switching control is difficult to implement [20].

Figure 2-4 shows the full-bridge topology on the left (a) and the half-bridge topology on the right (b). The switching devices are shown as Q1 to Q4 in the full-bridge circuit and Q1 and Q2 in the half-bridge.



a) Full-Bridge b) Half-Bridge

Figure 2-4: Full and Half-Bridge topology

2.1.1.3 Half Bridge

The half-bridge topology, shown in Figure 2-4 (b), uses two primary switching components and two large capacitors, and can also be used for both hard and soft switching, both transistors cannot be switched on at the same time and require a dead-time during which both switching devices should be turned off. This is required to prevent the switches from turning on at the same time which will cause a short-circuit. This will also limit the maximum duty cycle to about 45 %. Switching stresses are equal to the input voltage, making the design easy and reliable [21].

2.1.1.4 LLC Resonant Converter

The LLC resonant converter can be implemented in the push-pull, half-bridge and full-bridge power converter. There are many configurations for a resonant converter, they are series, parallel and series-parallel resonant converters. The LLC resonant converter (series resonant converter) uses additional components in the primary circuit that is connected to the transformer's primary coil. It uses a resonant capacitor in series with the transformer and utilizes the leakage inductance

of the transformer to form a resonating circuit [22]. This makes it possible to vary the switching frequency and achieve ZVS under both no-load and full-load conditions. Transistor turn-on losses will be reduced, resulting in a lower power dissipation in the transistor and ultimately less heat, a higher reliability [23] and a more dynamically adjustable power supply.

The LLC resonant converter has a variable gain that is calculated as follow:

$$Gain = B_g \times R_g \times N \tag{2.3}$$

Where B_g is the bridge gain (1 for a full-bridge and 0.5 for a half bridge), R_g is the resonant tank gain (determined by frequency) and N is the transformer ratio [24].

The resonant tank circuit can be simplified to the circuit shown in Figure 2-5 where C_r is the resonant capacitor, L_r is the leak inductance of the transformer but can also be an external inductor or the sum of both. the transformer magnetizing inductance is denoted as L_m. When a power converter has no-load connected to it, the magnetizing inductance will be high, but when the load is increased, the magnetizing inductance will drop [9]. The simplified model shows the load resistance as Rac and is modelled as a resistor in parallel with the magnetizing inductor on the primary (input) side of the transformer.

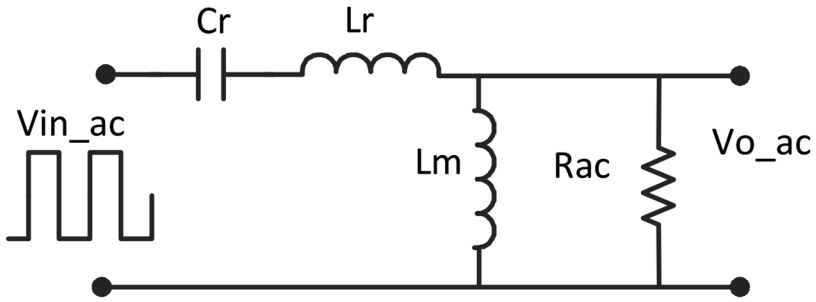


Figure 2-5: Simplified tank circuit [9]

The transfer function of the circuit shown in Figure 2-5 [9] is given by the following equation:

$$K(Q, m, F_x) = \left|\frac{V_{o_{ac(s)}}}{V_{in_{ac(s)}}}\right| = \frac{F_x^2(m-1)}{\sqrt{(m \times F_x^2 - 1)^2 + F_x^2 \times (F_x^2 - 1)^2 \times (m-1)^2 \times Q^2}} \tag{2.4}$$

where each symbol is defined as follow:

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \tag{2.5}$$

Q is the quality factor and it can be seen that for this kind of converter, the quality factor will improve as the load is increased because R_{ac} decreases when the load increases.

$$R_{ac} = \frac{8}{\pi^2} \times \frac{N_p^2}{N_s^2} \times R_o \tag{2.6}$$

R_{ac} is the reflected load resistance that is in parallel with the magnetizing inductance of the primary coil of the transformer. This is calculated from the load resistance, R_o, at the output of the converter.

$$F_x = \frac{f_s}{f_r} \tag{2.7}$$

F_x is the normalised switching frequency of the converter, f_r is the resonant frequency (natural frequency) and f_s is the frequency at which the converter is currently operating. The switching frequency, f_s, is determined by the controller.

$$f_r = \frac{1}{2 \times \pi \times \sqrt{L_r \times C_r}} \tag{2.8}$$

f_r is the resonant frequency of the leak inductance and the resonant capacitor. Switching at or above this frequency will result in ZVS for any load condition.

$$f_{r2} = \frac{1}{2 \times \pi \times \sqrt{(L_r + L_m) \times C_r}} \tag{2.9}$$

f_{r2} is the lowest frequency the converter can operate at during no-load while achieving ZVS. Switching between f_r and f_{r2} results in conditional ZVS and is dependent on the load.

$$m = \frac{L_r + L_m}{L_r} \tag{2.10}$$

m is the total primary inductance to leak inductance ratio. Figure 2-6 shows how the resonant tank circuit is implemented in a half-bridge converter. It can also be applied to the full-bridge converter to increase the efficiency and power capability.

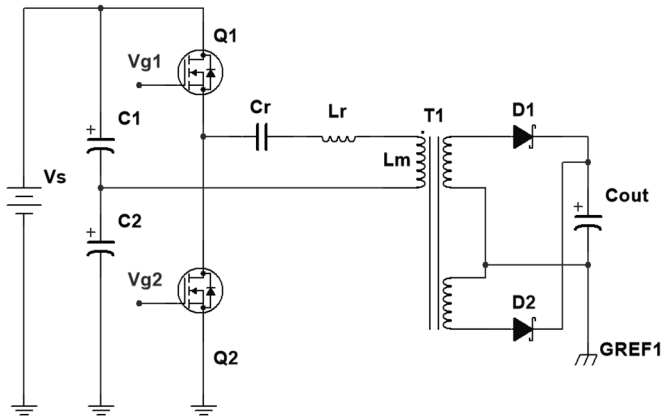


Figure 2-6: LLC Resonant Converter in a half-bridge converter

The LLC resonant converter has three operating regions, below resonance (ZCS), above resonance (ZVS) and a region where both ZVS and ZCS can occur (load dependent) [25]. During a short-circuit condition, the magnetizing inductance will drop to a very small value and the resonant frequency is given by (2.8). This is because the magnetizing inductance is short-circuited and the resonant frequency increases. During a no-load condition, the resonant frequency is given

by (2.9). When a finite load is applied to the resonant converter, the actual resonant frequency is between (2.8) and (2.9).

Figure 2-7 shows the three regions where the LLC resonant converter can operate in. During a light-load condition (shown in green), the peak gain is marked as (A). If the resonant frequency is lowered, the converter will operate in ZCS mode, which is also referred to as the capacitive region because the current waveform in the resonant tank circuit will lead the voltage waveform.

If the converter is operated at the resonant frequency, point (A), then the current and voltage waveforms of the resonant tank circuit will be in-phase and the converter will represent a resistive load in which both ZVS and ZCS is achieved. If the converter is operated above this point (to the right), then the converter will operate in the inductive region because the current waveform will lag the voltage waveform and the converter will achieve ZVS.

Conditional ZVS happens in the area encircled in purple. This is because the gain curve shifts to the right as the load is increased, shown in point (B), because the magnetizing inductance decreases. The new inductive region is now on the right side of point (B) and the capacitive region is to the left of point (B).

If the converter output is short-circuited, then the gain-curve loses the capability to boost the voltage (red) in the resonant tank circuit and the maximum gain that can be achieved is 1. The gain curve also shifts to the right and is now centered around point (C). Short-circuit protection can be implemented by rapidly increasing the switching frequency above point (C) when a short-circuit occurs at the output to prevent the converter from losing ZVS.

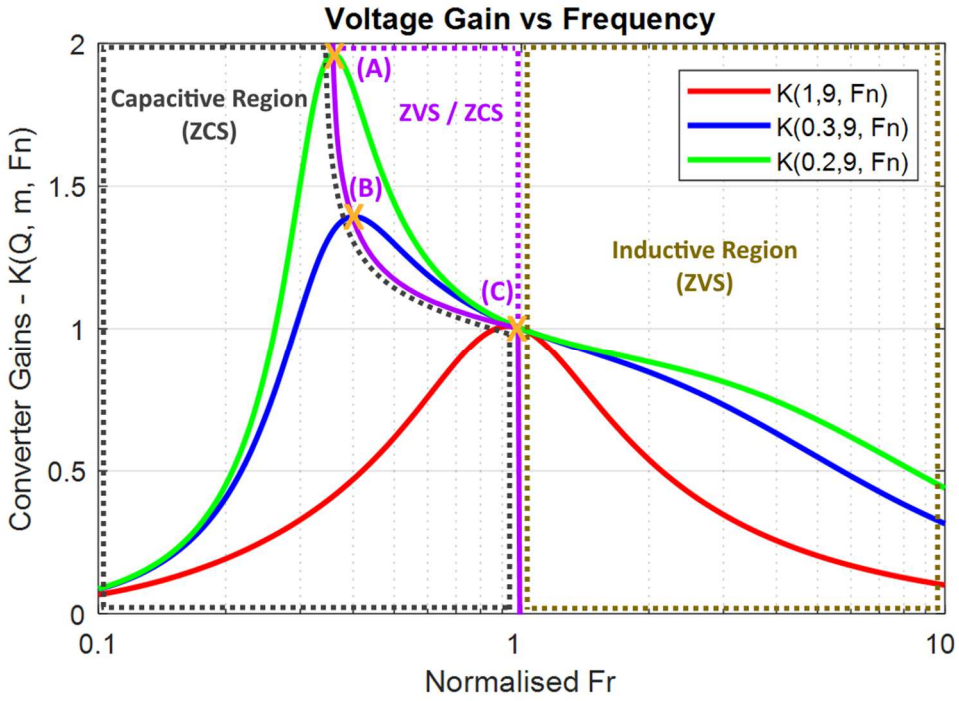


Figure 2-7: LLC Resonant Converter operating regions

This kind of converter has the ability to achieve high energy efficiency while also reducing EMI. It can also operate at a wide input voltage range because the gain during light-load conditions can go above 1 (depending on the design). The disadvantage of this converter is that it is difficult to regulate the output voltage [26]. A thorough design procedure is discussed in the next chapter for such a converter.

2.1.1.5 Direct coupling – no converter

Direct coupling is a method to match a solar panel to an electrolyser or vice versa for a direct electrical connection but it presents some solar panel to electrolyser matching challenges. Sizing is the biggest challenge for matching a renewable energy source to an electrolyser [27]. Even when this matching is done properly, the change in temperature and solar irradiance will cause a mismatch during certain periods of time when operating conditions differ from what was determined as “suitable” during the direct coupling optimization process.

The direct connection of a solar panel to an electrolyser requires the precise matching of the electrolyser to that solar panel or array of panels. This is based on certain assumptions that takes different operating conditions for the PV panels into account to maximize the power supplied to the electrolyser as more power will result in a higher hydrogen production rate. As conditions change, the MPP point of the solar panels will change which results in a reduction in the amount of real-time power supplied to the electrolyser. This will in turn lower the amount of hydrogen produced over a long period of time and thus decrease the system efficiency.

2.1.2 The MOSFET

A metal–oxide–semiconductor field-effect transistor (MOSFET) is an electronic device where an input voltage determines the output conductivity of the junction. This ability makes the device suitable for amplifying or switching electronic signals in analog or digital circuits [28]. They are made with either n-type or p-type semiconductors (which are complementary pairs). Due to the MOSFET being a voltage controlled device, it requires almost no input current which is in contrast with a Bipolar Junction Transistor (BJT).

Power MOSFETS are the preferred switching device in many power converters [29], but there are many aspects that needs to be considered when designing a power converter for maximum efficiency and reliability. In this section, a detailed literature regarding transistor soft-switching is discussed to better understand what is meant by the terms soft and hard switching.

This involves a detailed discussion of the internal functioning of a power MOSFET and the requirements needed to correctly drive a power MOSFET in a soft switching converter. In this mode of operation, certain criteria must be met or the transistor may fail permanently. It is thus critical to fully understand this section of the literature as this will help to better understand how a power MOSFET should be matched to a particular power converter to obtain both high efficiency and high reliability.

2.1.2.1 Hard and soft switching explained

In the hard switching mode of operation, the power density is low, the physical size of the converter is increased and as a result the cost is also higher. Current and voltage waveforms will also overlap during switching which will lead to an increase in both EMI (Electromagnetic Interference) and RFI (Radio-Frequency Interference). The device is also exposed to very high current and voltage transients, also referred to as hard commutation events, which may lead to MOSFET failure, which is the reason why soft switching is preferred. In the soft switching mode of operation, the voltage at the output of the switch (MOSFET) is zero or close to zero during turn-on and turn-off transitions.

Zero Voltage Switching (ZVS) is the preferred soft switching method for a MOSFET operating at high switching frequencies since the internal capacitance (parasitic capacitance) is not discharged into the drain-source junction at every turn-on cycle. In hard switching converters, this discharge is converted to heat and becomes higher as the switching frequency is increased. Ultimately, ZVS also decreases EMI and RFI dramatically due to the absence of voltage and current transients and eliminates the need for snubber circuits generally required in a hard switching converter to protect against primary breakdown in the MOSFET junction. Also important to note is that the intrinsic capacitances of a MOSFET becomes more important to take into consideration the higher the operating frequency, because the charging and discharging of these intrinsic capacitances will determine the response times of the MOSFET such as turn-on and turn-off delays. Drain to gate capacitance (Cgd) and the potential across it is referred to as "Miller". The Miller effect is defined as the unwanted capacitive (can be any impedance) coupling between the input and output of an amplifier that affects the gain and input impedance. This is unwanted because it will increase (under imperfect switching conditions such as hard switching) the apparent input capacitance of the MOSFET and therefore also increase the current required to charge or discharge the gate, which will result in slow turn-on or turn-off times and ultimately higher switching losses.

2.1.2.2 Advantages of soft switching

During ZVS operation, the miller effect is eliminated during turn-on and turn-off events because the MOSFET output capacitance is already fully discharged. This causes the negative effect of output to input capacitance relation, as perceived by the MOSFET gate driver, to become very stable and consistent, even though the parasitic capacitances are still present. This also improves efficiency as the MOSFET drain-source junction doesn't have to discharge the output capacitance into the junction itself, which will result in high current transients and heat generation inside the MOSFET. The output capacitance of the MOSFET (denoted as $Coss$ or Cds in device datasheets) is discharged by the circuit's parasitic inductances (usually transformer leak inductance as well as PCB traces) and internal MOSFET capacitor combination [29]. In perfect or near perfect ZVS mode, the MOSFET input capacitance is simply the parallel combination of the gate to source (Cgs) and gate to drain (Cgd) capacitances. An equivalent model for the MOSFET, including its parasitic capacitances, are shown in Figure 2-8 [5].

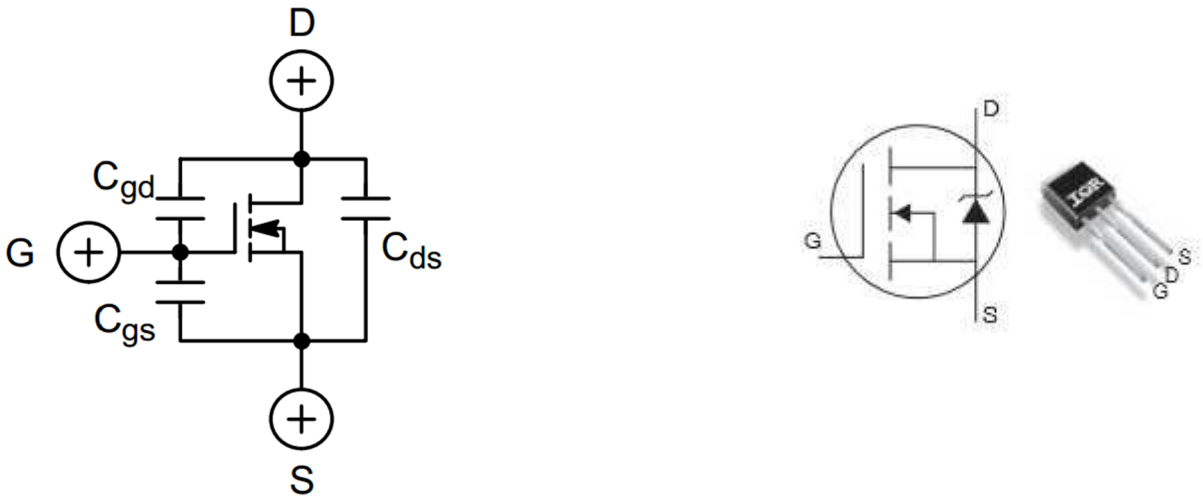


Figure 2-8: MOSFET equivalent model [5]

Parasitic capacitances in a MOSFET are not constant as they depend on the charge and voltage applied to the MOSFET [5]. Therefore, it is difficult to accurately determine the gate drive requirements of the MOSFET for a hard switching converter as the capacitor combination changes during each switching cycle. In the ZVS mode, this is not the case and the gate drive requirements can be predicted very accurately. Fortunately, manufacturers show the total gate charge (Qg) of the MOSFET, which is applicable to hard switching modes as this represents a worst case scenario [30]. Only a very few manufacturers show the effective gate charge for ZVS mode (Qg_{ZVS}).

2.1.2.3 The impact of dv/dt on the MOSFET

The dv/dt rating of a MOSFET refers to the rate of voltage change over its drain to source terminals and represents the voltage transients experienced by the MOSFET due to an inductive

load, as shown in Figure 2-9 [4]. This happens during the Miller plateau region (plateau implies the gate voltage does not change during this moment) of the switching transition. This means that the output of the MOSFET has a non-constant capacitive coupling to the input that affects the input (gate voltage) of the MOSFET as the output (drain current) is transitioning during a switching cycle. An excessive dv/dt rate may cause a false turn-on condition that will cause permanent damage to the MOSFET. The maximum dv/dt capability is a parameter that is given in the datasheet for a MOSFET.

As shown in Figure 2-9 [4], a gate-drain current will flow through capacitor Cgd and is given by the equation $Igd = Cgd \times \frac{dv_{gd}}{dt}$. This happens during the Miller plateau region and is caused by the rate of voltage change (dv/dt) at the drain-source capacitance, Cgd, regardless of the voltage and current sourced by the gate driver. During this Miller plateau, the MOSFET is in the process of forming a large capacitor between the gate and GND. Capacitor Cgs and Cgd will thus be in parallel when the MOSFET reaches its fully turned-on state (drain and source is short circuited).

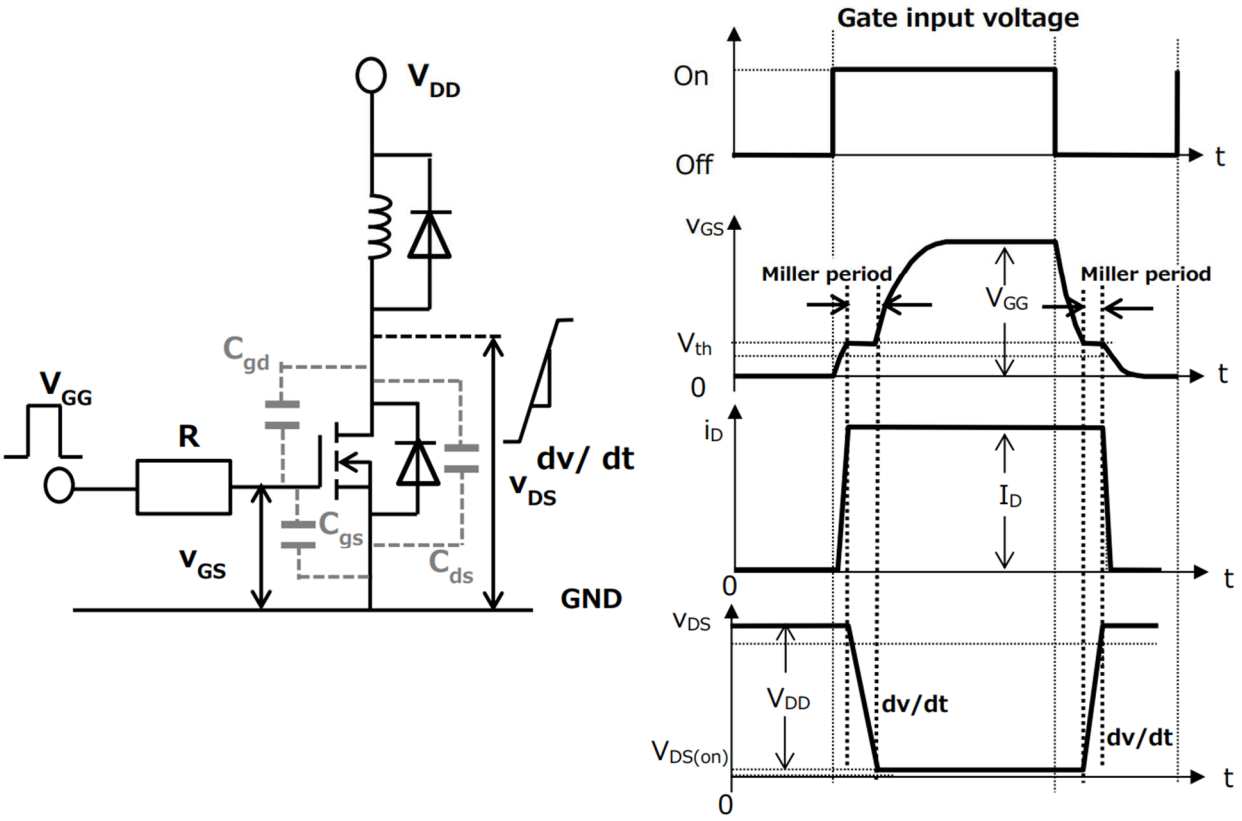


Figure 2-9: Inductive switching circuit and waveforms [4]

In the fully-turned on state, the resistance of the MOSFET is given by its Rds_{on} value in the datasheet. This is the reason why zero-voltage switching is preferred as the MOSFET's drain to source voltage will be at zero voltage when the device is switched on. During this mode of operation, the miller effect is completely eliminated and the effective capacitances of the MOSFET

will be close to being constant. This will also reduce the workload of the gate driver during the Miller plateau region.

When a high dv/dt condition occurs, normal operation of the MOSFET is affected as follow:

1.) The drain-source junction experiences a change in voltage during switching transitions such as during turn-on or turn-off which has a negative impact on normal operation by means of feedback to the input.
2.) In circuits having an inductive load, multiple pairs of MOSFETS (as used in a half or full-bridge topologies) may all be exposed to this phenomenon at the same time. It can also be caused if the intrinsic body diode of the MOSFET is transitioning from freewheel mode to reverse recovery mode.

To prevent the possibility of a high rate of voltage change during the turn-off cycle, a RC (resistor in series with a capacitor) can be placed across the drain-source pin of the MOSFET. This in only required in hard-switching applications because in a soft-switching converter, this will never occur.

2.1.2.4 Body diode reverse recovery

Switching converters driving an inductive load will use multiple MOSFETs, two for a half bridge and four in a full bridge configuration. During switching, an inductive load will generate voltage transients or back-EMF's due to a current that flows through the inductor. These voltages, given by $V_L = L \times \frac{di}{dt}$, will be relayed back to the power supply (depending on the switching topology) source via an intrinsic body diode that is present inside the MOSFET.

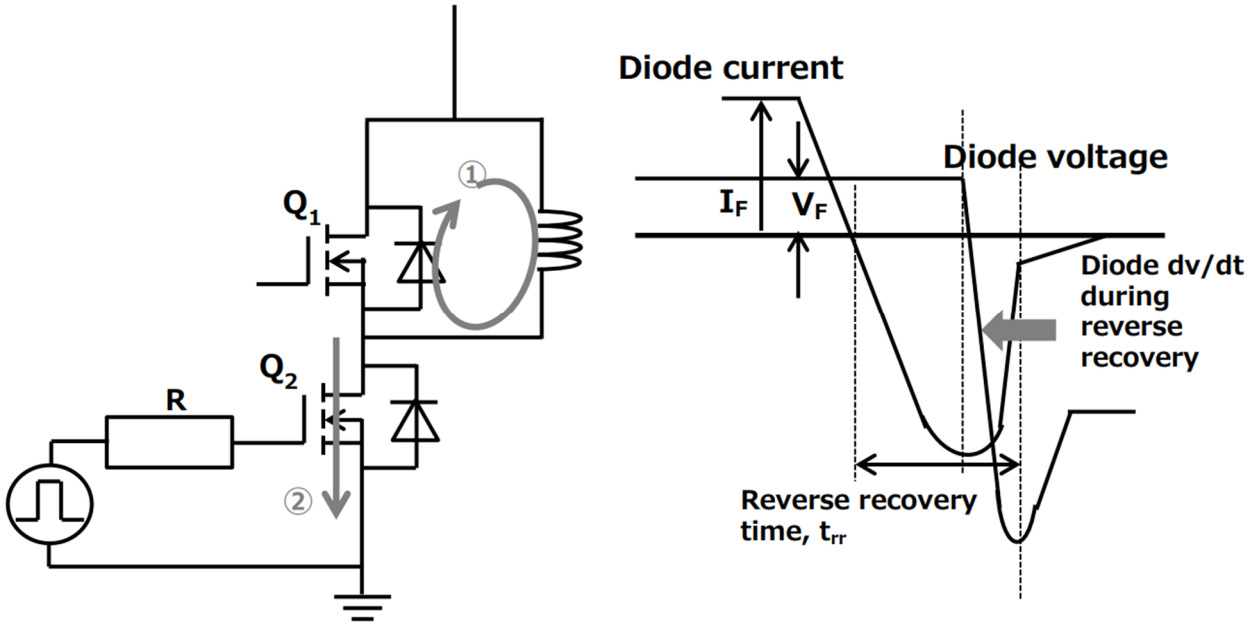


Figure 2-10: Body diode reverse recovery [4]

The body diode has a reverse recovery time during which it will conduct current in both directions for a moment before being able to block a voltage again.

During switching operation of the converter bridge shown in Figure 2-10 [4], the following will happen:

1.) If an inductor current is flowing through the low side MOSFET, Q2, and the device is then turned off, a freewheel current, I_f, will flow through the body diode of Q1.
2.) Q1 will then have a voltage drop equal to V_f, the forward voltage drop of the diode for that particular current vale, over its intrinsic body diode.
3.) When Q2 is turned back on again, a current loop will flow again through transistor Q2 and the body diode of Q1 will be entering a state which is known as reverse recovery, which will cause its drain-source voltage to rise very rapidly (dv/dt).

It is therefore important to look at the reverse recovery times of the intrinsic body diode of the MOSFET as this might also cause a false turn-on of the MOSFET, especially if the back-EMF's generated by the inductive load causes the body diode to act and exceed the rated dv/dt value of the MOSFET [31]. This may also turn on the parasitic BJT (Bipolar Junction Transistor) that is present in the MOSFET. A fast recovery diode can be added externally to the MOSFET's drain-source junction as shown in Figure 2-10. This will prevent the triggering of the parasitic BJT that is present inside all MOSFETs [32].

2.1.2.5 The parasitic BJT (Bipolar Junction Transistor)

The Power MOSFET's internal structure has a parasitic NPN BJT that is formed at its internal junctions. This effect is not observed during the turn-on of the power MOSFET as the parasitic BJT's effect is supressed due to the junction being in a short-circuit mode. The drain-source junction, between the N+ and the P- regions shown in Figure 2-11, of the MOSFET has a very low resistance, referred to as Rds_{ON} in the datasheet, when the gate-source is forward biased. This makes the device less prone to parasitic BJT turn-on during the MOSFET turn-on state, but during the turn off cycle of the MOSFET as used in a UIS (Unclamped Inductive Switching) circuit, a small current may flow more easily through the parasitic capacitance, denoted as C_{DB} in Figure 2-11, associated with the depletion region of the body diode [33]. During this stage, if the current exceeds the base current required to turn-on the parasitic BJT, the device will short-circuit permanently and self-destruct.

In spite of this, this mode of failure can still occur during device turn-on, as seen in Figure 2-11 [6] the BJT can still be turned on at location A as the resistance Rpb is finite at the base of the P-region. This means that switching in a UIS circuit where a high dv/dt at the drain, during reverse recovery mode of the diode, will cause the P-base and N-drift (Epi) junction to collect current that flows through the junction to the P-region will cause a voltage drop across R_{PB} that will bias the

parasitic BJT [6]. The BJT is a current controlled device that is forward biased at the junction between the N+ source region and the P-base region.

When the gate driver attempts to switch off the BJT, the blocking voltage capability of the power MOSFET structure has already been compromised, which will cause self-destruction. The equation that describes this voltage ramp type failure mode is given by [6]:

$$i_D = C_{DB} \times \frac{dV}{dt} \tag{2.11}$$

And dV/dt represents the voltage ramp that will trigger the MOSFET into a latch (stuck) condition. The voltage ramp for the parasitic RC circuit can also be written as:

$$\frac{dV}{dt} = \frac{V_{BE}}{R_{PB} \times C_{DB}} \tag{2.12}$$

V_{BE} is the base-emitter voltage and R_{PB} is the parasitic resistance. C_{DB} is the drain-to-base parasitic capacitance between the MOSFET and the BJT.

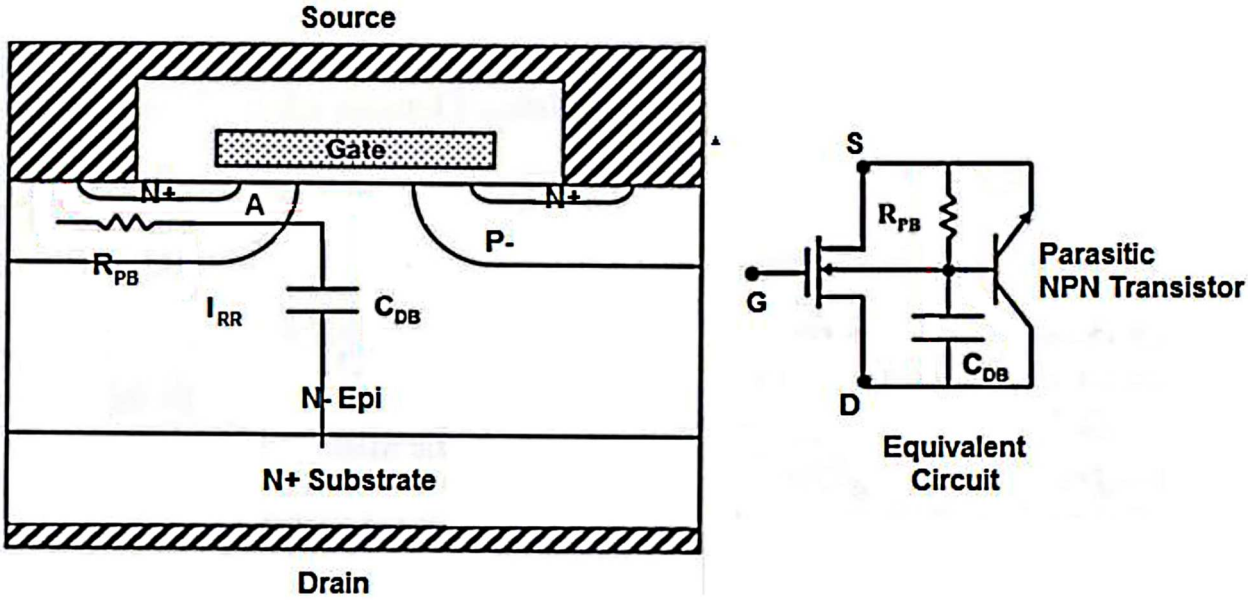


Figure 2-11: Power MOSFET internal structure with parasitic BJT [6]

To prevent this from happening, an RC snubber circuit can be added externally in parallel to the MOSFET. This voltage spike will cause a current spike in the externally added (connected to the drain-source pin of the MOSFET) RC circuit instead of the parasitic RC circuit inside of the MOSFET. The addition of fast recovery steering diodes (also called avalanche or freewheeling diodes) can also help to prevent the triggering of the parasitic BJT that is present inside the MOSFET.

2.1.2.6 MOSFET Avalanche

When a semiconductor is exposed to a voltage transient that exceeds its rated breakdown voltage, the device is said to operate in avalanche mode [10]. When the device is operated above its rated voltage, this will cause high voltage electric fields in its p-n junctions. Electron-hole pairs are formed that undergo a multiplication effect that will also lead to a transient current or sudden increase in current [34]. This energy is absorbed by the device which will cause a progressive increase in the on-state resistance (Rds_{ON}) [35]. This affects the device's reliability as it causes the junctions inside the device to slowly ionize over time, leading to higher leakage currents, slower switching times, worse conduction in the on-state and sudden, unpredictable failure.

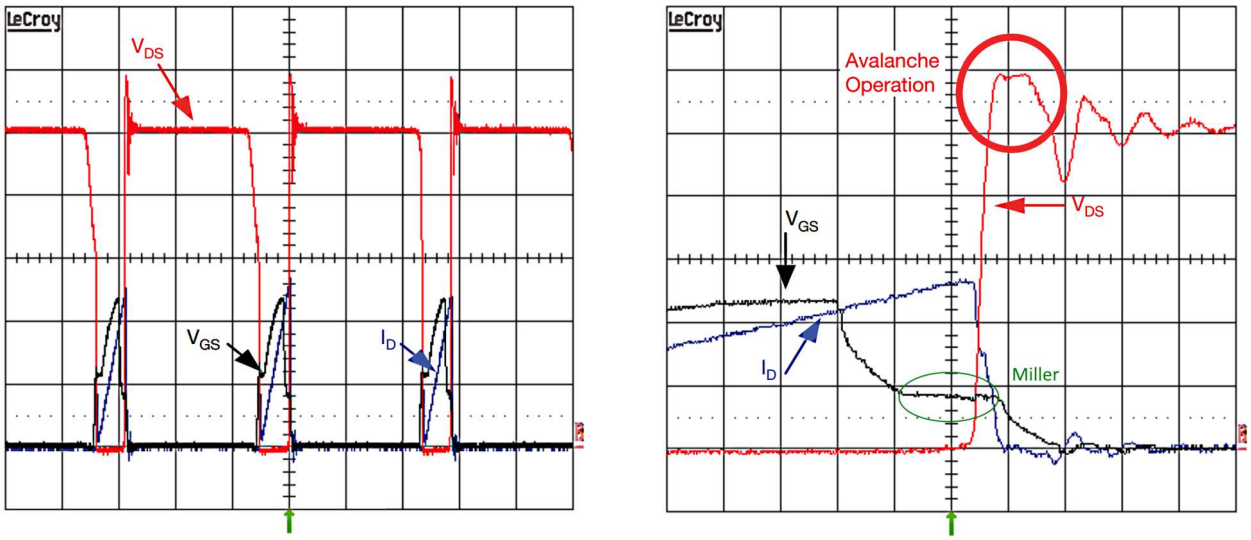


Figure 2-12: MOSFET Avalanche operation [10]

The waveforms in Figure 2-12 [10] represents a MOSFET that is operated under avalanche conditions that causes impact ionization. During avalanche, the drain-source voltage, indicated in red, is clamped (absorbed) by the MOSFET junctions and a current will flow through the junction. Significant ringing in the drain-source voltage can be seen during this occurrence - although ringing does not necessarily imply avalanche. Ringing is caused by parasitic inductances that store energy and then releases this energy back to the source, such as transformer leakage inductances. To the right-side of Figure 2-12 [10] the avalanche effect can be clearly observed as the drain-source voltage is clipped-off while the overlapping current waveform, shown in blue, is overlapping the voltage waveform. As can be seen in the black waveform, which indicated the gate-source voltage, the Miller effect is present and also overlaps the voltage and current waveforms. This is the avalanche operation in progress that may also trigger the parasitic BJT, but even if the parasitic BJT is not triggered into biasing, continuous operation in this mode will cause permanent damage to the MOSFET junction. This problem can only be solved by using a soft-switching power converter topology or by adding diodes and snubber circuits externally to the MOSFET.

2.1.3 Photovoltaic panels

Solar cells make use of the photoelectric effect which is the ability of some semiconductors to convert electromagnetic radiation to an electrical current. The magnitude of the electrical current depends on the amount of electromagnetic radiation each solar cell is exposed to. The rated efficiency of photovoltaics (PV) as tested in the laboratory often differs from that obtained outdoors by up to 18%. A study done in Greece found the annual PV efficiency to be around 8.7% [36]. The presence of dust on the PV panels will also decrease the efficiency. It becomes obvious that solar panels do not have a wide dynamic range in which it can perform efficiently. Therefore, solar trackers are used to optimize the angle at which the sunlight hits the panels to keep the solar to electrical energy conversion process running at its maximum potential.

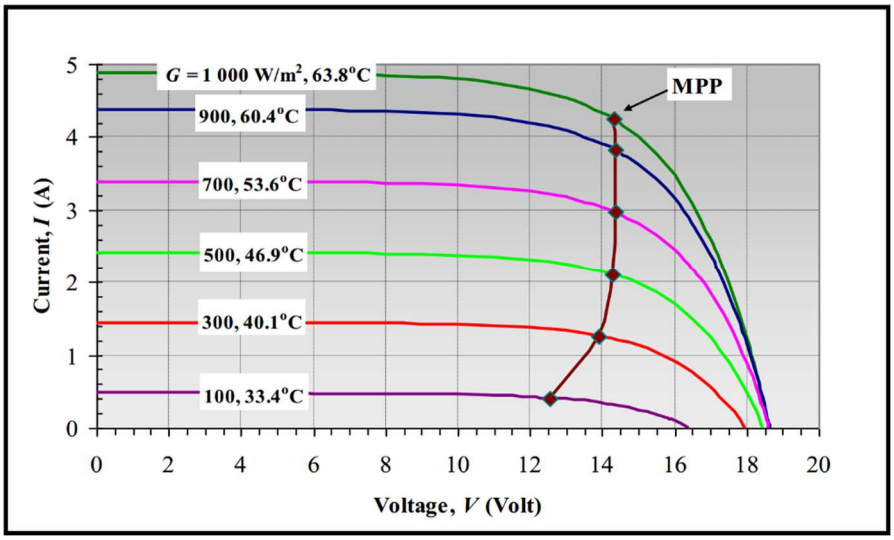


Figure 2-13: I-V characteristics for a BP275 solar module [11]

As irradiance and temperature changes, the characteristics of a PV panel also changes. This causes the already non-linear P-V and I-V curves to shift. Temperature changes will cause the output voltage to change whereas solar irradiance changes will cause fluctuations in the PV's output current. A point exists on the I-V curve which is known as the Maximum Power Point (MPP) [37]. This is the point at which the solar panel produces maximum power and when the PV is utilized at this point as conditions change, maximum energy (power integrated with regard to time) can be extracted from the panel. Figure 2-13 shows how the behaviour of a BP275 solar module changes as the irradiance and temperature changes. There is a drastic change in the MPP point as the conditions changes and requires a continual adjustment of the operating point to be able to keep it as close to its MPP as possible.

Due to the maximum power point being unknown as a result from the changes in irradiance and temperature, a Maximum Power Point Tracking (MPPT) algorithm is usually employed in the systems connected to the PV panels. The appropriate tracking algorithm is chosen based on the control variables involved, the type of regulation required, response time, cost, efficiency and the

system in which it will be employed. In the case where an electrolyser is directly coupled to the solar panels, it is required that the MPP point of the solar panels be determined first which involves a matching procedure. If the coupling is indirect with a DC-DC converter connected in-between, the DC-DC converter needs to employ an MPPT technique in order to adjust the impedance conversion process to keep the solar panels operating at their optimal point.

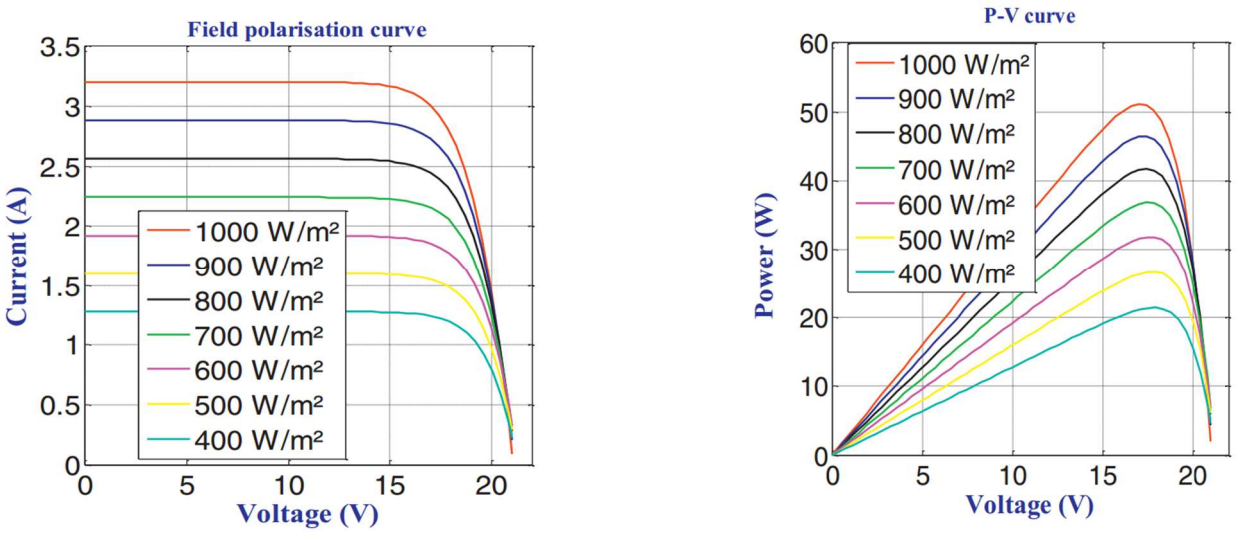
2.1.4 MPPT algorithms

Maximum Power Point Tracking (MPPT) is a technique used to allow the full utilization of the amount of power that a PV panel is able to produce [38]. MPPT is a programming algorithm running on an embedded system and makes use of no mechanical parts. It is thus not the same as a solar sun tracking system where an electro-mechanical system keeps track of the sun to keep the PV panels pointed directly into the sun.

There are two points on the I-V curve, V_{OC} and I_{SC}, where the power developed is equal to zero. This is called the open-circuit voltage and the short-circuit current respectively. The maximum power point on the VI curve is where the product of V and I is a maximum and is usually denoted as V_{mpp} and I_{mpp} to indicate the maximum power point for both the voltage and current. Unfortunately, the maximum power point is not static and changes as the temperature and amount of electromagnetic radiation changes.

Figure 2-14 shows a simulated I-V curve of a solar panel on the left side with its corresponding P-V curve shown on the right hand side [39]. The top of each curve in the P-V curve figure is the point at which maximum power can be extracted from the solar panel.

Different MPPT methods will be investigated in order to test and evaluate their performances when used in a DC-to-DC converter purposely designed for direct solar to hydrogen conversion. The different topologies for DC-to-DC conversion will also be investigated. Finally, an MPPT method will be implemented in the optimum DC-to-DC converter to achieve the highest efficiency and maximize hydrogen generation. Various MPPT algorithms will be investigated in order to determine the best solution suitable for use with Zero Voltage Switching (ZVS).



a) I, V simulation curve

b) P, V simulation curve

Figure 2-14: PV panel I-V curve [39]

The most commonly used methods for implementing MPPT are:

- Perturb and Observe (P&O) [40]
- Incremental Conductance (INC) [41]
- Current Sweep
- Short Circuit

Each of these methods will now be discussed in detail.

2.1.4.1 Perturb and Observe (P&O)

Both perturb and observe and incremental conductance are methods of hill climbing. These methods can “climb” the IV curve and thus attempt to find the true maximum power point of the PV panel. As seen in Figure 2-16, in the perturb and observe method, the microcontroller will need two sensors namely a voltage and current sensor which will serve as two feedback inputs. A continuous power point adjustment is made by increasing or decreasing the Pulse-Width Modulation (PWM) signal to detect if the adjustment increased or decreased the maximum power drawn from the PV panel.

Shown in Figure 2-15 is a basic circuit diagram showing how a DC/DC converter is generally connected to solar panels. The solar panel array is represented by Vin whereas the voltage and current sensors is represented by $Vpanel$ and $Ipanel$ and respectively. A microcontroller receives the measurements from the sensors to evaluate the real-time power curve of the solar panel array and make continual adjustments in the PWM signals, represented by $g1$ and $g2$, which is fed to the MOSFET gates as shown in the full bridge circuit block of Figure 2-15.

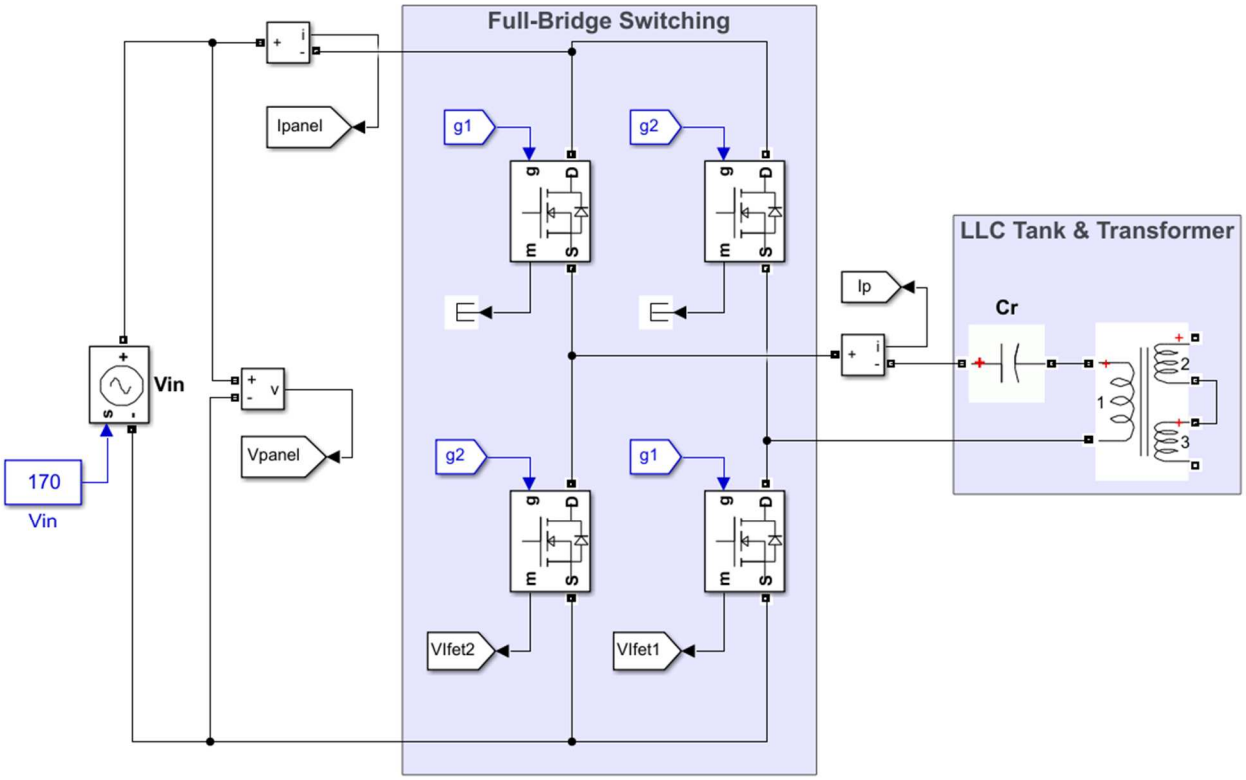


Figure 2-15: Basic PWM circuit

The drawback of using this method is that it may increase ripple in the output as the system makes continuous adjustments to the way current and voltage are switched. It never reaches the actual “true” maximum power point, instead it keeps the system running very close to the maximum power point. This method proves to be 99 % effective when the operating conditions, such as load requirements, do not change rapidly.

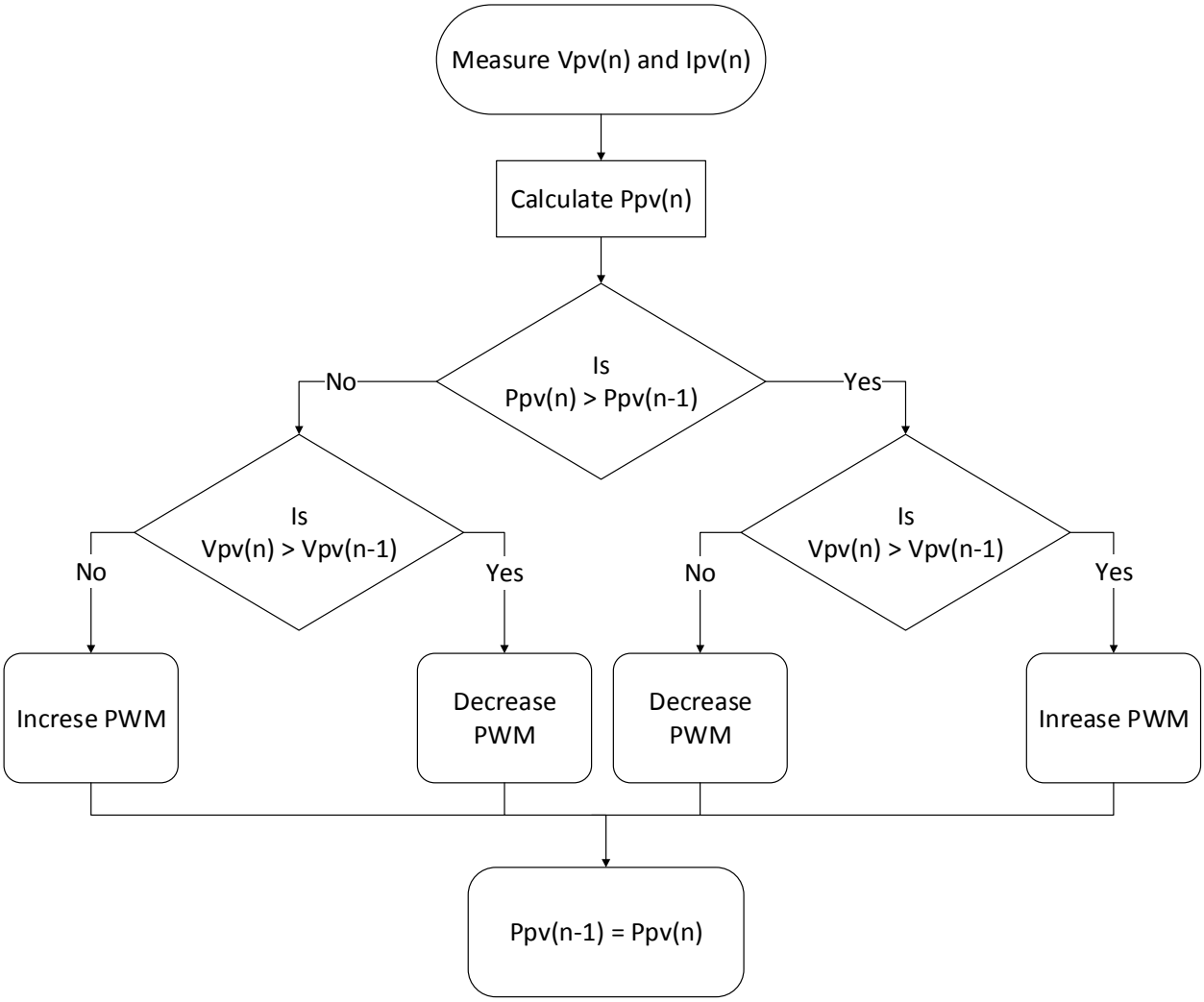


Figure 2-16: Perturb and Observe (P&O) MPPT algorithm

2.1.4.2 Incremental Conductance (INC)

The incremental conductance method is also part of the hill climbing method. It is based on the fact that the derivative of the power curve (slope) is zero at the point where the PV develops maximum power. The slope is positive on the left hand side of the curve and negative on the right hand side [42].

Shown in Figure 2-17, the system also requires two sensors for measuring voltage and current. The derivative is then calculated and based on the derivative the system will “sense” the current power point and is able to calculate by how much to increase the duty cycle. If both the voltage and current derivative is zero, the system will stop making adjustments, but will continue to make adjustments as soon as the slope changes. Hill climbing allows the system to make instant changes to the system, without having to take temperature and other environmental factors into account.

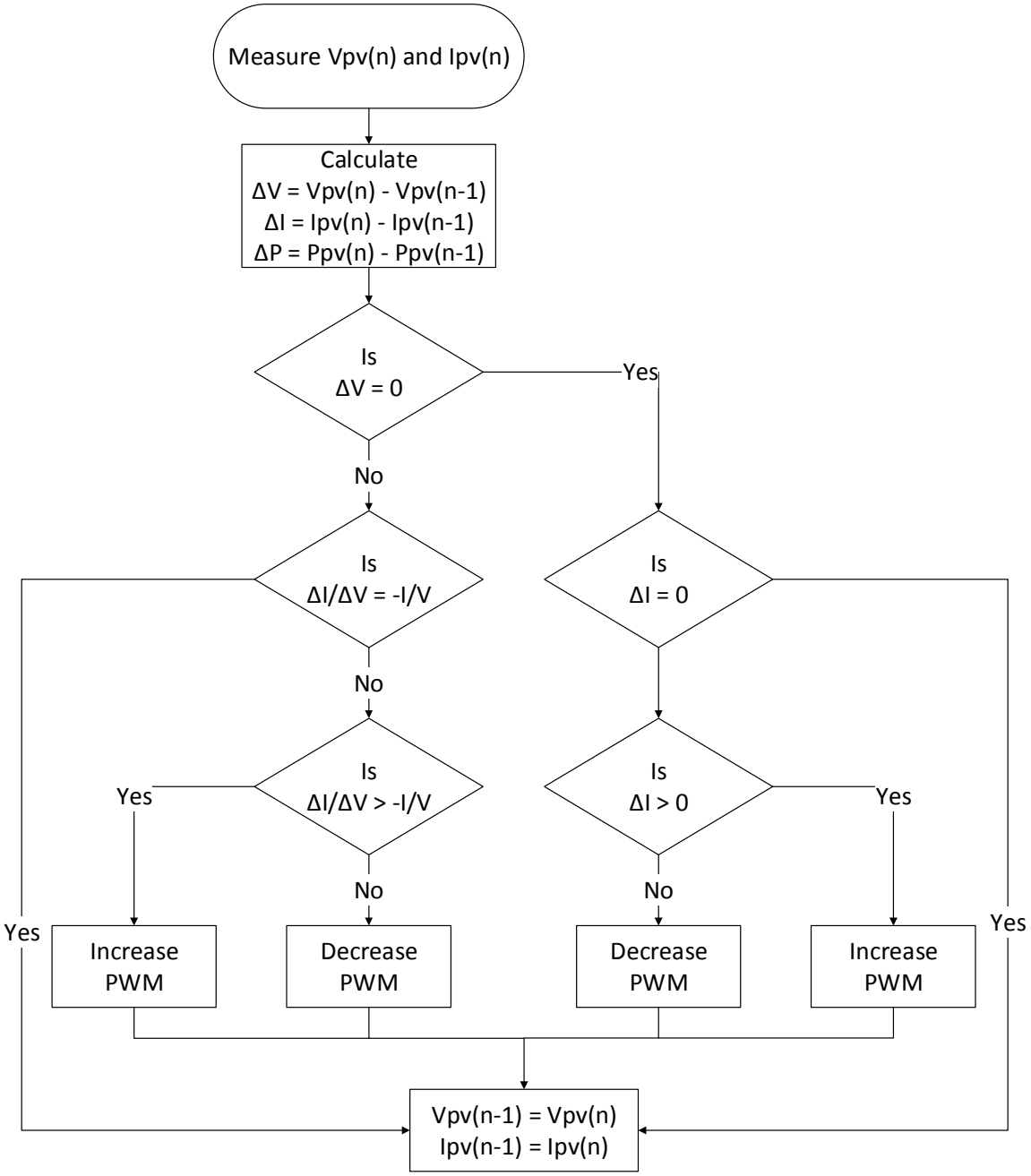


Figure 2-17: Incremental Conductance (INC) MPPT algorithm

2.1.4.3 Current Sweep

This method performs a current sweep on the PV panel's IV curve by measuring both current and voltage as it sweeps through the I-V curve by simulating an increasing load [43]. In this method, the system tries to determine the I-V curve directly. This can take up to 50 ms during each measurement interval which the cell is not necessarily at its MPP point [44].

2.1.4.4 Short Circuit

Figure 2-18 shows the concept of combination between the current sweep and short circuit method. A value for a constant, k, must be determined by measuring the short-circuit current for

the solar panel under ideal conditions. This value is multiplied by the short-circuit current value to determine the value of I_{mpp}. In this method, current sweep is regularly performed to ensure that the optimal value for k is selected [45]. A form of DC-chopper circuit is required for varying the PWM signal which will then find the current sweep curve.

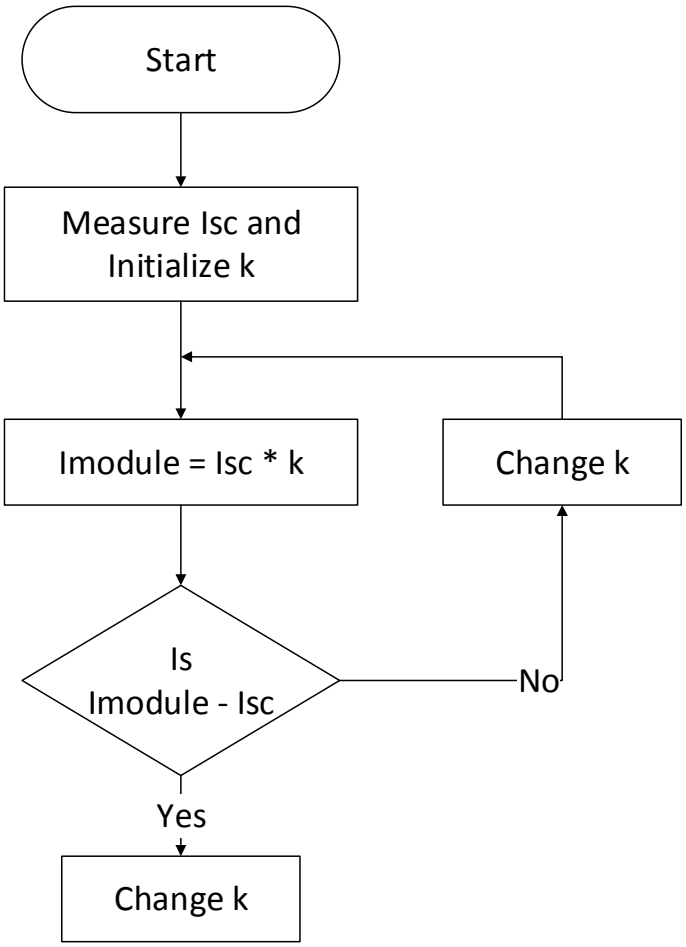


Figure 2-18: Current sweep & short circuit MPPT algorithm

2.1.5 High Frequency Transformer Design

In this section, different high-frequency transformer design strategies together with their trade-offs are discussed. The effect and cause of each design strategy is discussed as this is important to understand the design strategy that must be used for each type of transformer and the design challenges associated therewith.

2.1.5.1 Conventional HF Transformer

Conventional high-frequency transformers are designed for hard-switching applications where the transformer is designed to have a maximum magnetising inductance while having a minimal amount of leakage inductance. The conventional design process for such a transformer is to

calculate the product of the windowing area and the cross-sectional area of the core required for a certain power level [46]. This is calculated as follow:

$$W_a \times A_c = \frac{0.68 \times P_{out} \times d_w}{B_{\max} \times f} \tag{2.13}$$

Where each symbol is defined as follow:

- W_a is the windowing area of the core hosting the copper windings.
- A_c is the cross-sectional area of the core's centre leg.
- P_{out} is the output power level.
- d_w is the area of the wire used in the primary winding.
- B_{max} the maximum core flux density found in the datasheet and
- f is the desired switching frequency;

This factor must be multiplied with 1.3 to accommodate the space required for two secondary windings. It is also recommended to wind the secondary windings between the primary windings as indicated in Figure 2-19 [3]. This will require winding half of the primary winding on the bobbin, then the secondary windings and finally the rest of the primary windings on top of that. It is referred to as sandwiching and is done to reduce leakage inductance, proximity and skin effects [3].

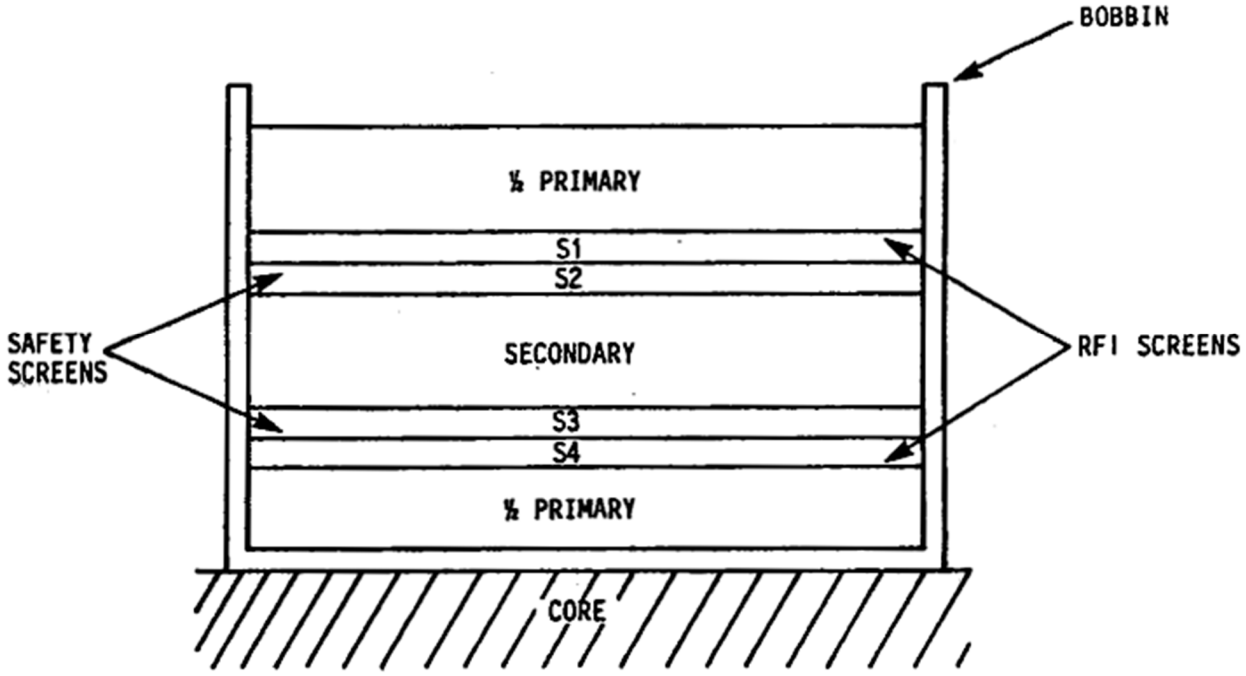


Figure 2-19: Recommended winding method [3]

During operation of the transformer, a fraction of the flux produced by the primary winding completes its path through the air instead of the ferrite material used for manufacturing the core. This is referred to as leakage flux [47] and contributes to the leakage inductance of the transformer. Energy stored in this part of the magnetic circuit will generate significant back EMF

that will generate EMI and may even cause damage to the circuit components. The leak inductance can be calculated as follow:

$$L_{leak} = \frac{K_1 \times L_{mt} \times N_x^2}{100 \times W_1} \times \left(T_{ins} + \frac{b_w}{3}\right) \quad (2.14)$$

Each symbol is defined as follow:

- K_1 is 3 for a simple primary and secondary winding or 0.85 if the secondary winding is interleaved between the primary windings as in Figure 2-19.
- L_{mt} is the mean length around the bobbin for the whole winding (in).
- N_x is the number of turns of the winding being analysed.
- W_1 is the total length of the winding (in).
- T_{ins} is the thickness of the insulating material (in) and
- b_w is the build thickness from the bobbin center to the most outer winding on the completed transformer (in);

It can be clearly seen that the number of turns, the thickness of the isolation material, the build thickness and the length of the magnet wires have a significant influence on the leak inductance. To minimise the leakage inductance, the transformer needs to be wound with high precision and very tight tolerances. In a hard switching converter, it is strongly recommended to keep the leak inductance to a minimum (in contrast to the design of an LLC Transformer) because this kind of power converter does not have the ability to recover energy from the leak inductance.

Another common problem in the design of a high frequency transformer is the inter-winding capacitance. Two adjacent windings have different voltages and the insulation material may create a large capacitance between the windings that can store energy and release it back through the windings. The stored energy is released back into the switches as voltage and current spikes and can be calculated as follow:

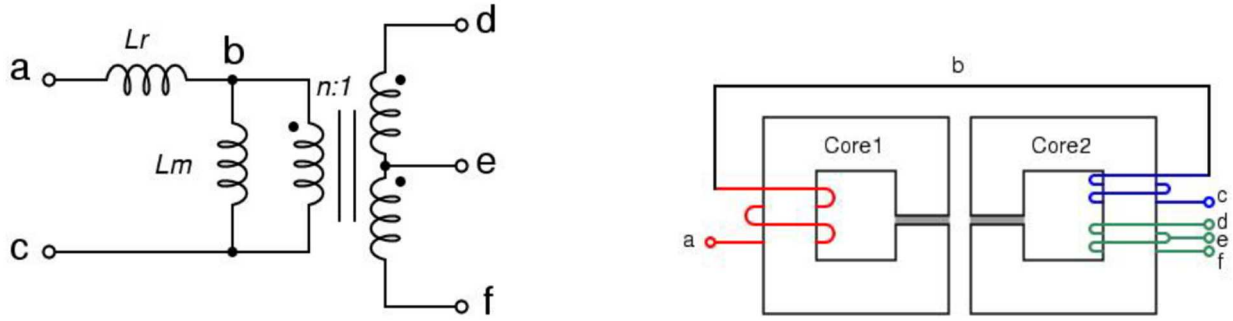
$$E_{stored} = 0.0194 \times \frac{V^2}{Ln\left(2 \times \frac{s}{d}\right)} \quad (2.15)$$

where

- V is the voltage difference between the adjacent windings.
- s is the distance between the windings (m) and
- d is the diameter of the wire (m);

2.1.5.2 LLC Transformer

In the case of the LLC resonant converter, there are two magnetic components involved. They are commonly referred to as the resonant inductance (Lr) and the magnetizing inductance (Lm). Two different approaches can be used to obtain the needed inductance values namely discrete magnetics design and integrated magnetics design. The benefit of using the discrete design is that the design methodology is well established and there are many fully documented design procedures for doing so. Figure 2-20 shows the corresponding schematic as well as the physical structure for the discrete magnetics design. Core 1 represents the resonant inductor whereas Core 2 represents the magnetizing inductor which is part of the transformer.



a) Schematic b) Physical structure

Figure 2-20: Discrete magnetics design [15]

At higher frequencies, core losses the dominating problem in the LLC converter's magnetics design as this kind of converter operates at very high frequencies. It is also preferred that the input voltage be higher when very high efficiency is required for this kind of converter as a lower input voltage will lead to an increase in flux density, however this is not a critical problem. The leakage inductance is the critical design parameter as this determines the resonant inductor's value which determines a major part of the operating point (frequency) of the converter.

The major drawbacks of this kind of design are listed below [48]:

1. Two separate magnetic components and design thereof are required which increases the component count and number of connections.
2. High flux ripple is common in this kind of design which will lead to high magnetic loss.
3. A major drawback is the large footprint needed by the whole structure.

When considering the integrated magnetics design where both magnetic components are integrated within the same physical magnetic structure. The challenge in this design is to accurately control the leakage inductance. In this kind of design, the leakage inductance will exist on both the primary and secondary side of the transformer. It is important to note that the leakage inductance will increase the magnitude of back EMFs, which will require the use a higher voltage secondary rectification devices as this increases the stress on these devices.

In the integrated magnetics structure as shown in Figure 2-21, the magnetic flux density in the centre leg is greatly reduced, which will reduce core losses. It should also be noted that the introduction of the gap across all three legs makes for a mechanically more stable structure. This should also be taken into account as the ferrite core is brittle and might vibrate at its structural resonant frequency which might cause the core to crack or break apart [49].

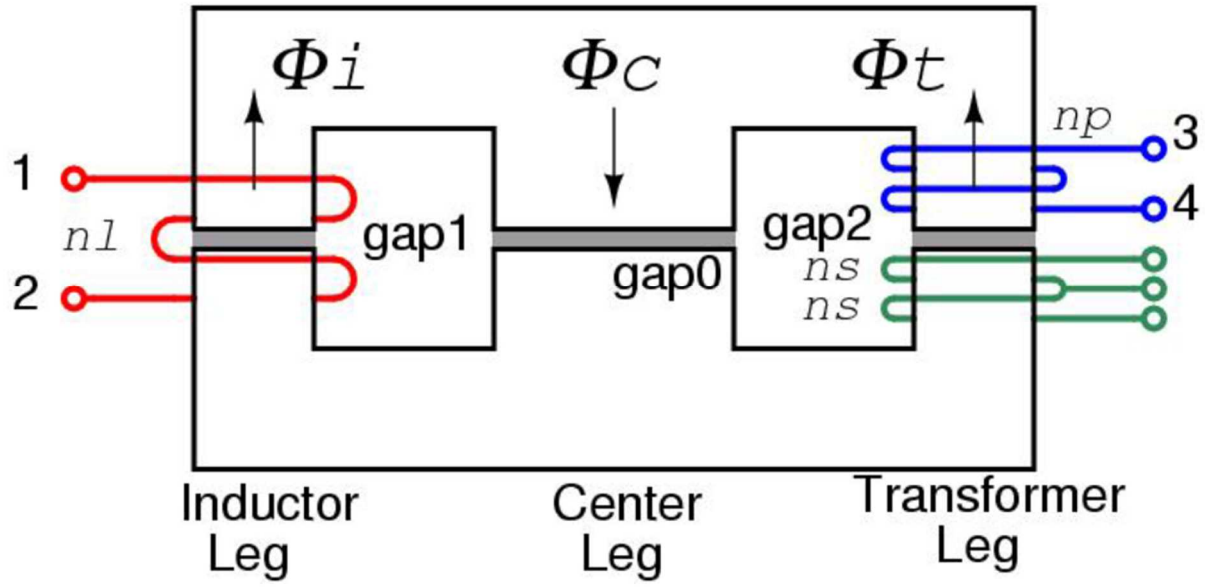


Figure 2-21: Integrated magnetics design structure [16]

The air gap in the core is introduced to obtain the proper magnetizing inductance requirement. Magnetizing current has an influence on the magnetic flux within the core and therefore contributes to core loss due to saturation whereas the resonant current contributes to winding loss [49]. Traditional design methodologies are based on the assumption that there is an infinite permeability of the core and therefore no energy is stored in the core, however this is not an accurate assumption for this converter as the relative permeability of the core is of high importance in this design. It is also generally assumed for traditional hard switched converters that the optimally designed transformer will have a core loss that is equal to the winding losses, which is not true for this kind of converter. Therefore, the appropriate design strategy will be to focus on an optimized core to copper loss ratio, which will not be 1:1 as is the case with hard switched devices.

Furthermore, the introduction of the air gap will also lead to fringing effects which has an impact on the adjacent windings. This will cause heat spots to form in the wiring situated over the air gap. Proximity effects of the wiring also needs investigation due to the high switching frequencies involved in this kind of converter. The LLC transformer design focuses on inductor design based on stored energy rather than the conventional power transfer design.

2.2 Conclusion & Chapter 2 Summary

Different topologies exist for designing power converters. The two main topologies used is the half-bridge and full-bridge topology. When designing a power converter, either one of the two can be used but the efficiency does not only depend on the topology or type of MOSFET that is used. Various different techniques can be applied (hard-switching, phase shifted switching or resonant mode) to the topology in order to increase the efficiency. MOSFETs are preferred because they can operate at high frequencies and have very low losses – however, the soft-switching mode of a MOSFET is very different than the soft-switching mode of a BJT or IGBT. ZVS is the soft switching mode for a MOSFET (voltage controlled device) while ZCS is preferred for BJTs, IGBTs and diodes. Choosing the correct topology, switching technique and switching device is preferred because it can increase the efficiency while also increasing the reliability of the power converter. In this study, two different power converters will be used to compare the effects of hard and soft switching. The LLC resonant converter will be implemented and applied to the full-bridge topology (while using a smaller transformer and a higher switching frequency) and will be compared to a hard-switching converter that has the same output power and voltage capability. Both converters will use the MOSFET as a switching device in order to compare the difference between soft and hard-switching.

CHAPTER 3: DESIGN

In this chapter, a summary of the design procedures, or combinations thereof, as reviewed in the literature review will be discussed in detail for all the critical components that is needed to make the DC/DC converter work in a soft-switching mode. This involves a detailed step by step discussion for the circuit design and calculations, the transformer design, the programming and control strategies as well as other items that is critical to the functioning of the power converter. The reason for the detailed step by step discussion is to ensure repeatability of all implemented systems in order to be able to verify it in simulation and ultimately test and validate through the construction of a physical model.

3.1 The Full-Bridge LLC Resonant Converter

The detailed design process for a highly energy efficient LLC resonant converter is discussed in this section. This includes the design of the resonant tank circuit, power electronics, high frequency gapped ferrite transformer and heatsink requirements. These characteristics will be simulated and verified against the literature. A similar design process will be followed for the hard switching converter.

3.1.1 LLC Resonant Tank Circuit

This section focuses on the design of the resonant tank circuit and aims to explain a generic design procedure that will be followed when designing an LLC resonant converter for any load requirement. This guideline will also focus on the use of parasitic elements, such as transformer leakage inductance, and how to utilize these parasitic elements as part of the design parameters in order to satisfy the requirements for a high efficiency and low EMI power converter.

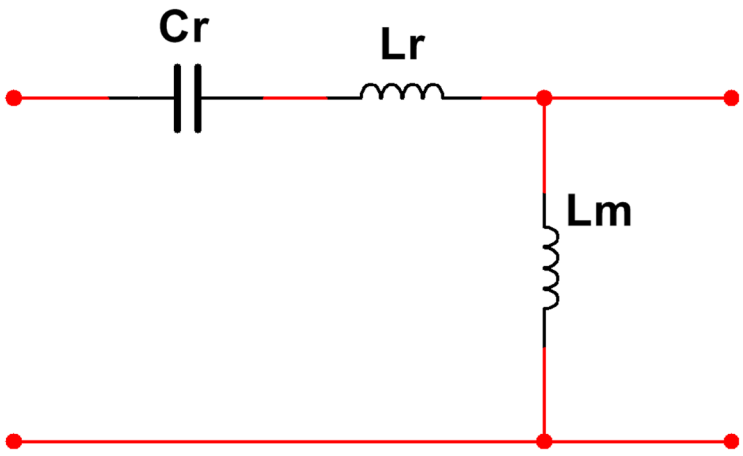


Figure 3-1: LLC tank circuit

In this design procedure, the power converter design will take minimum and maximum input voltage variations into account since the converter will be used in conjunction with solar panels. The design methodology uses the First Harmonic Approximation, also referred to as FHA method, to determine the circuit characteristics [24], [25]. Shown in Figure 3-1 is the circuit components to be designed. The inductances are dependent on the transformer design and can both be integrated to form an integrated magnetics design.

Parasitic inductances will contribute and add up to the leakage inductance, Lr, which is needed in the LLC resonant converter to achieve zero voltage switching across the entire load range. It is the inductance which is normally associated with flybacking – a condition in which the inductance will cause a back EMF due to the stored energy being reflected back to the source instead of being transferred. In a real transformer, the leakage inductance is very difficult to predict because it is highly dependent on the transformer's winding dimensioning. The magnetizing inductance, Lm, is the inductance that is responsible for transferring energy from the transformer's primary side to its secondary side. Finally, the resonant capacitor, Cr, will also serve as a dc blocking capacitor and is needed together with the resonant inductance to determine the circuit's quality factor.

3.1.1.1 Resonant Tank Circuit Design Steps

Step 1: Define the requirements of the LLC resonant converter.

Start the design by defining the input voltage range as follow:

$$Vin_{\max} = 230 \text{ V}$$

$$Vin_{nom} = 170 \text{ V}$$

$$Vin_{\min} = 120 \text{ V}$$

The nominal voltage is the voltage point of the solar panels when operating at their maximum power point. The highest and lowest voltages represent the open-circuit voltage and the minimum input voltage from the solar panels which may be caused by weak solar irradiance.

The next step is to define the full load requirements, with at least 10 % overhead included as a safe margin. This includes the required maximum power level, voltage and current.

$$P_{load} = P_{o\,max} = 1100 \text{ Watt}$$

$$V_{load} = 42 \text{ V}$$

$$I_{load} = \frac{P_{load}}{V_{load}}$$

When calculating the transformer turns ratio, it is important to define whether the circuit will use a half-bridge or full-bridge design. In the case where a half-bridge design is preferred, the transformer turns ratio is calculated as follow:

$$n = \frac{Vin_{nom}}{2 \times V_{load} + 2 \times 0.6} \tag{3.1}$$

In the case where a full-bridge design is preferred, the equation becomes

$$n = \frac{Vin_{nom}}{V_{load} + 2 \times 0.6} \tag{3.2}$$

This equation also takes into account the effects of using a half-bridge, which is that the input voltage supplied to the transformer will be half that of a full bridge, but the current will be twice as high. It also takes the effect of rectifying diodes at the output side into account as they may have a voltage drop of approximately 0.6 V each. In the case of full-wave rectification, the voltage drop is 2 × 0.6 V and for a centre-tap output transformer it is only 0.6 V. It is not critical to take this into account, but aids in good design practice.

For synchronous rectification (where MOSFETs are used), this may be omitted. The calculated value for the transformer n-ratio may also be rounded to the nearest realistic value. It is preferred to round the value up to the closest but higher value instead of a lower value.

Step 2: Calculate the required gain parameters of the power converter based on the parameters in step 1.

In the case of an LLC resonant converter, the converter operating frequency determines the amount of voltage boost or bucking (step-down) at the input side of the transformer without the need of an additional buck or boost converter or PWM control. This is referred to as the converter gain and is denoted as M.

$$M_{nom} = 1$$

$$M_{max} = M_{nom} \times \left(\frac{Vin_{nom}}{Vin_{min}}\right) \tag{3.3}$$

$$M_{min} = M_{nom} \times \left(\frac{Vin_{nom}}{Vin_{max}}\right) \tag{3.4}$$

The equations represent the nominal or normalised gain, which is 1 for a specified transformer turns ratio. It can be better understood when looking at the following equation:

$$\frac{N_p}{N_s} = \frac{Vin_{nom}}{V_{out}} \times Mnom \tag{3.5}$$

Where

$$\frac{N_p}{N_s} = \frac{Vin_{nom}}{V_{out}} \tag{3.6}$$

This results in $M_{nom} = 1$

M_{max} is the resonant tank's required maximum gain and M_{min} the minimum gain required for the resonant tank. This is used later on to verify that the design is feasible and can achieve the required gains.

Step 3: Select the maximum allowed quality factor at full load operation.

For the LLC resonant converter, it is very important to keep in mind that the quality factor is not a constant value. It changes as the load and input voltage and load changes. A high quality factor will result in a wide switching frequency modulation requirement, but will have a low converter gain capability. A lower quality factor will result in a narrower converter gain curve but will result in a smaller frequency modulation range. The optimal starting point for the quality factor is 0.4 as can be seen in various application notes. This is a value that is chosen. Because the design procedure is an iterative process, the selection of this parameter can be observed when the gain curve is plotted and can then be adjusted accordingly. An increase in load will result in a higher quality factor whereas a lower quality factor will be observed at lighter load conditions. For other switching converters, this behaviour will be exactly the opposite. Quality factor has a direct impact on load regulation when the input voltage drops. It will be easier to maintain regulation at the output with a properly selected quality factor as this directly affect the converter's gain capabilities but frequency modulation range will also be increased.

The maximum quality factor (Q_{max}) is expressed as

$$Q_{max} = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac,min}} \tag{3.7}$$

Where Lr is the resonant inductance. In the LLC resonant converter, Lr is the sum of all parasitic inductances in the resonant tank path. This includes the transformer primary side leakage inductance, the secondary side leakage inductance that is reflected back to the primary side as well as the PCB trace inductance. A transformer may be designed to have a low leakage inductance since it is difficult to predict the value of the leakage inductance.

An external inductor may be added if additional inductance is required. At this stage, this values for Lr and Cr, the resonant capacitor, is still unknown and will be calculated later using the defined quality factor.

Rac, min is the value of the load at the secondary side that gets reflected back to the primary side. It is therefore the equivalent AC resistance as seen from the primary side during full load operation. It can be expressed as follows:

$$R_{ac}, \min = \frac{8}{\pi^2} \times \frac{N_p^2}{N_s^2} \times \frac{V_0^2}{P_{o\,max}} \tag{3.8}$$

It should now become apparent why it is important to define the quality factor of the circuit as it will be used to calculate the resonant tank parameters required to meet the design specifications up to the full load requirement.

Step 4: Selecting the resonant inductance ratio.

The quality factor is not the only parameter that needs adjustment. It is more important to rely on the inductance factor, denoted as m. for achieving the gain requirements. To understand the trade-offs involved in the inductance factor ratio, consider the following conditions.

Selecting a lower inductance factor results in:

- Higher boost gain
- Narrower frequency modulation range
- Better regulation flexibilities

A higher inductance factor will result in:

- Higher magnetizing inductance
- Lower magnetizing inductance currents
- Higher converter efficiencies

Because an electrolyser does not require such a dynamic power supply and because high efficiency is required, it is preferred to choose a high inductance factor. A good starting value would be to choose the magnetizing inductance to be approximately six times higher than the leakage inductance [9]. In a hard switched converter, it is preferred to have a high magnetizing inductance and a very low leakage inductance. This results in a magnetizing inductance many times larger than the leakage inductance and a low switching frequency.

The ratio of total primary to resonant inductance can be expressed as:

$$m = \frac{L_r + L_m}{L_r} \tag{3.9}$$

Where Lr is the leakage or resonant inductance and Lm is the magnetizing inductance of the transformer.

Step 5: Choose a desired switching frequency.

A higher switching frequency, f_s, will result in smaller magnetics components but may increase the complexity of the switching circuitry, controller programming and magnetics design.

Step 6: Finding the minimum required normalised switching frequency.

The gain equation for an LLC resonant converter, when using the FHA method is given as:

$$K(Q, m, f_n) = \left|\frac{V_{o_{ac}}(S)}{V_{in_{ac}}(S)}\right| = \frac{f_n^2(m-1)}{\sqrt{[(m \times f_n^2 - 1)^2 + f_n^2(f_n^2-1)^2 \times (m-1)^2 \times Q^2]}} \quad (3.10)$$

Substitute the values of Q and m into the equation above and then rewrite the equation. Then, find the derivative of the function to obtain the point on the gain curve where the slope is equal to zero. This point will be the maximum gain point and must be solved for f_n to obtain the switching frequency where the gain will reach a maximum.

$$\frac{d}{dF_n} K\left(Q, m, f_{n_{\min}}\right) \big| \, (Qmax = 0.4, m = 6) = 0 \quad (3.11)$$

This value will represent the normalised switching frequency and must be multiplied by the switching frequency, f_s, that has been chosen in step 5 to find the actual switching frequency in Hertz. When solving the equation using a simulation package such as MATLAB®, multiple values may be found. The correct value will be the solution that yields only a real, non-complex, positive number.

Step 7: Verify that the selected Q and m values can reach the desired gains.

This step only verifies the design feasibility and can be either calculated or plotted in a graph using a for-loop or both.

To calculate the maximum gain point, use the gain equation and calculate the maximum gain as follow:

$$K_{\max} = K\left(Q_{\max}, m, f_{n_{\min}}\right) \quad (3.12)$$

Note that this maximum gain is not the maximum attainable gain. It is an indication of the maximum required gain for the load at a specific input voltage. This value should be greater than the two values calculated in step 1.

Step 8: Calculate the resonant tank component values

Use the values in steps 1 to 3 to calculate the reflected AC resistance, R_{ac}, and use this value together with the selected maximum quality factor value. Substitute these values into the Qmax equation in step 3 as follow.

The equation should be solved with the selected $Qmax = 0.4$, and $R_{ac} = 20.13$ value, but with Lr and Cr still left in symbolic form as follow:

$$Q_{max} = 0.4 = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac} = 20.13} \tag{3.13}$$

Then the resonant frequency should be written in terms of the resonant frequency for an LC circuit and also be left in terms of symbols as follow:

$$f_r = 80\ kHz = \frac{1}{2\pi\sqrt{(L_r \times C_r)}} \tag{3.14}$$

Finally, the inductance ratio can be expressed in terms of component values as follow:

$$m = 9 = \frac{L_r + L_m}{L_r} \tag{3.15}$$

To obtain the resonant tank components, the three equations can be rewritten in a linear algebra form and entered into a matrix which must then be solved to row reduced echelon form to obtain the values for Lr, Lm and Cr.

In the case where the calculated resonant capacitor value is unrealistic or not easily obtainable, the design parameters may be adjusted or the whole process as outlined here may be reversed to determine the Q_{max} and m value for a selected capacitor, leakage inductance or magnetizing inductance.

3.1.1.2 Summarizing The Resonant Tank Design Process

The design process has been simplified in Figure 3-2 which shows a flow chart that can be followed to design the LLC resonant tank circuit. It also indicates which parameters must be adjusted when the desired converter gains cannot be achieved. Caution should also be taken when choosing a desired resonant frequency as the actual switching frequency at the maximum gain point may fall below this value. If this is the case, one can also adjust the inductance factor, m, or increase the required resonant frequency. Increasing the resonant frequency will shrink the magnetics involved in the design, but will lead to a more complicated magnetics design. Once all the design specifications have been met, the resonant tank components can be calculated.

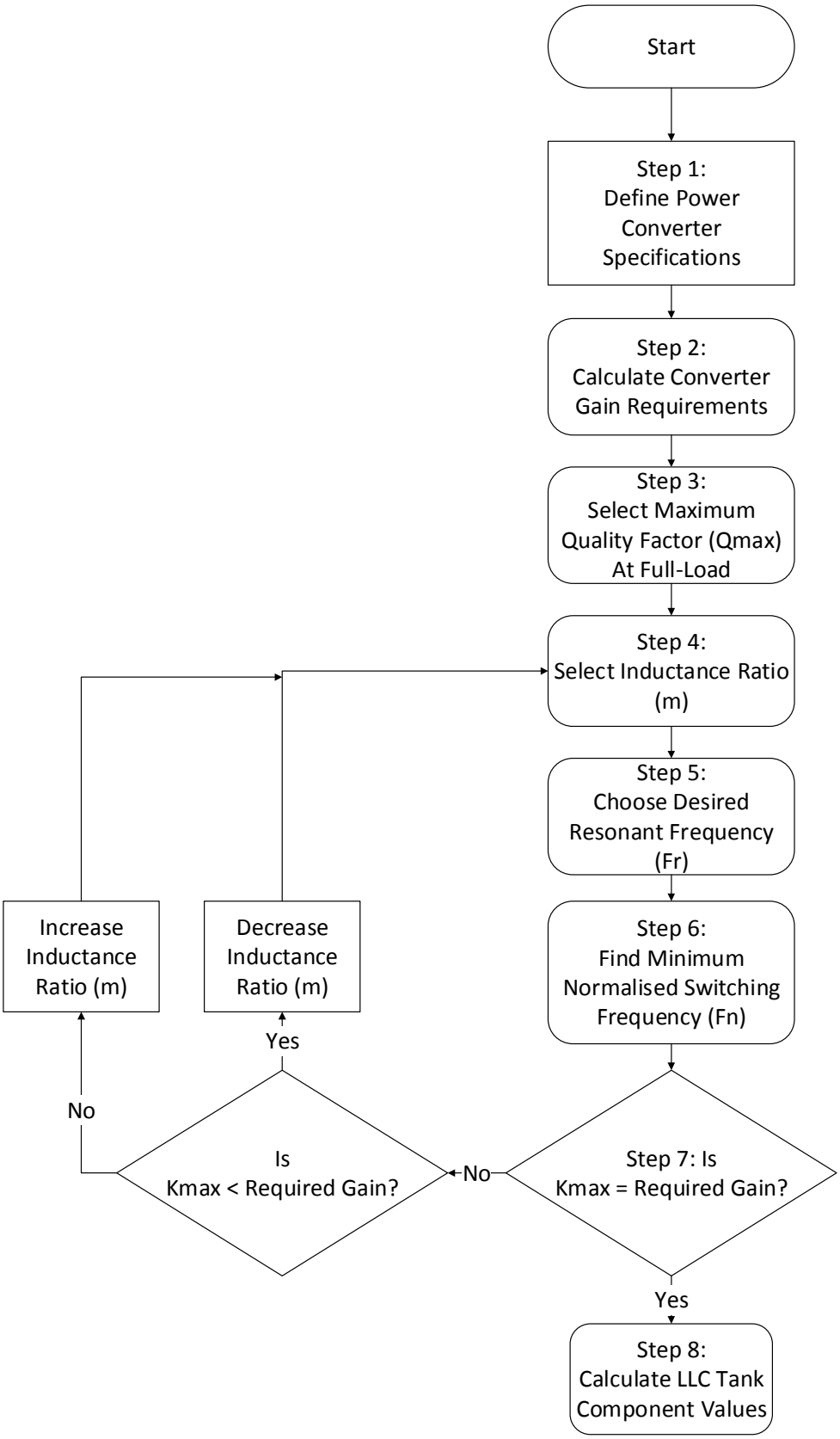


Figure 3-2: LLC tank design flow chart

3.1.2 MOSFET Gate Drive Circuit

The gate drive circuitry interface a low voltage microcontroller to a high voltage source like a solar panel in order to control the MOSFETs used in the power converter while providing an electrical isolation barrier. In the event of a MOSFET failure, the gate drive circuit should be able to prevent any transient pulses from damaging the gate drive electronics or microcontroller attached to its input. It should also focus on a fail-safe design so that when it is impossible to prevent transient voltage spikes, the circuit should rather clamp the pulses down by converting them to heat or by relaying them away from sensitive devices. In systems where hydrogen is being generated and stored, it is critical to maintain safety and isolation to prevent damage to any computer systems connected to the power converter by means of its USB port. This section will therefore discuss the design of such a gate drive circuit that is suitable for both hard and soft switching applications where PWM signals are generated by a digital controller.

Some component values used in the actual circuit may differ slightly from what is shown in Figure 3-3 and Figure 3-4 due to the reason that the software used to draw the circuit diagram may not have the exact same part number from the same manufacturer in its database. Instead, the closest match have been chosen and used in the shown schematic. The microcontroller is modelled using pulsed sources, shown as V1 in Figure 3-3 (section of the gate driver circuit from Figure 3-4) on the next page and V2 in Figure 3-4 (the complete circuit) that mimics the PWM signals. To calculate the values for the biasing resistors R1 and R2, the forward biasing voltage and current value can be found in the gate driver, SiLabs Si8261, datasheet.

This is calculated as $R = \frac{V_{mcu} - V_f}{I_f}$ where V_{mcu} is the microcontroller voltage, V_f is the forward voltage drop of the LED emulator in the gate driver and I_f is the required biasing current that can be found in the datasheet. The required value to meet this need is not critical and was calculated as 110 Ω. A transient voltage supressing diode (TVS) can be added in parallel with the gate driver that will clamp the voltage down to a safe level (3.6 V) for the microcontroller. On the gate driver output side, pulse steering diodes (D2, D3, D11 and D12) were added in parallel with the totem pole MOSFETs inside the gate driver. This helps to protect the gate driver against transient voltage spikes that may cause failure or latch-ups in the totem pole MOSFETs. The diodes can be any type of diode that has a fast recovery time and a blocking voltage of at least 50 volts. Figure 3-3 shows a section of the gate driver circuit that interfaces to the microcontroller. This is just a section of the circuit shown later in Figure 3-4, which shows how the rest of the gate driver circuit connects to an actual MOSFET.

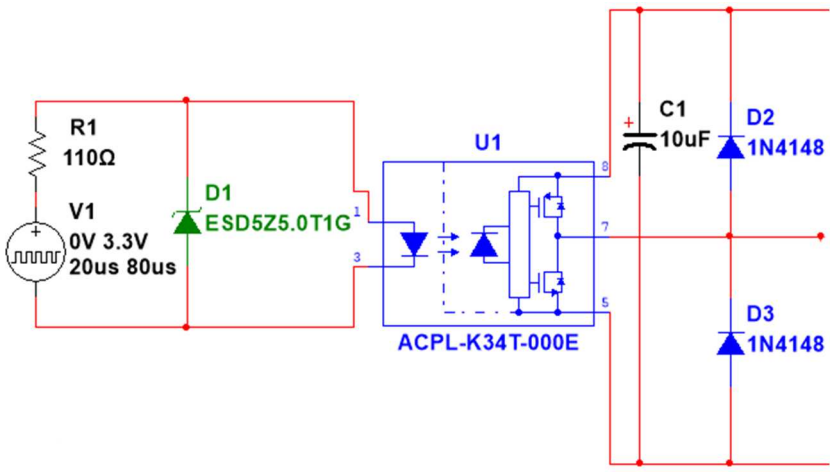


Figure 3-3: Gate driver circuit

This gate drive circuit requires that the high side gate driver's capacitors be fully charged before it is operational. To do this, a bootstrapping diode is added to the high side driver because the high side driver's ground is not at the same voltage level as the low side driver. Mixed capacitors, in terms of size and type, are used to minimise the Equivalent Series Resistance (ESR) of the capacitors as a high ESR may hinder the capacitor's ability to filter voltage ripple and spikes. There is no maximum allowed capacitance value, but the time to charge the high side capacitor array can be calculated as follow:

$$V_c = VccDrv\left(1 - e^{\frac{-\frac{t}{2}}{R \times C}}\right) \tag{3.16}$$

Each symbol represents the following:

- $VccDrv$ is the low side gate driver supply voltage.
- R is the low side MOSFET's maximum Rds_{ON} as found in its datasheet.
- t is the capacitor charge time required (take into account a 50 % duty cycle).
- C is the value of the total capacitance and
- V_c is the final voltage level of the capacitors and should be 99 % of $VccDrv$;

By re-arranging the equations, it was found that the minimum time required to charge a 22.1 µF capacitor is 2 µs. The gate driver datasheet states that it requires up to 30 µs to start-up after initial power-on. To be safe, the microcontroller will allow an initial bootstrapping time of at least 1 ms for compatibility with different gate drivers. A zener diode or TVS diode can be added in parallel with the bypass capacitor to clamp the voltage down to a level that is safe for the gate driver as it will prevent overcharging of the bypass capacitor. In this case, an 18 V zener diode (D6 and D7) was used as its value is lower than the driver's allowed value of 30 V, but higher than the supply voltage of 12 V.

The gate driver uses a separate resistor-diode combination for improved turn-off propagation delay. Using resistors also supresses ringing due to parasitic inductances caused by the PCB traces. Caution should be taken when selecting a gate drive resistor as this is highly dependent on the kind of power converter. Choosing a value that is too low for a hard switching converter may lead to a latch-up. Choosing a value that is too high will increase switching losses and increase the risk of cross-conduction or dv/dt shoot-through. This is discussed in section 2.1.2.3.

The turn-on resistor value for a IXTH48N65X2 MOSFET used with a Si8261BBC-IP gate driver, is calculated as follow:

$$IG_{Src_{Spike}} = \frac{Vg_{ON} - Vg_{OFF}}{Rg_{MOSFET} + Rg_{DRIVER_{ROH}} + Rg_{Ext}} \tag{3.17}$$

The external resistor to add should be chosen so that the driver's maximum source current value is not exceeded at the desired operating temperature. This information can be found by carefully studying the Safe Operating Area (SOA) graphs in the gate driver's datasheet.

Each symbol used in the equation represents the following:

- $IG_{Src_{Spike}}$ is the maximum driver source current.
- Vg_{ON} is the required MOSFET turn-on voltage, equivalent to the driver supply voltage.
- Vg_{OFF} is the required MOSFET turn-off voltage which is zero.
- Rg_{MOSFET} is the MOSFET's parasitic internal gate resistance.
- $Rg_{DRIVER_{ROH}}$ is the driver's totem pole resistance and
- Rg_{Ext} is the externally added resistor value;

By rearranging the equation, the smallest allowable value can be obtained for the turn-on resistor. A value of 2.2Ω was used to limit the current spike to 2A. The value for the turn-off resistor can be calculated similarly. Furthermore, the driver's allowed power dissipation level can be calculated as follow:

$$P_d = V_f \times I_f \times D_C + V_{dd} \times \left(I_{ddq} + (Q_d + C_l \times V_{dd}) \times f\right) \tag{3.18}$$

and

$$C_l = \frac{Q_g}{V_{dd}} \tag{3.19}$$

Where each symbol used corresponds to the following:

- P_d is the driver's internal power dissipation.
- V_f is the LED emulator's forward voltage drop.
- I_f is the LED emulator's input current.

- D_C is the maximum duty cycle which is 50%.
- V_{dd} is the gate driver supply voltage which is 12V in this case.
- I_{ddq} is the driver bias current and can be found in the datasheet.
- Q_d is the driver's totem pole charge given in the datasheet.
- C_l is the MOSFET's total gate charge and
- f is the resonant switching frequency of 80-kHz;

The calculated value for the power dissipation was found to be 0.14W per gate driver. To ensure reliability, an exaggerated ambient operating temperature of $Tamb = 80\,°C$ was chosen to calculate the driver's maximum allowed power dissipation at this temperature as follow:

$$PdMax = \frac{Tjmax - Tamb}{Tja} \tag{3.20}$$

Where $PdMax$ is the maximum allowed power dissipation at the chosen ambient temperature of 80°C. $Tjmax$ is the maximum junction temperature (140 °C) and Tja is the package junction-to-air thermal resistance (110 °C/W). The maximum safe limit for the power dissipation per driver was found to be 0.55W. Each driver dissipates only 0.14W which is well within safe limits.

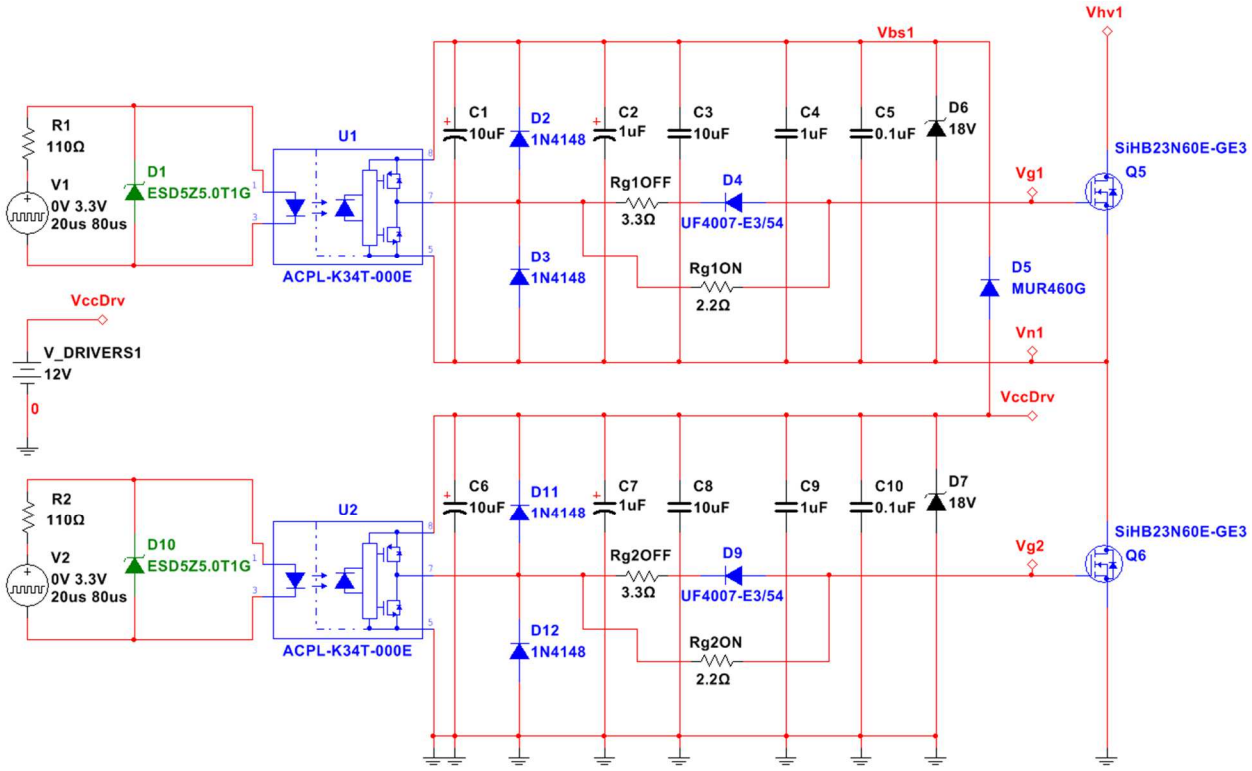


Figure 3-4: Gate drive circuit

Figure 3-4 indicates how the gate driver circuit is connected to the MOSFETs contained in the full-bridge switching section. Vhv1 is the drain of the upper MOSFET and is connected to the high voltage DC bus. The complete switching bridge circuit is shown in Figure 3-5.

Other symbols used in Figure 3-3 and Figure 3-4 are defined as follow:

- Vbs1 which is the high-side bootstrapping voltage and should be the same as the low side driver supply voltage of $VccDrv = 12\text{V}$.
- Vg1 will go to the high side MOSFET gate.
- Vg2 will go to the low side MOSFET gate and
- Vn1 is the high side MOSFET source which is also the high side driver circuit's ground;

Figure 3-4 and its discussion above is the complete representation of an electrically isolated gate-drive circuit suitable for both hard and soft switching applications in a half-bridge configuration using a bootstrapped high-side driver. In a full-bridge application, the circuit in Figure 3-4 can just be duplicated. The design of the switching section to which this circuit connects is discussed in the next section.

3.1.3 The High-Voltage Switching Circuit

The switching bridge circuit contains the high-voltage MOSFETs that receives a low voltage square wave signal from the gate driver which is then amplified to a high voltage square wave. This high-voltage square wave is then fed to the LLC resonant tank circuit that consists of a capacitor, transformer and inductor. The high voltage switching section consist of two half-bridge configurations that forms a full bridge of which the design will be discussed in this section.

Designing a Switched Mode Power Supply (SMPS) starts with defining the bulk or holdup capacitor size. This is the capacitor that filters out the voltage ripple on the high-voltage line and is referred to as a holdup-capacitor because the power supply needs to be able to regulate or maintain a constant output voltage during the time the input voltage drops to its lowest value. During this time, the bulk or holdup capacitor must be correctly sized in order to provide a stable voltage to the power supply so it can maintain proper operation. The optimal holdup capacitor size can then be calculated as follow:

$$C_{bulk} = 2 \times \frac{P_{out}\left(\frac{1}{4 \times f_{line}} + \sin^{-1}\frac{\left(\frac{V_{min}}{V_{peak}}\right)}{2 \times \pi \times f_{line}}\right)}{\eta\left(V_{peak}^2 - V_{\min}^2\right)} \tag{3.21}$$

Each symbol is defined as follow:

- f_{line} is the line frequency before rectification, which is 50 Hz.
- V_{min} the minimum voltage the converter requires to maintain regulation.
- V_{peak} is equal to $V_{min} \times \sqrt{2}$ where $\sqrt{2}$ is the crest factor for a sine wave.
- η is the targeted efficiency of 90 % and
- P_{out} is the maximum output power capability;

From this calculation, it was found that the minimum bulk capacitor required is 1200 µF. Multiple small value capacitors can be added in parallel to minimise the ESR, but the minimum value for a parallel combination should be at least 1200 µF. To obtain the closes value to 1200 µF, a 1000 µF capacitor (C15) was placed in parallel with a series combination of two 470 µF (C11 + C12) capacitors. It is recommended to use electrolytic capacitors in parallel with polymer capacitors because polymer capacitors provide a very low ESR and have a high ripple current handling capability. It will thus be an excellent candidate for filtering out high frequency noise and ripple over the electrolytic capacitors caused by the switching currents of the MOSFETs. The value of the polymer capacitors can be calculated in the same way as the big bulk capacitor, except that it is targeted at filtering out high frequency ripple and transient spikes. Therefore, the frequency to use in the equation should be 80-kHz (as this is the resonant frequency of the designed LLC

tank). The calculated polymer capacitor value is 0.723 µF. A standard value of 1 µF will be used instead because polymer capacitors are not very expensive.

As seen in Figure 3-5, the design makes use of a split-capacitor design, C11 and C12, to allow each half-bridge to be used or tested independently of the full-bridge. The bleeding resistors R7, R8 and R9 is there to allow the high-voltage capacitors to discharge over a long time for safety purposes. Adding a TVS diode or MOV to suppress transient voltage spikes are also recommended. These components are labelled D20, D21 and D22 in Figure 3-5.

Furthermore it is recommended to add a gate to source resistor to each MOSFET to prevent the MOSFETs from accidently switching on when power is applied the first time [50]. The value of this resistor (R3, R4, R5 and R6) is not critical and can vary between 10 to 100 kΩ as recommended in many application notes. Another TVS diode (D13, D15, D17 and D19) can be added to each MOSFET's gate-source to further protect it from transient spikes that may harm or trigger the MOSFET. The value of the TVS diode's clamping voltage should be higher than the voltage supplied by the driver, but lower than the MOSFET's maximum gate-source voltage. Diodes D8, D14, D16 and D18 is used as anti-parallel diodes and are used to relay kickback voltages generated by inductances away from the MOSFET. To conclude this section, the DC supply is connected between the Vhv1 and ground terminal.

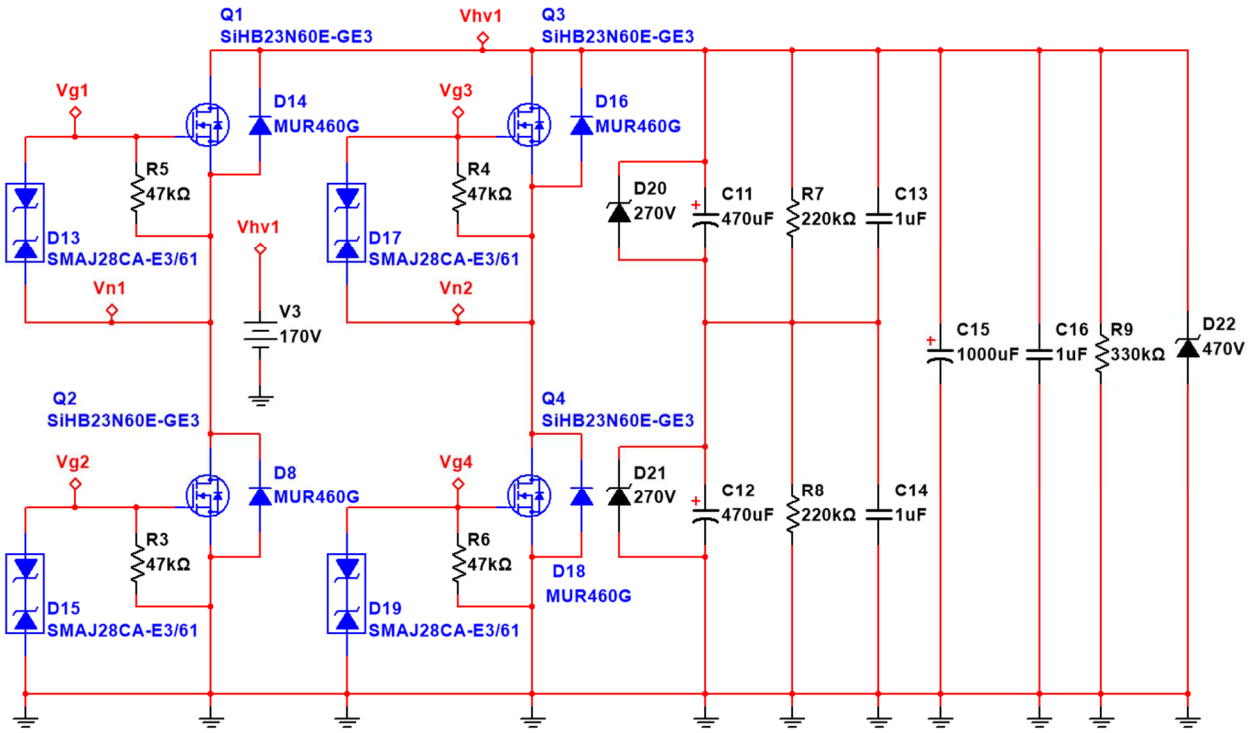


Figure 3-5: Full-Bridge switching circuit

3.1.4 Rectification Circuit

The rectification circuit converts the high frequency AC coming from the transformer back into DC by using fast recovery diodes and low ESR capacitors. Nodes Vn1 and Vn2 shown in Figure 3-6 represents the LLC resonant circuit that connects to the corresponding nodes in Figure 3-5.

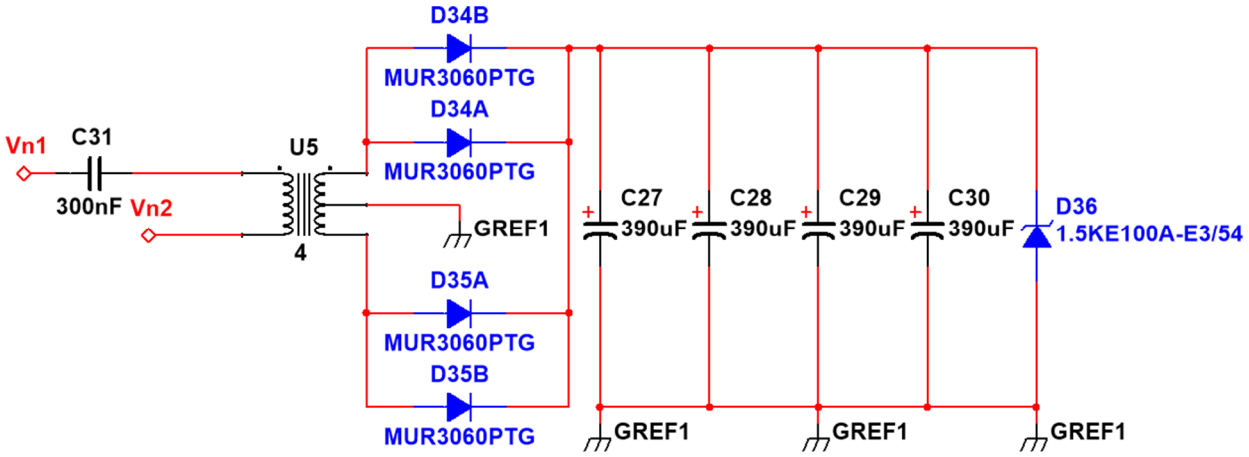


Figure 3-6: Rectification circuit

Capacitor C31 is the resonant capacitor connected in series with the transformer. Diodes D34 and D35 is the rectifier diodes and should be ultrafast recovery diodes (Schottky diodes) because they have a low forward voltage drop and consequently a low power dissipation and high efficiency. Multiple Schottky diodes can be used in parallel to lower the forward voltage drop while simultaneously increasing the current capability even further.

The minimum capacitance value required on the output side can be calculated as follow:

$$C_{filter} = 2 \times \frac{P_{out}\left(\frac{1}{4 \times f_s} + \sin^{-1}\frac{\left(\frac{V_{rms}}{V_{max}}\right)}{2 \times \pi \times f_s}\right)}{(V_{max}^2 - V_{\mathrm{rms}}^2)} \quad (3.22)$$

Each symbol is defined as follow:

- f_s is the lowest possible switching frequency (30-kHz from Figure 4-2).
- V_{rms} is the electrolyser voltage required.
- V_{max} is equal to V_{min} + preferred ripple (0.5 V) and
- P_{out} is the load power requirement;

From the information above, the minimum required capacitance is 870 µF. A parallel combination of 4 × 390 µF low ESR capacitors capable of 100V have been used in parallel with a TVS diode of the same voltage rating to suppress transient spikes that may cause capacitor degradation.

3.1.5 High Frequency Ferrite Transformer

Successful operation of the LLC resonant converter is highly dependent on the value of each component that makes up the resonant tank circuit. This includes the transformer leak inductance, magnetizing inductance, resonant capacitor and output capacitance of the MOSFETs as well as the kind of topology (Half or Full-Bridge) it is used in. Switching frequency and dead-time is critical for ensuring perfect ZVS operation while also avoiding transformer core saturation. This section will therefore focus on the design of the high frequency transformer and the necessary calculations to obtain the desired inductances while avoiding saturation of the core.

The design process is an iterative process that starts at the design of the resonant tank circuit as discussed in section 3.1.1. Higher switching frequencies results in a higher power density, allowing a smaller transformer size as an advantage. It can also complicate the design of the switching electronics, require a higher timer resolution in the controller and may have higher losses due to the skin-effect which will be discussed in this section. An EE55 ferrite transformer, as shown in Figure 3-7, using N87 ferrite material was chosen using an iterative process. It should be kept in mind that the kind of ferrite, N87 in this case, in conjunction with the core size is what determines the saturation point and temperature stability. Data on temperature stability as well as core losses at a certain frequency can be obtained using the TDK® Ferrite Magnetic Design Tool®.

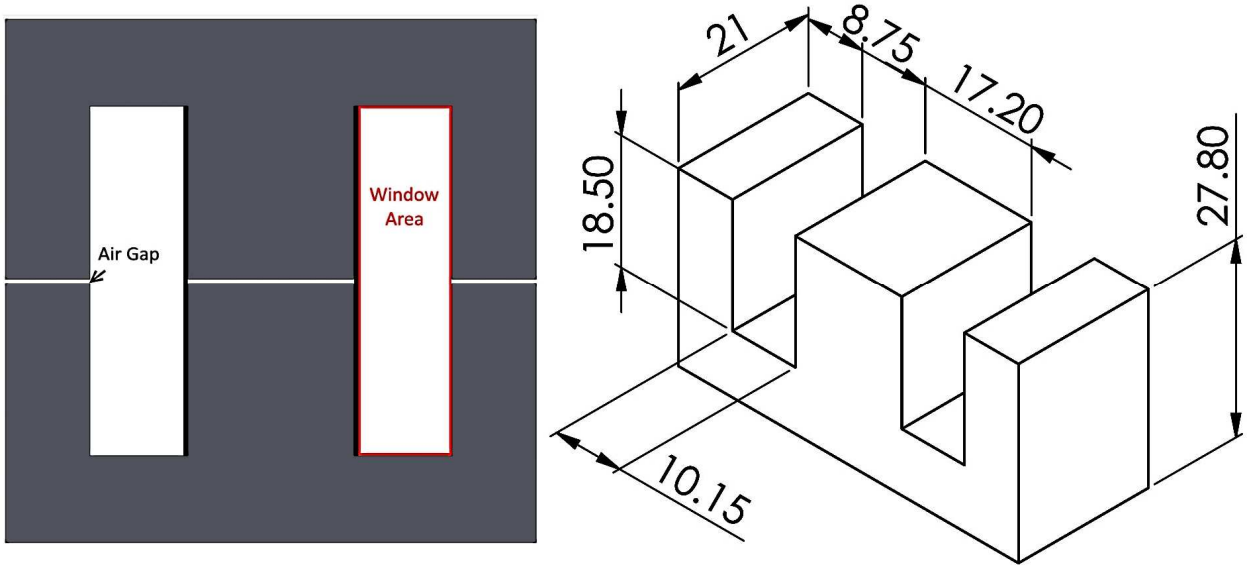


Figure 3-7: EE55 ferrite transformer (N87)

After choosing the transformer size, it is required to calculate the new relative permeability by using the relative permeability for the ferrite material (N87) as shown in the datasheet. By choosing an air gap smaller than 1 mm the relative permeability can be calculated as follow:

$$\mu_{eff} = \frac{1}{\frac{2 \times g}{l_c} + \frac{1}{\mu_r}} \tag{3.23}$$

Where each parameter is defined as follow:

- μ_{eff} is the new relative permeability.
- g is the chosen air gap size in mm.
- l_c is the magnetic path length as given in the datasheet (without the air gap) and
- μ_r is the relative permeability of the ferrite material as obtained from the datasheet;

Then, it is required to calculate the transformer A_L value. The A_L value for a given inductor or transformer defines the relationship between the inductance and number of turns squared. This is influenced by the air gap, which is why a new relative permeability is calculated. An A_L relationship for the core can be calculated as follow:

$$A_L = \frac{\mu_0 \times \mu_r \times A_c}{2 \times g \times \mu_r + l_c} \tag{3.24}$$

Where $\mu_0 = 4 \times \pi \times 10^{-7}$ is the permeability of air and A_c is the total cross-sectional area of the core, for both halves of ferrite.

The number of primary turns can be calculated as follow using the required inductance value as calculated in section 3.1.1: $N_p = \sqrt{\frac{L_m}{A_L}}$

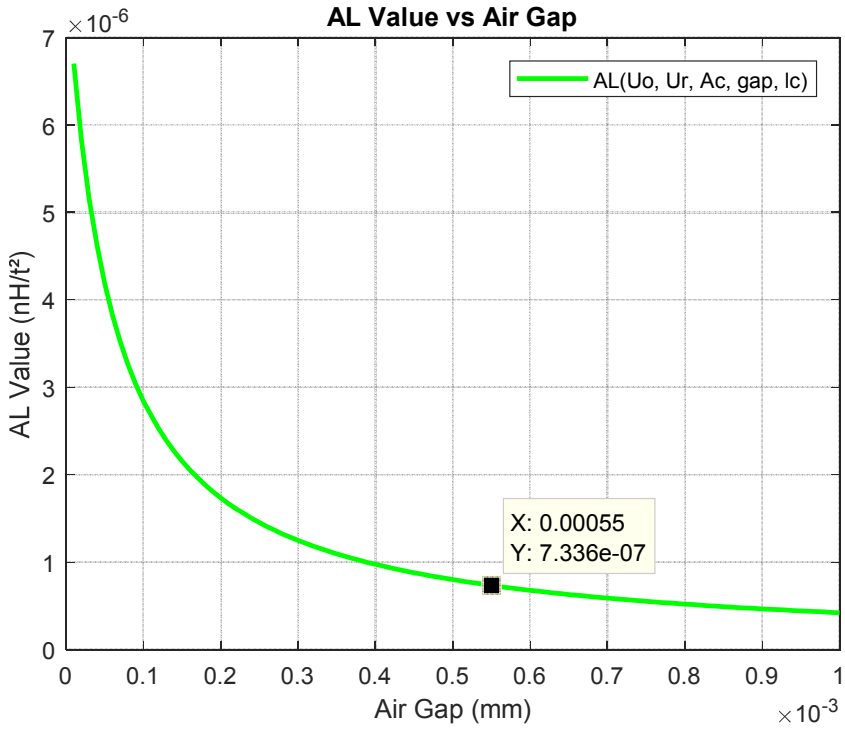


Figure 3-8: AL value vs air gap

The effect of air-gap on the A_L value is shown in Figure 3-8. This was calculated for the transformer core shown in Figure 3-7 using an air gap of 0.55 mm.

It is clear from Figure 3-8 that the smaller the Air-gap, the more difficult it becomes to achieve a desired inductance as the effect of air gap on inductance is exponential. The number of turns on the transformer secondary side can now be calculated as follow:

$$N_s = \frac{N_p}{a}$$

Where a is the transformer turns-ratio and N_p is the number of turns at the primary side.

Furthermore it is required to verify that the core will not saturate for the calculated number of turns as well as the chosen air-gap size. The air-gap can never saturate due to the low permeability of air, but the ferrite material is prone to saturation. Verifying the previous number of turns can be done as follow:

$$Np_{\min} = \frac{a * V_{load}}{2 * fs_{min} * A_c * B_{max}} \tag{3.25}$$

Where Np_{min} is the minimum number of turns required at the lowest operating frequency of Fs_{min} in order to avoid exceeding the maximum flux density of B_{max} as defined in the core datasheet. If the minimum number of turns as calculated here is not lower than previously calculated, then the air-gap must be adjusted (to no bigger than 1mm to avoid fringing), a bigger core must be selected or a core made out of different material must be selected. The core-utilization can be calculated by calculating the amount of flux-swing. This may give an indication as to how far the core will saturate under the given conditions and can be calculated as follow:

$$\Delta_B = \frac{a * Vload}{Np * 2 * fs_{min} * Ac} \tag{3.26}$$

The delta value (in Tesla) is the total flux swing in both directions, not the maximum flux as given in the datasheet. A magnetization curve for a given core can be obtained using the TDK® Ferrite Magnetic Design Tool®. Half of this value should not exceed the maximum value as specified in the datasheet at a given operating temperature. Using the TDK® Ferrite Magnetic Design Tool®, the core losses can also be calculated.

When the transformer has been optimised, the wire gauge can also be optimized to avoid losses due to the skin effect. The skin effect is the tendency of high-frequency alternating current to flow at a higher density at the outer layer of the conductor instead of being equally distributed throughout the conductor. Skin depth is the point where the current density reaches 37% of its value at the surface of the conductor. If the frequency is increased further, the skin depth where current will flow on the surface will become smaller to the point where the AC resistance of the wire increases too much and results in high power losses. To avoid this, Litz wire can be made out of multiple thinner strands of enamelled wire twisted together to form a single strand of thick wire.

Skin depth is calculated as follow:

$$\delta = \sqrt{\frac{\rho}{\pi \times f_0 \times \mu_r \times \mu_0}} \tag{3.27}$$

Where $\rho = 1.678 \times 10^8$ Ω.m is the resistivity of copper and f_0 is the resonant switching frequency. To better understand the effect of skin depth, the effect of skin depth vs frequency for copper has been plotted in Figure 3-9. It becomes apparent that at higher frequencies the AC resistance increases.

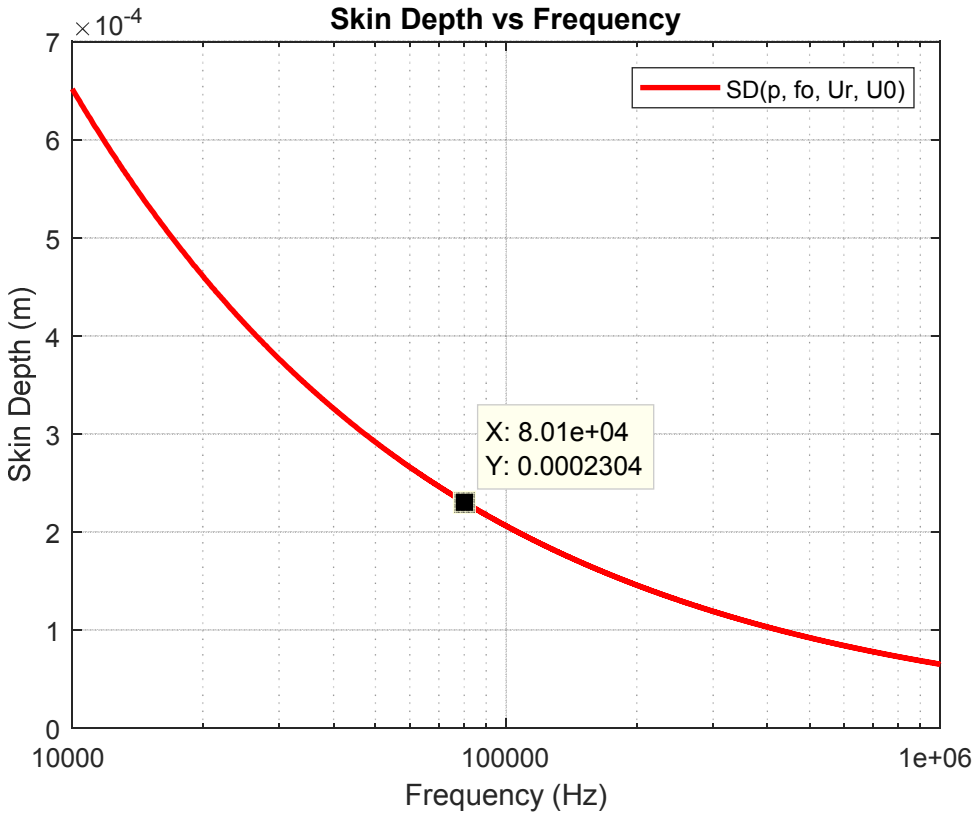


Figure 3-9: Skin depth vs frequency

At a resonant frequency of 80-kHz, the skin depth will be 0.23 mm. It is recommended to use the resonant frequency of the LLC resonant converter for calculating skin depth as this is the highest frequency the converter will operate at during light-load conditions when less current will be flowing through the core windings. This is also dependent on the type of application and therefore the gain curve of the LLC resonant converter can also be beneficial for determining the optimal switching frequency for the given load and then calculate the skin depth from that value.

To optimize the Litz wire design for the LLC resonant converter, 15 strands of 0.25 mm diameter enamelled wire has been chosen for the Litz wire design. It is also important to take into consideration the transformer windowing area, as shown in Figure 3-7 to make sure that the wire thickness (and thickness of the insulation material) and number of turns will fit easily into the

windowing area. The calculations for this will not be shown for the LLC resonant converter as it is just a matter of adding thicknesses together and multiplying it with the number of turns. It is however shown for the hard switch converter in the last design step of section 3.2.1 because this is more important for the hard switch converter.

Due to the design of the Litz wire, the new strand of wire will have a thicker outer diameter. This is calculated as follow:

$$OD = \rho \times \sqrt{n} \times d \tag{3.28}$$

Where $\rho = 1.26$ is the packing factor (for 1 to 20 strands), n is the number of strands and d is the diameter per single strand of wire. The new diameter of the litz wire was calculated as 1.22 mm and were used on the primary side of the transformer (16 turns total to achieve 128 µH inductance) as this is the side carrying the least current and requires the most number of turns. On the secondary side insulated copper foil, 8 turns total (4 turns per coil of 8.1 µH inductance each), with a thickness of 0.125 mm were used to minimise conduction losses and optimize the available transformer windowing area. If the leakage inductance is not sufficient, an inductor may be added in series with the core that can be designed in the same way as the transformer.

The total inductance is measured on the primary side coil with the transformer secondary side open-circuited. It should be noted that this total inductance includes the sum of the leak and magnetizing inductance. Then, the secondary side is short circuited, and the leak-inductance can be measured on the primary-side. To obtain the true magnetizing inductance, subtract the measured leak inductance from the total measured inductance. Furthermore, it should be noted that the magnetizing inductance not only exists on the primary side, but also on the secondary side. This should have a minimal effect, but can be calculated as $llks = \frac{llkp}{a^2}$.

On the controller side, it is critical to have a high-resolution timer in order to control the frequency increments very precisely as the MOSFETs must switch at specific time intervals to maintain true ZVS operation. As the load on the transformer increases, the effective shunt inductance (magnetizing inductance) will decrease. The MOSFET output capacitance depends on the magnetizing inductance to discharge it in time before the MOSFET is switched on. This is achieved by switching above the resonant frequency and also using the proper dead-time.

The minimum dead time for a MOSFET (in full-bridge configuration) having an output capacitance of 3200 pF (IXTH48N65X2) during a no-load condition is calculated as follow:

$$t_d \geq L_m \times 16 \times \frac{0.5 \times C_{oss}}{T_s} \tag{3.29}$$

where t_d is the dead time for a center-aligned PWM signal, L_m is the magnetizing inductance, T_s is the period of the current switching frequency, C_{oss} is the MOSFET output capacitance which is multiplied in the equation above with a factor of 0.5 because it assumes the MOSFETs are being used in a Full-Bridge configuration. In a Full-Bridge configuration, a high-side MOSFET is effectively in series with a low side MOSFET. In a Half-Bridge configuration, the effective output capacitance, C_{oss}, should not be multiplied by 0.5. If the MOSFETs have a low output capacitance that makes it difficult for the controller to maintain a dead-time or if the controller does not have a high-resolution timer, then an external capacitor may be added in parallel to each MOSFET's drain-source pin and the new dead time may be calculated using the total capacitance combination.

The effect of magnetizing inductance on the dead time is shown in Figure 3-10. It can be seen that the dead-time required for ZVS operation at no-load condition is 327.7 ns. The dead-time can be larger than this value, but not smaller than this value.

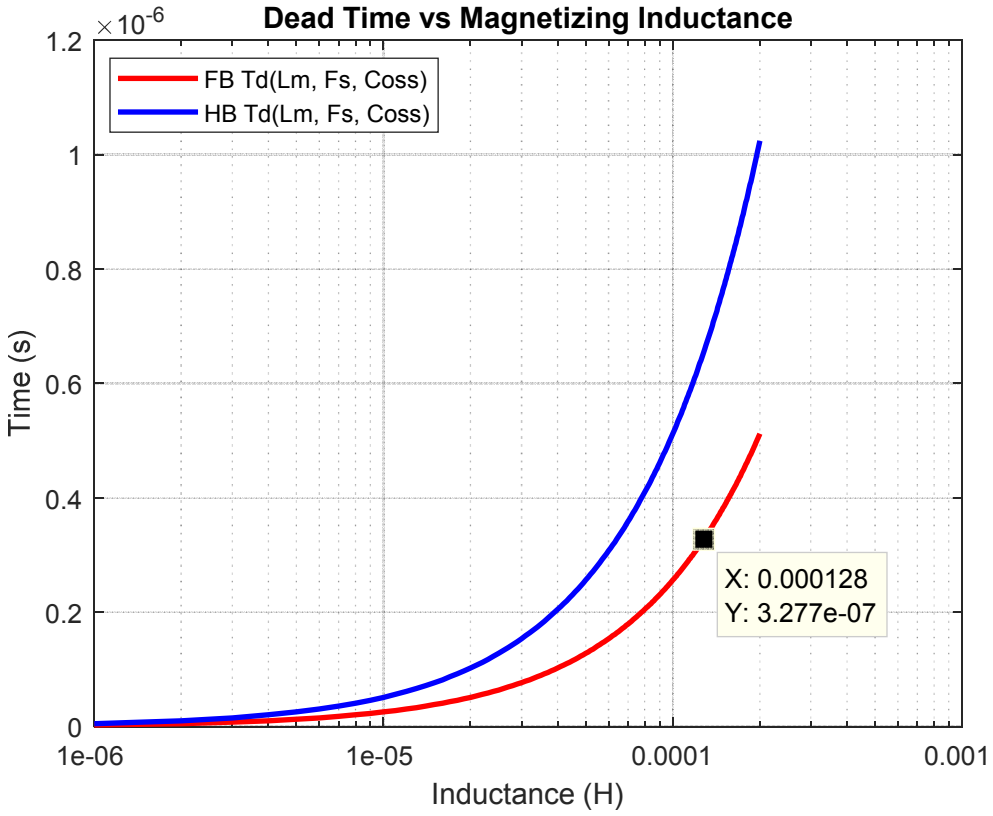


Figure 3-10: Dead time vs magnetizing inductance

Also important to note is that the operating frequency also has an influence on the optimal dead-time as shown in Figure 3-11. In both Figure 3-10 and Figure 3-11, the Full-Bridge configuration (shown in red) has been compared to the Half-Bridge configuration (shown in blue) for the same type of converter. It can be seen that for the same kind of converter, the Full-Bridge configuration requires less dead-time to operate in the ZVS mode.

The effective duty-cycle at the controller side is affected by the dead-time, and it should also be verified that the dead-time does not cause an overlap in the MOSFET switching cycle.

This can be calculated for the highest-frequency and the lowest frequency to ensure the effective duty per MOSFET does not exceed 50 % as this will cause a short-circuit.

The effective duty-cycle is calculated as follow:

$$D = \left(\frac{1}{f_s} - 2 \times t_d\right) \times F_s \times \frac{100}{2} \tag{3.30}$$

where D is the effective duty-cycle (per MOSFET). Twice this amount ($D \times 2$) is the effective duty cycle for the converter. The LLC resonant converter operates in Pulse Frequency Modulation (PFM) mode instead of Pulse-Width Modulation (PWM) mode at a constant duty-cycle.

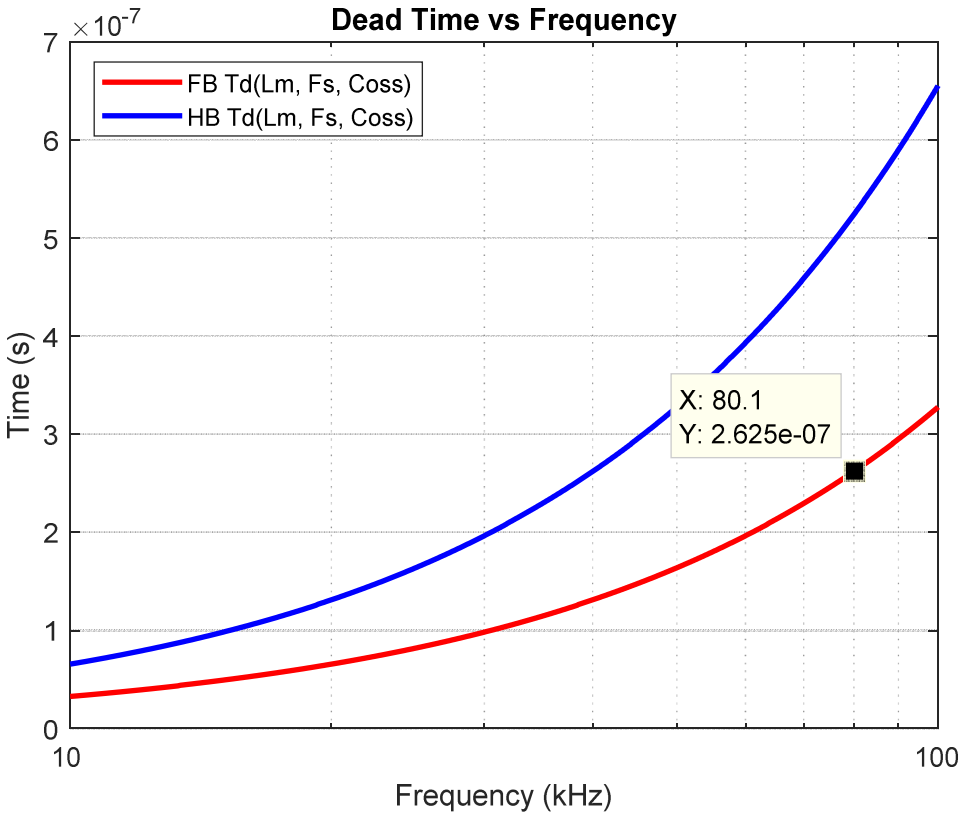


Figure 3-11: Dead time vs frequency

When the frequency is adjusted on the controller, the dead-time register value must be updated to maintain a constant dead-time as the adjustment of the frequency will influence the actual dead-time value. This must only take effect in the next pulse without accidently interrupting the current pulse as this may cause a transient and ultimately MOSFET failure, as discussed in section 2.1.2.3.

3.1.6 MOSFET Heatsink Requirement

To optimize the production cost and weight of a switching converter, it is preferred to use the smallest heatsink possible for all switching transistors. This will however increase conduction losses in the MOSFET and trade-offs need to be considered between cost, size, weight, performance and reliability. To see the effect of temperature on a particular transistor, consider the datasheet for tables and graphs showing the MOSFET turn-on resistance, $R_{ds(ON)}$, as a function of T_j (junction temperature). Based on this information the designer can calculate the losses due to an increase in junction temperature. Note that this refers to the instantaneous junction temperature inside the MOSFET – smaller heatsinking will drastically increase the peak junction temperatures. Exceeding the maximum junction temperature will cause irreversible damage to the silicon die and will consequently destroy other electronic components if the MOSFET short-circuits.

At higher temperatures, switching losses and times will decrease, leading to improved performance. This information can be found in the switching characteristics section of the datasheet and also the graphs showing the effective capacitances as a function of the junction temperature. Conduction losses on the other hand will increase due to the higher $R_{ds(ON)}$. A higher temperature will also increase the MOSFET's breakdown voltage (the maximum voltage it can handle). The MOSFET becomes more prone to avalanche failure at higher junction temperatures as the increased heat reduces the amount of energy required to free an electron from the atoms, leading to a higher risk of impact ionization.

To calculate the minimum heatsink size required, the thermal conductivity can be modelled as resistances that model the ability of each layer to conduct heat away from the junction to the air in °C/W. As shown in Figure 3-12, the thermal resistance of the layers are modelled as R_{th-jc} (junction to case), R_{th-cs} (case to transistor tab) and R_{sa} (heatsink to ambient).

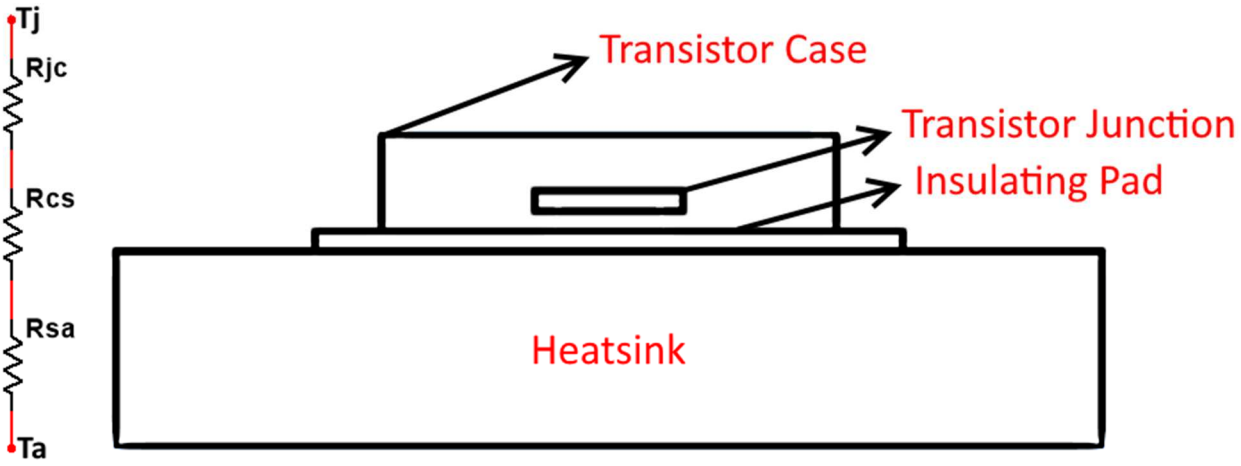


Figure 3-12: Junctions involved in heatsinking

Due to the many factors involved in accurately calculating the required heat-sink size, it is recommended to over-design as not all the parameters at which the junction can operate safely are listed in the datasheet. It is an iterative process in determining the correct heatsink size. The recommended procedure is to select a reasonable (depending on the wanted efficiency and reliability) junction temperature at which the MOSFET has a high $R_{ds(ON)}$, then calculate the conduction loss from that value. If the conduction loss is acceptable for the efficiency goal, proceed to calculate the transistor's junction to ambient temperature dissipation rate. The equations can be re-arranged to calculate the required ambient temperature to maintain a specific junction temperature in the MOSFET. Based on this iterative process, the optimal heatsink requirements can be obtained.

The junction temperature can be calculated as follow:

$$Tj = Pd(R_{th-jc} + R_{th-cs} + R_{interface} + R_{sa}) + Ta \tag{3.31}$$

To obtain the size of heatsink required, re-arrange the equation as follow:

$$R_{sa} = \frac{Tj - Ta}{Pd} - R_{th-jc} - R_{th-cs} - R_{interface} \tag{3.32}$$

The thermal resistance for the thermal insulating pad can be obtained as follows:

$$R_{interface} = \frac{t_{int}}{L_s \times W_s \times k_{interface}}, \tag{3.33}$$

where each symbol is defined as follows:

- T_a is the ambient air temperature
- P_d is the MOSFET power dissipation
- t_{int} is the pad thickness
- L_s is the height of the pad (only area underneath the transistor)
- W_s is the width of the pad (only area underneath the transistor)
- $k_{interface}$ is the thermal conductivity of the material as given in the datasheet

Fill in the values for the maximum allowed junction temperature as shown in the MOSFET datasheet as well as the junction to case and case to sink temperatures. Power dissipation can be calculated using (4.6) and by simulating in software. Then simply select a heatsink based on the calculated value that is lower than the calculated R_{sa} value.

Shown in Figure 3-13 [2] is the IXTH48N60X2 (normalised to 65 m.Ω) MOSFET's turn-on resistance as a function of junction temperature. The maximum allowed junction temperature of this MOSFET is 150 °C. A power dissipation of 3.5 W per MOSFET was calculated for a worst case scenario during a full load of 1-kW at 170 V (the lowest voltage during full-power MPPT) and an ambient air temperature of 35 °C was chosen. The maximum junction temperature will be 115 °C (to maintain a high efficiency) will be reached for a heatsink capable of at least 4.94 °C/W. If the MOSFET is operated up to its maximum junction temperature, then the required heatsink needs to be capable of dissipating heat at a minimum rate of 7.4 °C/W.

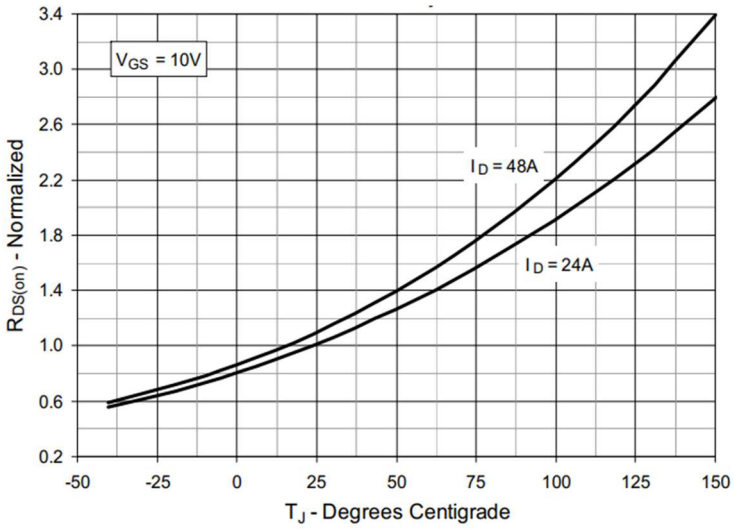


Figure 3-13: IXTH48N65X2 Rds(On) vs Tj [2]

The value for equation (3.33) was calculated as follow.

$$R_{interface} = \frac{t_{int}}{L_s \times W_s \times k_{interface}} = \frac{0.002}{0.014 \times 0.018 \times 1.8} = 0.44 \text{ °C/W}$$

Then the minimum required heatsink value is calculated from equation (3.32)

$$R_{sa} = \frac{Tj-Ta}{Pd} - R_{th-jc} - R_{th-cs} - R_{interface} = \frac{150-35}{14} - 0.19 - 0.21 - 0.44 = 7.4 \text{ °C/W}$$

The effective junction to air resistance can be calculated by adding together all the resistances

$$T_{ja} = R_{th-jc} + R_{th-cs} + R_{interface} + R_{sa} = 0.19 + 0.22 + 0.44 + 7.4 = 8.24 \text{ °C/W}$$

This indicates that the junction temperature of each MOSFET will rise at a rate of 8.24 °C per watt (2.06 °C per 0.25 W for each MOSFET). A flat aluminium heatsink measuring 80 mm × 200 mm × 4 mm has a thermal resistance of 5 °C/W [51] and will be sufficient and can be calculated using the thermodynamics for natural convection of a flat plate [52].

3.2 The Full-Bridge Hard Switching Converter

The hard switching converter uses the same design for all the power electronics with the addition of snubber circuits to supress EMI and voltage overshoots that may harm the MOSFETs in the high voltage section. Different MOSFETs (IPW60R099CP) with a lower output capacitance of 300 pF were used in this topology because they have a lower risk of latch-up and failure due to the lower capacitance as discussed throughout the literature study.

3.2.1 Ferrite Transformer (Hard Switching)

The design of a high frequency ferrite transformer suitable for hard-switching follows the same design procedure as the LLC resonant converter except there is no air-gap. This converter requires a lower switching frequency to prevent inductive ringing from superimposing, potentially causing MOSFET failure. Due to this lower switching frequency, a bigger core is required because more windings are required to avoid core saturation. Reduction of the air gap also causes a significantly bigger magnetizing inductance. A detailed step-by-step design procedure will be discussed in this section. This is an iterative process that may require repeating some design steps.

Step 1: Choose a transformer core and switching frequency

The transformer core and switching frequency must be chosen to start the first iteration of the design process. An E65 core were chosen with an operating frequency of 30-kHz. A low switching frequency, but high enough to be out of the audible range, should be chosen for the first iteration to keep the MOSFET switching losses to a minimum. Figure 3-14 shows the core dimensions for the chosen core.

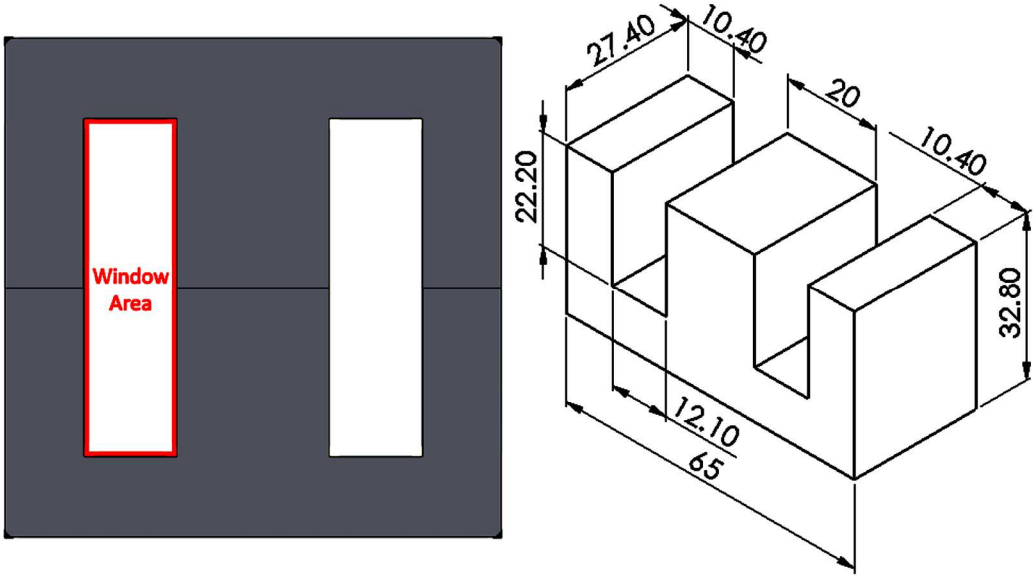


Figure 3-14: EE65 ferrite core for hard switching

Step 2: Defining the transformer turns-ratio

Define the requirements of the converter such as the input and output voltage requirements. The transformer turns ratio can then be calculated as follow:

$$a = \frac{Vout}{Vin_{nom} \times 2 \times D} \tag{3.34}$$

Where each symbol is defined as follow:

- $Vout$ is the output voltage of the transformer multiplied with 1.2 and adding 0.6. This is because 80 % efficiency is assumed as well as a forward voltage drop of 0.6 V caused by the output diodes.
- Vin_{nom} is the nominal input voltage, which is 170 V as this is the voltage associated with the maximum power point of the solar panels.
- D is the maximum duty cycle per MOSFET which is 0.45 to prevent shoot-through. This is a standard figure used by designers to prevent shoot-through.

Then calculate the primary to secondary turns ratio as $N = \frac{1}{a}$. The turns ratio was calculated as 3. The number of primary turns can be calculated as follow:

$$Npri = \frac{Vin_{nom}}{2 \times f_s \times A_c \times B_{max}} \tag{3.35}$$

The core cross-sectional area (A_c) is 535 mm² and the core saturation point (B_{max}) which has been found in the datasheet is 0.35 T. This number was reduced to 0.25 T due to the unknown effects caused by the square waves of the hard-switching converter. Transient current and voltage spikes may cause the core to saturate and cannot be calculated.

The number of primary turns required was found to be 21.2 which has been rounded up to 22. Then the secondary number of turns can be calculated as $Nsec = \frac{Npri}{N}$ = 7.

Step 3: Calculate the inductance ratio

To be able to simulate the transformer in LTspice®, the inductances of the core need to obtained. This can be calculated as follow:

$$Ueff = \frac{1}{\frac{2 \times g}{lc} + \frac{1}{U_r}} \tag{3.36}$$

Each symbol used are defined as follow:

- g is the air-gap, which is 0 mm for the hard switching converter.
- lc is the magnetic path-length of the core as found in the datasheet and
- μ_r is the permeability for the N87 ferrite in the core datasheet which is 1700;

The effective permeability equation reduces to $\mu_{eff} = \frac{1}{\mu_r} = 1700$ due to the absence of an air-gap. This also simplifies the calculation of the inductance ratio, which can be calculated as follow:

$$AL = \frac{\mu_o \times \mu_r \times Ac}{2 \times g \times \mu_r + lc} = \frac{\mu_o \times \mu_r \times Ac}{lc} \quad (3.37)$$

The calculated AL value is 7775 nH/t^2.

Step 4: Calculate the inductances

The corresponding primary and secondary coil inductances are calculated as follow:

$Lm_{pri} = AL \times Np^2$ = 3800 µH (Measured on transformer as 3700 µH)

And

$Ls_{\text{sec}} = AL \times Ns^2$ = 381 µH (Measured as 420 µH)

Small winding imperfections may be due to a small but negligible air gap. Permeability is also greatly affected by temperature when no air-gap is added to a transformer.

Step 5: Calculate skin depth

To minimise the effect of skin depth, it is preferred to use multiple strands of thin wires and twist them together to make a thicker strand. This occurs at higher frequencies where current starts to flow on the surface of the conductor instead of distributing throughout the entire conductor. It is also referred to as the wire's equivalent AC resistance. The effect of skin depth vs frequency is shown in Figure 3-9 in the previous design section of the LLC resonant converter.

Step 6: Calculate the Litz wire requirement

The outer diameter of the Litz wire can be calculated using the following formula:

$$OD = p \times \sqrt{N} \times d \quad (3.38)$$

Where OD is the outer diameter, p is the packing factor of 1.25, N is the number of strands and d is the thickness of each strand. The primary coil consist of six twisted wires each having a

diameter of 0.5 mm. This makes the total thickness of the strand 1.4 mm. The secondary coil uses 7 turns of 0.125 mm copper foil per winding (two windings) and has two windings.

Step 7: Verifying all parameters

To verify that all the copper will fit onto the core of the transformer, the windowing area must be known. For the EE65 core, these dimensions are W×L = 12.10 mm × 44.40 mm as shown in Figure 3-14. To make sure the primary number of turns (22 turns) will fit into the height (length) of windowing area, multiply half the number of primary turns with the thickness of the Litz wire diameter. The reason for taking half the number of primary turns into account is because the secondary windings will come in the middle – thus half the number of primary turns, then the secondary windings, then the other half of the primary windings. This is to keep the leakage inductance of the transformer at a minimum.

Height required = 1.4 mm × 11 = 15.4 mm. There will thus be plenty of space in the total windowing height of 44.4 mm. The secondary foil can be cut to fit this height. Then the width of the windowing area needs to be verified. This may become more complicated and will be listed in bullet form below to avoid confusion. It can be determined as follow:

- There will be 22 turns of 1.4mm Litz wire, wound as 11 + 11. Thus the total thickness required by the primary coil will be 1.4 mm + 1.4 mm = **2.8 mm**.
- The Kapton tape that will be used to insulate the copper foil is about 0.0625 mm thick. Two layers are required to cover the copper foil (thus the total thickness is 0.0625 × 2 = 0.125 mm) on both sides and there are 7 + 7 turns of copper foil which is 0.125 mm thick per turn. This gives a total thickness of 0.25 mm required per secondary turn. Now simply multiply this with the number of copper layers inside the windowing area which is 0.25×14 = **3.5 mm.**
- Because the centre leg of the core is not perfectly round, it is also important to understand that the winding of the core will cause the copper to lift off from the core. It will not fit perfectly. This can be better understood by looking at Figure 3-15. The red are is where the circular winding of the copper will create an air-gap. This is somewhat compressible when assembling the core and the thickness of the air gaps created can be calculated using the Pythagorean theorem and drawing a small triangle in the centre of the leg. It is important to note that the air-gap created has no effect on the magnetizing inductance as the air-gap does not lie between the two EE core halves.
- The radius for an equivalent circle can then be calculated. The air-gap thickness is then 17 mm - 10 mm = 7 mm, but can easily be compressed to below **3 mm** when assembling the core.

- The thickness required to insulate the primary and secondary windings from each other and the outer legs (for safety) is 0.25 mm and three insulations are required. This adds to **0.75 mm** and
- Finally all the values can be added together to result in a total thickness of **10 mm**. The total number of windings will thus fit onto the core and the core is now optimised. Multiple iterations, starting at step 1 may be required to obtain the perfect core utilization.

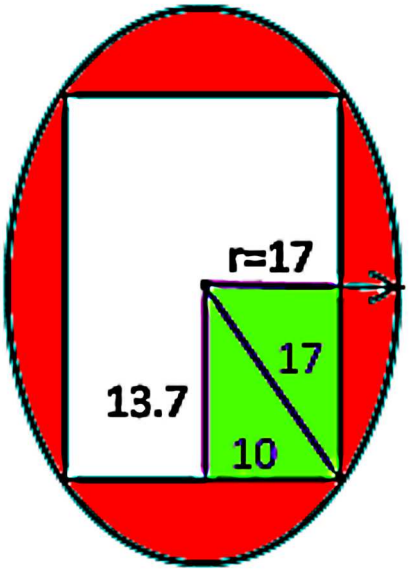


Figure 3-15: Winding around centre leg

3.2.2 Snubber Circuits

The addition of RC snubber circuits have the following advantages:

- Reduced voltage and current spikes.
- Limits the rate of change (dV/dt and dI/dt).
- Prevents excessive power dissipation in the switches.
- Reduced total loss due to minimised switching losses and
- Reduced EMI due to the damping of current and voltage ringing.

Adding a diode in parallel to the resistor (RCD snubber) adds the benefit of reducing the power loss in the resistor. It also helps to reduce the rate of voltage change when the MOSFET switches off and can greatly reduce its switching losses. The disadvantage is that during the charging cycle of the snubber capacitor the effective resistance will be zero due to the parallel diode. This will result in a higher peak voltage during the MOSFET's turn-on switching cycle. Peak current in the snubber capacitor will also be higher but it will lower the switching losses of the MOSFET.

An optimised snubber circuit will dissipate the energy stored in the parasitic inductances instead of allowing the inductor to deliver this energy back to the MOSFET junction which can lead to an

avalanche condition. These parasitic inductances are caused by the transformer, PCB traces and MOSFET leg and bond wire inductance.

From well established literature [53], [54], [55] on RC snubber design it is recommended to start the design process by selecting a capacitor value (C_{snub}) equal to the sum of the MOSFET's output capacitance and its mounting capacitance. By measuring the transformer leakage inductance, select a series resistor that critically damp the ringing as follow:

$$R = \sqrt{\frac{L_p}{C_{snub}}}. \tag{3.39}$$

Where L_p is the parasitic inductance and C_{snub} is the chosen capacitor value. To ensure the resistor value is reasonable, calculate the power dissipated in the resistor as follow:

$$P_{diss} = C_{snub} \times V_{sw}^2 \times f_s \tag{3.40}$$

Where V_{sw} is the switching voltage of the MOSFET. The power dissipating resistor must be chosen so that its rated power dissipation value is larger than twice the calculated value.

The average voltage across each MOSFET in the full-bridge converter is half of the supply voltage which is 170 V. The transformer leak inductance is 4 µH and the parasitic output resistance of each MOSFET (including the mounting capacitance) is about 500 pF. A 1 nF capacitor in conjunction with a 100 Ω resistor will dissipate 0.2 W of power across each MOSFET as seen in Figure 4-18. Figure 3-16 below shows the connection diagram of the RC snubber (R15 and C7). It should be noted that D7 shown in Figure 3-16 does not form part of the RC snubber design, it represents an internal body diode or externally added freewheeling diode for the MOSFET.

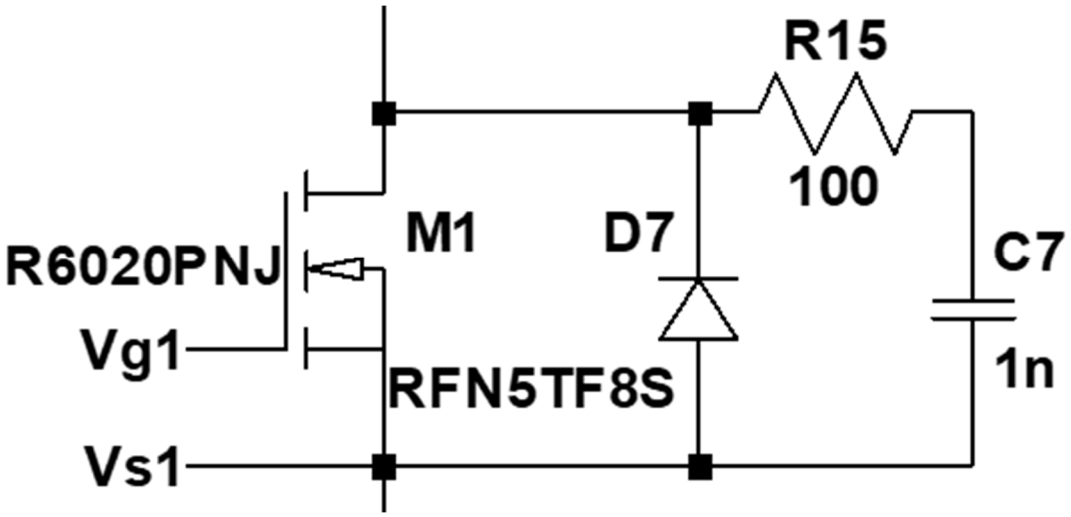


Figure 3-16: RC snubber circuit

3.3 Conclusion and Chapter 3 Summary

This chapter shows how to design an LLC resonant converter and a hard switching converter while optimizing the transformer to achieve a maximum efficiency. The LLC resonant converter is able to achieve soft-switching over a wide input voltage range and at any load (even at no-load). This will make this kind of converter highly suitable for coupling a renewable energy source to an electrolyser because renewable energy sources do not provide a constant output voltage and an electrolyser do not represent a constant resistive load. It is also evident from the design procedure that the LLC resonant converter requires a more sophisticated transformer than the hard-switching converter, but requires fewer components due to the absence of snubber circuits. The hard-switching converter will be less energy efficient because it cannot achieve ZVS at all and may not even achieve the design goal of 1-kW before causing a MOSFET failure. A properly optimised RC snubber can prevent a MOSFET failure in the hard-switching converter. This will also be verified in the simulations and validated in the measured results.

CHAPTER 4: SIMULATION AND VERIFICATION

4.1 LLC Resonant Converter

The simulation of the LLC resonant converter will be disussed in this section. It is known from the literature that the LLC resonant converter is able to achieve ZVS over the entire load range and therefore has a high efficiency. This converter is preferred for coupling an electrolyser to a solar panel array due to its high efficiency, reliability and lower component count. It has been simulated in both Matlab Simulink® as well as LTspice® to verify the accuracy of implementation in the simulation software against the literature and theoretical design process including the mathematical modelling in 3.1.1.

4.1.1 Resonant Tank Circuit

In this section, various methods were used to test the design chapter's models in order to verify the predicted results. In order to fully understand the results below, one has to consider the circuit shown in Figure 4-1 where a square wave is applied to the tank circuit which results in a near perfectly shaped sinusoidal output. A load on the output side of the converter can therefore be modelled as an ac resistance on the primary side of the circuit.

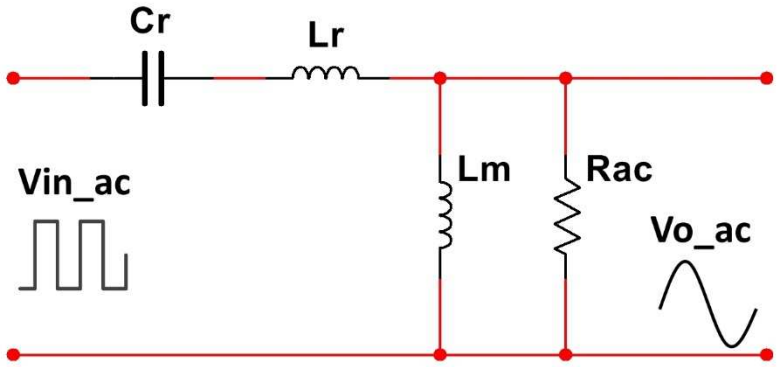


Figure 4-1: LLC transfer circuit

The transfer function for the circuit given in Figure 4-1 is given by

$$K(Q,m,Fn) = \left|\frac{Vo_{ac(S)}}{Vin_{ac(S)}}\right| \tag{4.1}$$

and the reflected ac resistance as viewed from the primary side circuit model in Figure 4-1 is calculated as:

$$R_{ac} = \frac{8}{\pi^2} \times \frac{N_p^2}{N_s^2} \times R_o \tag{4.2}$$

Where $\frac{N_p^2}{N_s^2}$ is the transformer primary to secondary turns ratio and R_o is the output resistance. Quality factor is calculated as follow:

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \tag{4.3}$$

4.1.2 First Harmonic Approximation (Mathematical Model)

Presented in Figure 4-2 is the LLC resonant converter's resonant tank gain. This is highly dependent on the switching frequency, load resistance and input voltage. The characteristic curves will change as the input voltage, load or converter design factors such as inductance ratio or quality factor changes. To be able to correctly interpret the results from the characteristic curves, it is important to understand the operating principle and the mathematics involved which is explained here.

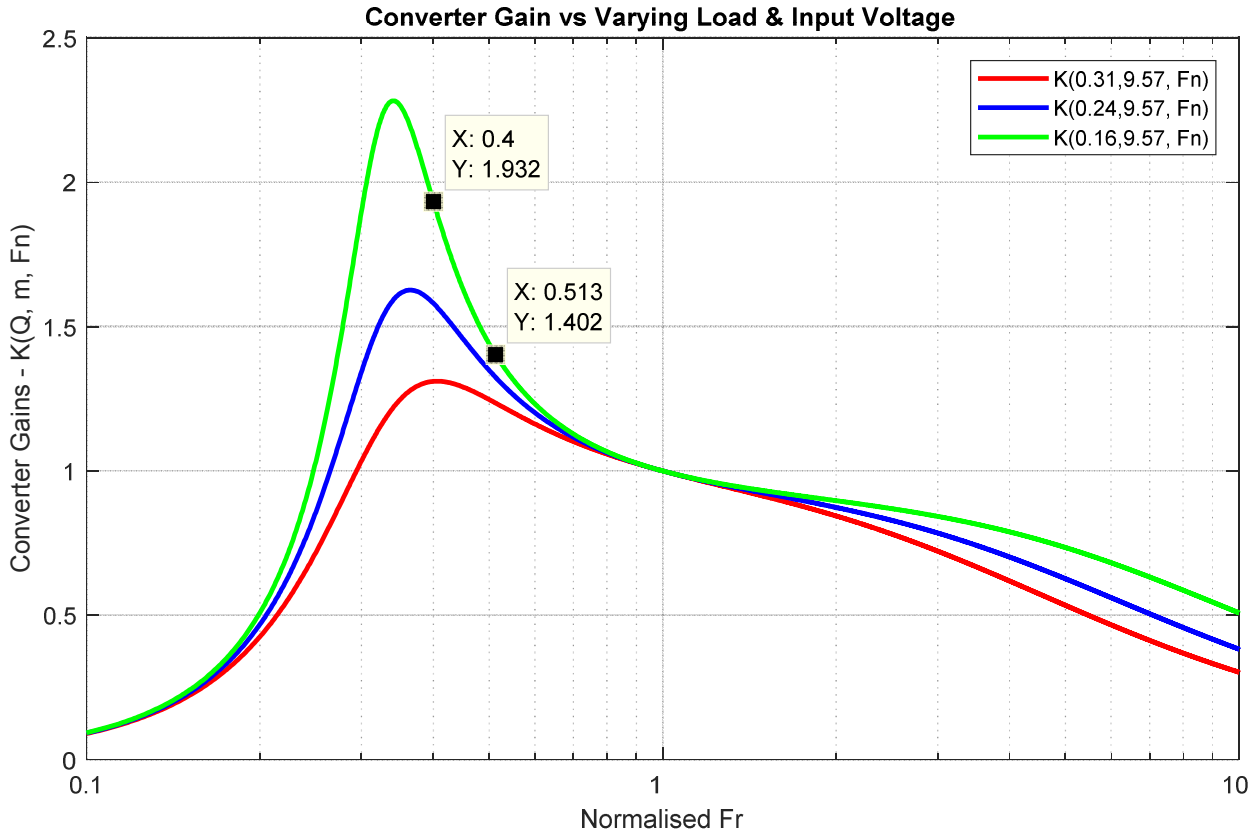


Figure 4-2: LLC Resonant Converter characteristic curve

To calculate the effective conversion gain, which is used to predict the output voltage at a specific load, consider the following equation:

$$\begin{aligned} &Converter\ gain \\ &= switching\ bridge\ gain \times resonant\ tank\ gain \\ &\times transformer\ turn\ ratio\ (Ns/Np) \end{aligned} \tag{4.4}$$

Switching bridge gain is a constant value that depends on the primary switching bridge. It's value is 0.5 when the switching bridge is a Half-Bridge and 1 for a Full-Bridge. The resonant tank gain is the curve presented in Figure 4-2 which is a logarithmic plot with a normalised frequency on the x-axis. The resonant frequency was normalised to 74-kHz instead of 80-kHz because the actual inductances as measured on the transformer differed slightly from the calculated values because of winding imperfections. The resonant capacitor value used was the closest value locally available. Finally, the transformer turns ratio was calculated as 3.8, but was rounded up to the nearest integer value which is 4.

The required resonant tank parameters were determined to be as follow

- Resonant inductance (Lr) of 16 µH (15.4 µH on actual transformer).
- Magnetizing inductance (Lm) of 129 µH (132 µH on actual transformer).
- Resonant capacitance (Cr) of 0.25 µF (0.3 µF on actual circuit) and
- The resonant frequency is 74-kHz due to the slight differences in component values;

To correctly interpret the results from the gain curve, one must first understand the equations in section 4.1.

To calculate the output voltage of the point indicated on the green curve of Figure 4-2, which represents a quality factor of 0.31, an inductance ratio of 9 and a supply voltage of 120 V, use the converter gain equation as follow.

$$V_{out} = V_{in} \times K_{switch} \times K_{tank} \times N \quad (4.5)$$

Where V_{in} is the input voltage, K_{switch} is the switching bridge gain, K_{tank} is the tank circuit gain and N is the transformer secondary to primary turns ratio.

$$V_{out} = 1 \times 120 \times 1.402 \times ¼ = 42\,V$$

The load resistance is 1.7 Ω which indicates the converter will easily be able to achieve a gain to supply 1-kW of power at a switching frequency of $0.513 \times 74e^3 = 38$-kHz.

4.1.3 Circuit Simulation (Matlab® Simulink Model)

Shown in Figure 4-3 is the Simulink® circuit implemented in Matlab® that represents the LLC resonant converter for which the circuit parameters in sections 3.1.1 and 4.1.1 has been mathematically calculated. It is divided into 4 main sections, they are:

- Full-Bridge Switching (section responsible for the high voltage switching).
- LLC Tank and Transformer (resonant circuit components such as the transformer).
- Diode Rectifier (shows the AC to DC rectifier) and
- Output Filter (a filtering capacitor);

Shown in the full-bridge switching section are the MOSFETs and their corresponding input and output measurement points. Scope 1 and Scope 2 shown in Figure 4-3 shows what signals are measured as well as where it is being measured according to the labels. As can be seen, MOSFET 1 and MOSFET 3 share the same input signal from the PWM controller. This means they will switch on and off at the same times and will therefore close the circuit for continuity. The same current will flow through both switches when they are on as they are effectively in series with each other and the LLC tank circuit when switched on.

The pulse generator generates PWM signals, g1 and g2, with an adjustable frequency and dead-time. These PWM signals are fed into the MOSFETs to control the switching frequency and dead-time, which is required to give the MOSFETs enough time to discharge their parasitic capacitances completely before they are being switched on. On an actual implemented circuit, it is required to plot the gate-source voltage (g1 and g2 in Scope 1 and 2) on the same graph as the drain-source voltage (V fet1 and V fet2 in Scope 1 and 2). If the circuit is operating in ZVS mode, the drain-source voltage should be zero when the gate-source voltage rises to switch the MOSFET on. The drain-source current should also be measured to ensure the MOSFET current ratings are not exceeded and can be used to calculate the power losses in the MOSFET. Since the LLC resonant converter does zero voltage switching across the entire load range and therefore eliminates the Miller effect, the switching losses can be neglected and only conduction losses will be measurable. The conduction loss per MOSFET is given as

$$P_{sw} = D \times I^2 \times Rds_{ON} \tag{4.6}$$

Where D is the effective duty cycle, I is the RMS current in the resonant tank and Rds_{ON} is the MOSFET's turn-on resistance. Simulated values may differ from measured values as a rise in the MOSFET's temperature will cause a significant rise in the turn-on resistance.

Scope 4 shows the measured parameters in the LLC tank. This includes the primary tank current, Ip, the capacitor voltage, Vc, and the square wave generated by the switching section, Vt. The primary tank current should correspond to the sum of the current through the switches and should have the shape of a sinusoidal wave with minimal distortion. This is also the case for the voltage

over the resonant capacitor as should represent a sinusoidal waveform and should not contain any transient voltage spikes that exceed the capacitor's voltage rating. The voltage generated by the switches should represent that of a high voltage square wave with a DC offset of zero volts with minimal distortion.

In the diode rectifier section, the current waveforms are measured for each diode (d1 and d2) to verify that each diode's current rating is not exceeded. A current imbalance in this section is normal for a centre-tapped secondary winding transformer. This is due to the outer winding being wound on top of the inner coil and therefore uses a longer conductor and have a larger leakage inductance. It can be compensated for by adjusting the gate drive signals to have a counter imbalanced PWM duty cycle. The rectified current value is measured as Id and should be the same as the sum of $d1$ and $d2$. Output power is measured as the product of Vo and I_0 after filtering. When implementing MPPT on PV panels, I_0 and V_o will represent the output voltage and current and can also be used for short-circuit and over-voltage protection.

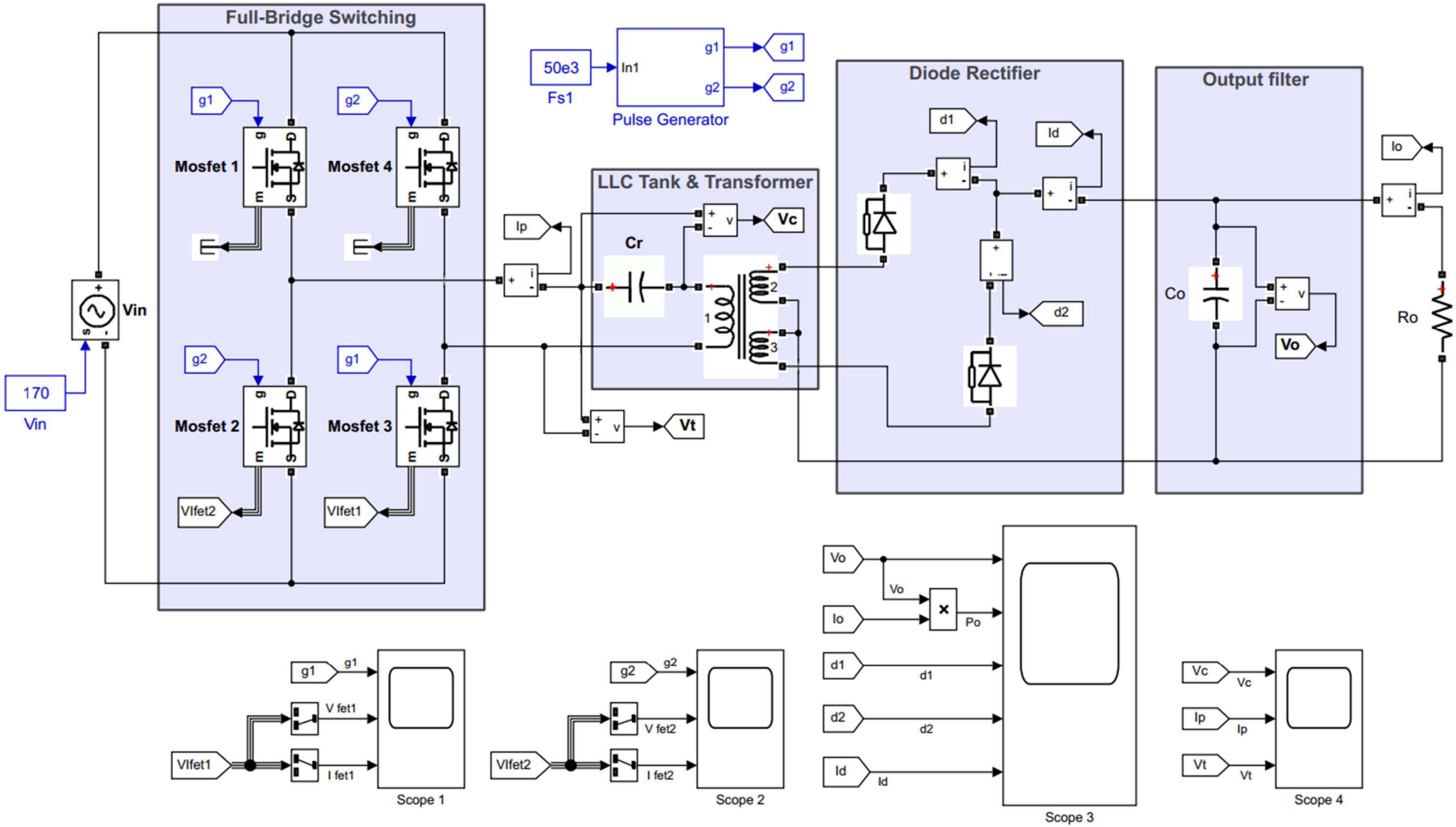


Figure 4-3: LLC Resonant Converter (Matlab® Simulink model)

The simulation setup as depicted in Figure 4-3 assumes an integrated magnetics design where the resonant inductor, L_r, is contained in the same core as the magnetizing inductance L_m. Parasitic resistances present inside the transformer windings were measured on the actual transformer and was found to be 50 mΩ for the primary coil and 2.5 mΩ per secondary coil. The switching frequency was set to 50-kHz with a dead time of 500 ns as this is the required switching frequency to dissipate 1-kW of power into a 2.45 Ω load at approximately 50 V while the input is at a stable 170 V.

It can be seen that the MOSFET waveforms shown in Figure 4-4 is characteristic to that of a circuit operating the ZVS mode. As the gate of the MOSFET is turned on, the MOSFET's drain-source voltage is already at zero voltage, resulting in a perfect ZVS turn-on with minimal switching losses associated with low heat dissipation. The Miller effect is absent and no inductive ringing can be observed and therefore a very high reliability. These waveforms will look identical for each MOSFET, except there will be a small dead time (500 ns) between each high and low side MOSFET, however what is important to note is the trend of what is happening which is the verification of a ZVS turn-on condition. The drain-source voltage is shown in Figure 4-4 as $V\ fet1$ while the current is shown as $I\ fet1$.

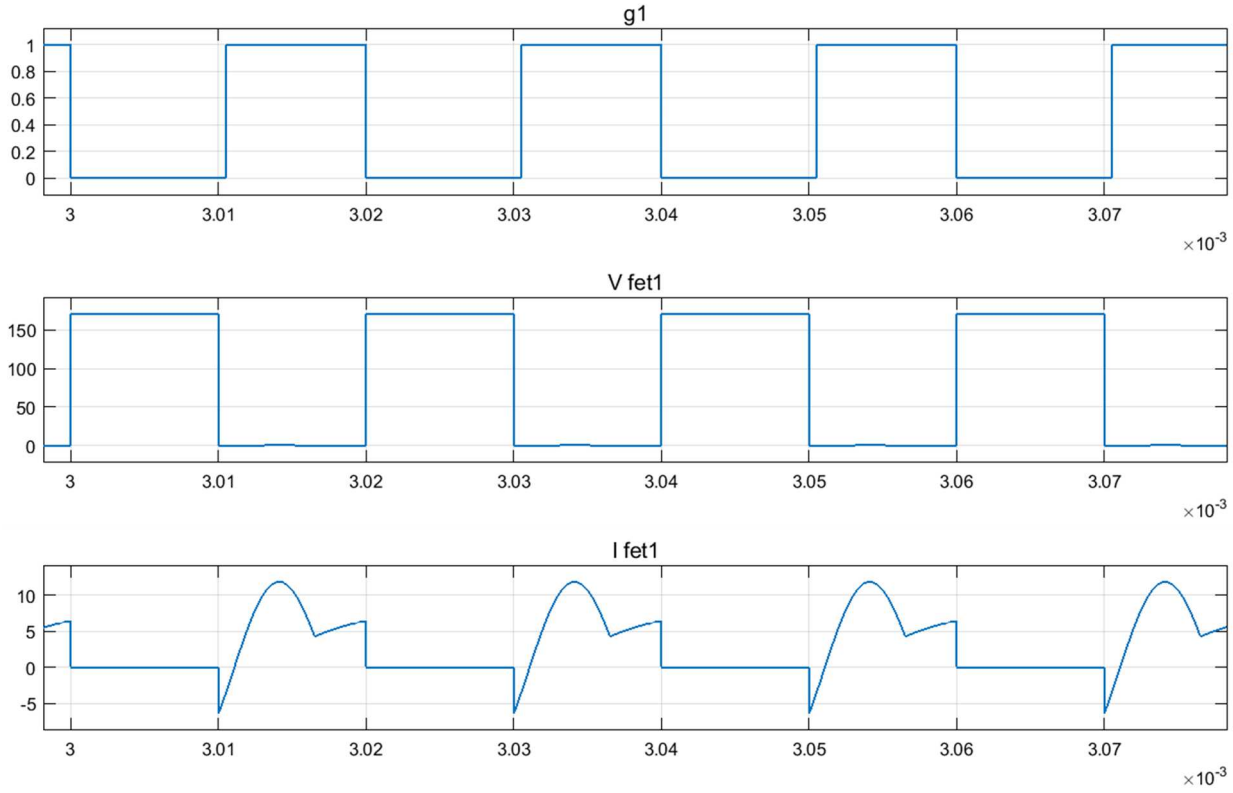


Figure 4-4: MOSFET switching waveforms (Simulink®)

It can be seen that the circuit is operating above resonance by measuring the voltage over the resonant capacitor as well as the current flowing through it. The voltage over the resonant capacitor is nearly sinusoidal, indicating the converter is operating above its resonant frequency. When the converter is operating at its resonant frequency, the voltage waveform over the capacitor will be a perfect sinusoid, however this is unwanted as this would mean the converter is operating at the maximum gain point and has no more room left for a voltage boost or buck capability. It should be noted that operation above resonance is preferred when designing an LLC resonant converter as this gives the converter the ability to buck the voltage down to a lower level while achieving true zero voltage switching.

The LLC tank current is shown in Figure 4-5 as Ip while the voltage over the capacitor is shown as Vc. The high-voltage square wave shown as Vt is the voltage generated by the full-bridge circuit that is supplied to the LLC tank circuit. All currents greater than zero that is shown in waveform Ip passes through MOSFETs 1 and 3 shown in Figure 4-3 while all current cycles below zero are passing through MOSFETs 2 and 4 shown in Figure 4-3. This also corresponds to Figure 4-4 which shows the waveforms for MOSFET 1 and 3.

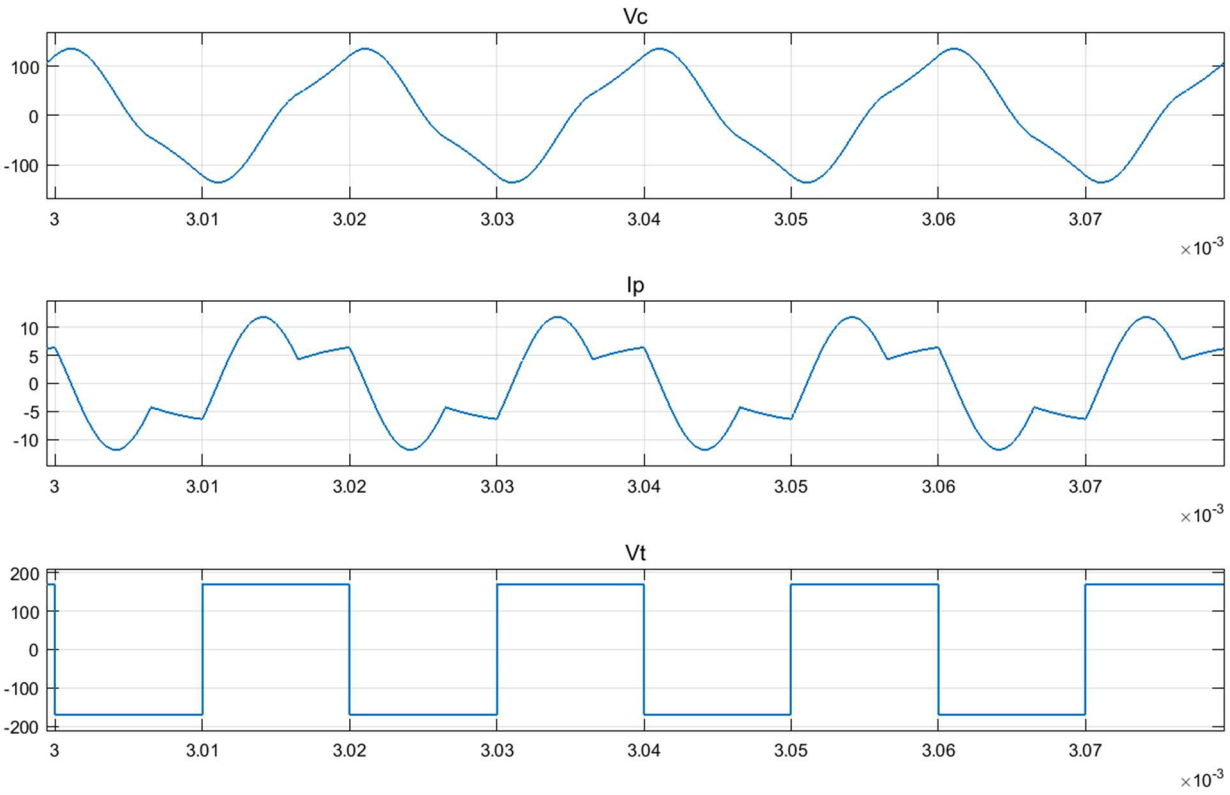


Figure 4-5: Resonant capacitor measurements (Simulink®)

Ripple voltage during full-load operation is less than 150 mV peak-to-peak as shown in Figure 4-6. Each current waveform shown in Figure 4-3 ($d1$ and $d2$) corresponds to each output coil on the transformer as well as the current passing through each of the diodes. The total rectified diode current is shown as Id while the output voltage and power supplied to the load is shown as Vo and Po respectively in Figure 4-6. Ripple can be reduced by adding multiple output capacitors in parallel to increase the capacitance while reducing the total ESR.

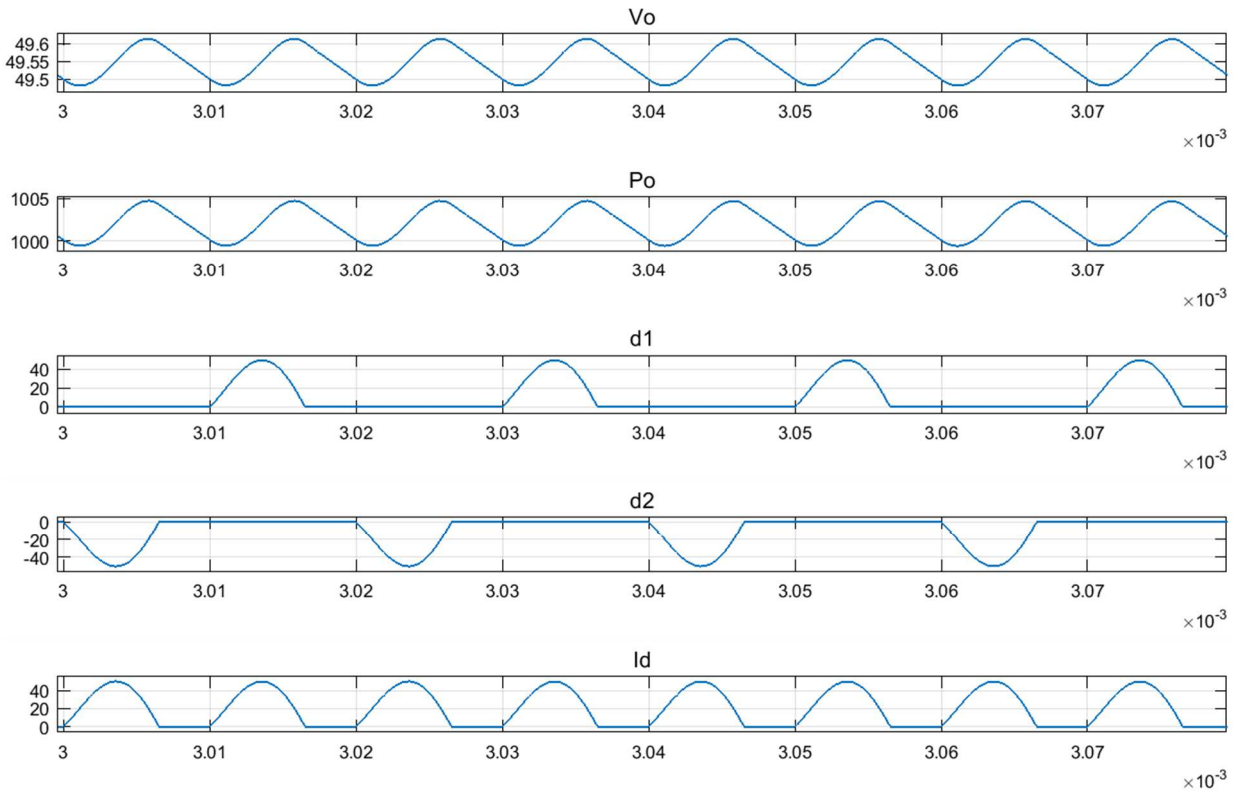


Figure 4-6: Output circuit waveforms (Simulink®)

4.1.4 Circuit Simulation (LTspice® Model)

The equivalent model for the LLC resonant converter implemented in Matlab® Simulink® has been re-implemented in LTspice® because the Simulink® model only provides a generic component database and does not automatically take parasitic components into account as it is aimed at simulation speed rather than accuracy. This can be handy for verifying a mathematical model, but it may be slightly less accurate than the LTspice® which has a significantly bigger component database containing detailed parasitic elements for each component. It will also ease the measuring of MOSFET, diode and copper losses and also allows for the simulation of a model where the resonant inductor is not integrated into the magnetic structure that contains the magnetizing inductance. This model, including the SPICE directive code used in the simulation is shown in Figure 4-7.

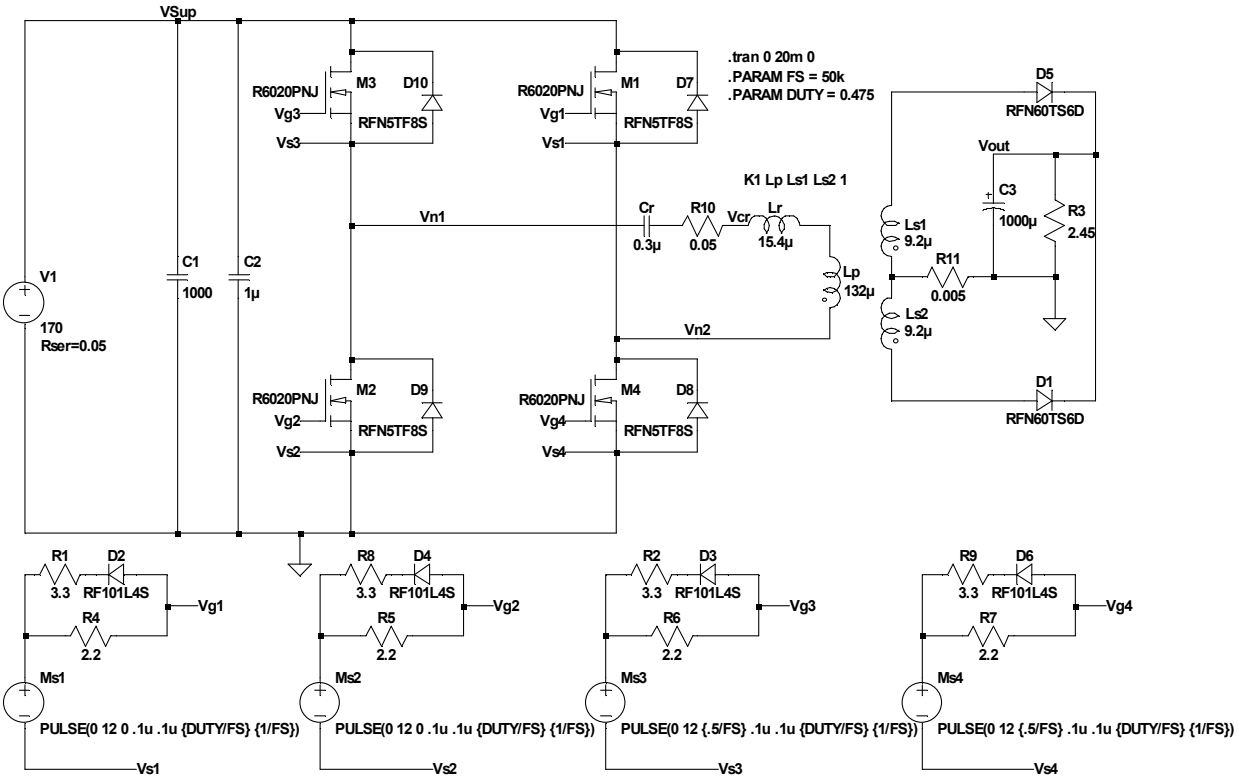


Figure 4-7: LLC Resonant Converter (LTspice® model)

Each MOSFET driver's gate circuit containing the turn-on resistor as well as the fast-turn off diode is shown in Figure 4-7. All gate drivers are mimicked using a SPICE directive and a pulsed voltage source. It can also be seen that in this model, the freewheeling diode of each MOSFET is added externally. These measurements are shown in Figure 4-8 where the red waveform shows the MOSFET junction and body-diode current. Parts of the current waveforms that are encircled in light-blue shows the current that flows for a fraction of the time through the MOSFET body-diode before the MOSFET junction is switched on. The part of the current waveform that flows through the MOSFET junction is between the yellow circles.

The section of current flowing through the body-diode of the MOSFET causes the body diode to start conducting, allowing the voltage across it to drop very close to zero. Then the controller allows just enough dead-time to allow the current flowing through the body diode to completely discharge the MOSFET's output capacitance as the diode switches on. After the controller waits a short time of 500 ns, the MOSFET is forward biased, allowing the turn-on resistance of the MOSFET junction to dominate over the body diode and allowing current to flow through the junction instead of the diode. This also forces the last bit of parasitic charge out of the diode junction and also allows for a faster diode reverse recovery time (yellow in Figure 4-8). This also eliminates the Miller effect caused by other parasitic capacitances in the MOSFET. The result is an ultra-fast, transient-less turn-on and turn-off of the MOSFET that dramatically improves the converter efficiency. The areas in Figure 4-8 encircled in light-blue is where the body diode starts to conduct and the areas in yellow is where reverse recovery takes place.

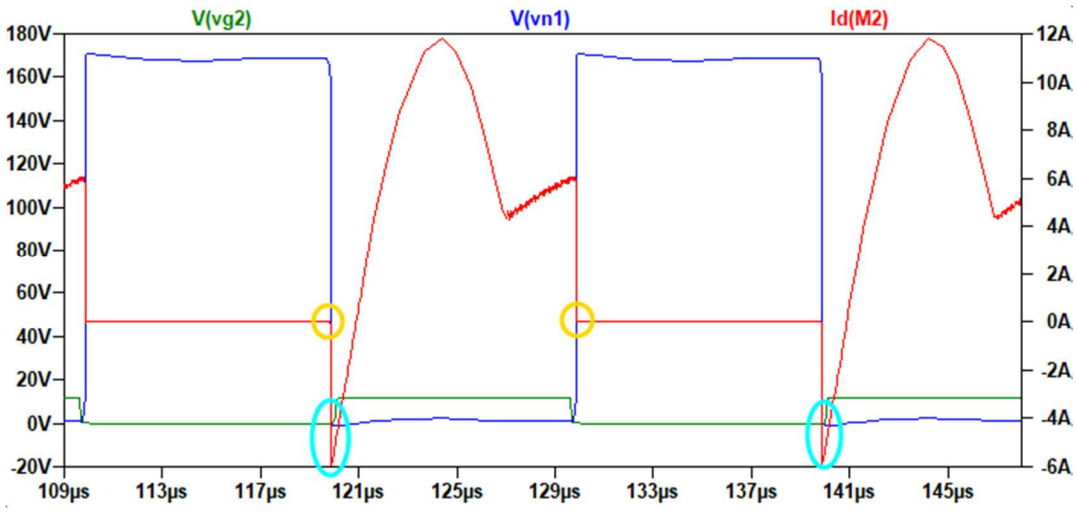


Figure 4-8: MOSFET switching waveforms (LTspice®)

Figure 4-8 shows the MOSFET gate-source voltage waveform (green) and the corresponding drain-source voltage (blue). The voltage scale is shown to the left while the current scale is shown on the right hand side. Measurement nodes are shown at the top and corresponds to the nodes seen in the simulated SPICE circuit in Figure 4-7.

Shown in Figure 4-9 is the voltage waveform generated by the H-Bridge (blue) and the current waveform (green) flowing in the primary side LLC tank circuit. As can be seen, the current waveform (red) lags the voltage waveform, indicating a lagging power factor associated with an inductive load. The circuit is therefore said to operate in the inductive region which implies operation above resonance and will always result in ZVS. If the circuit enters the capacitive region (to the left of the gain curve shown in Figure 4-2) it will begin to hard-switch and will lose its ZVS capability. This can lead to permanent MOSFET damage as the diode may not exit its reverse-recovery mode in time and cause a latch-up in the MOSFET junction as explained in sections 2.1.2.4, 2.1.2.5 and 2.1.2.6.

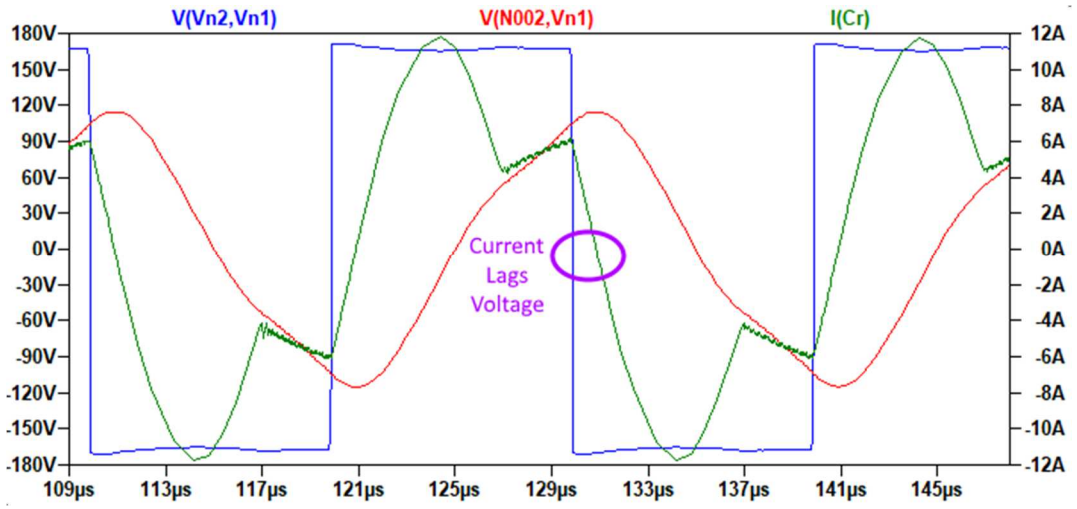


Figure 4-9: Resonant capacitor measurements (LTspice®)

The rectifying diode waveforms are shown in Figure 4-10 and each label corresponds to the component labels in the circuit shown in Figure 4-7. Each diode pair used in the actual circuit is capable of up to 120 A peak (two DSEI60-06A diodes in parallel on each output coil capable of handling currents up to 60 A each). It should be noted that the current rating given in the datasheet usually represents the diode's peak current (unless specified) and not the RMS current. Peak currents will always be higher than the RMS current. In Figure 4-7 the peak current per diode is about 45 A while the RMS current is at 10 A per diode. A load of 1000 W will draw 20 A at 50 V.

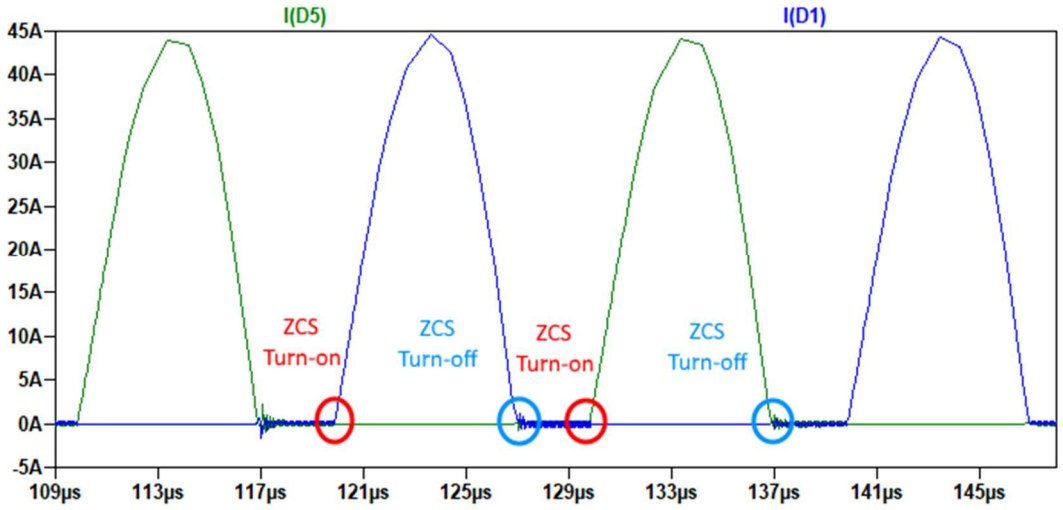


Figure 4-10: Diode waveforms (LTspice®)

An output load is simulated as a 2.45 Ω resistor, shown as R3 in Figure 4-7. Voltage (green) and power (blue) waveforms are shown in Figure 4-11. The simulated peak-to-peak voltage ripple is less than 100 mV for a supply voltage of 49.68 V while delivering 1-kW of power to the load.

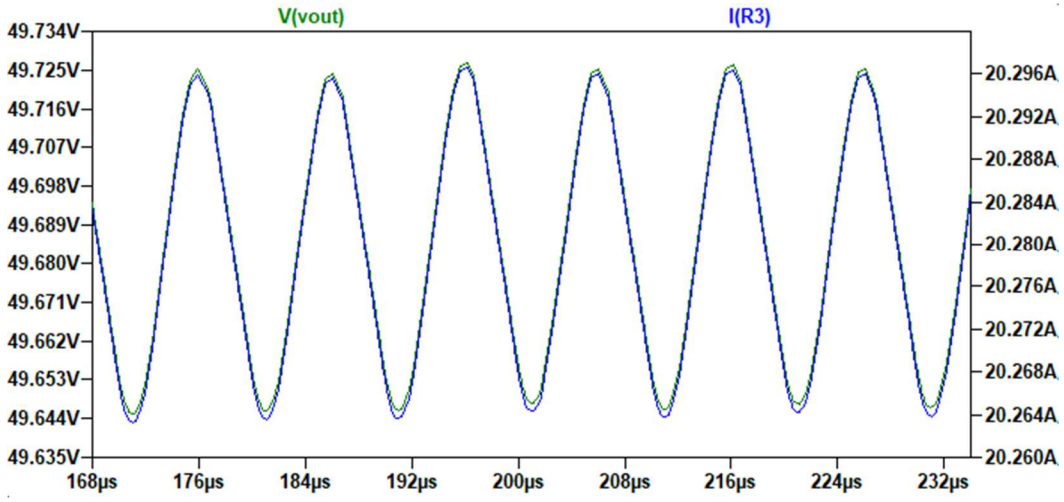


Figure 4-11: Output waveforms (LTspice®)

What is important to note in these simulations are the ZVS, the fast recovery of the body diode and the absence of voltage and current spikes. The magnitude of the output voltage is not important because it can be changed by varying the switching frequency. In a closed-loop control system this happens continuously to maintain ZVS.

4.1.5 Transformer Utilization (ZVS)

The utilization of the core must be calculated to ensure the ferrite material does not saturate as this will lead to a drop in the transformer's inductance and therefore will cause the LLC tank circuit to behave like a capacitive load (leading power factor). This will cause a short-circuit, temperature rise, increased core, copper and switching losses.

Shown in Figure 4-12 is the plot of the delta flux density (ΔB) vs frequency for the EE55 transformer core shown in Figure 3-7 in Section 3.1.5. The calculation of the transformer flux density is given in (3.26) and is a function of frequency (Hz), total cross sectional area (A_c in mm²), primary to secondary turns ratio (N) and output voltage ($Vload$) of the core. Magnetic saturation for N87 ferrite occurs at 0.38 T, it is therefore required to operate well below this point to avoid saturation. Also shown in the data-points of Figure 4-12 is the flux density swing at 30-kHz (which is the converter's lowest operating frequency – the point of maximum gain) and 50-kHz (the point at which the converter will operate most of the time).

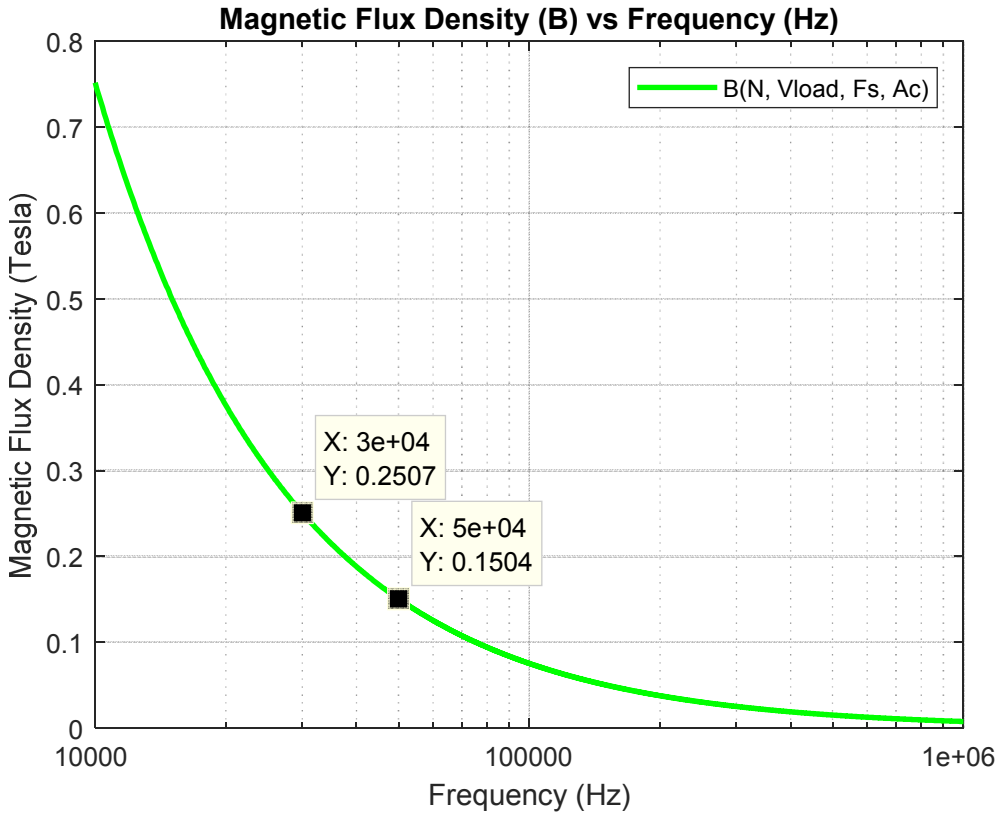


Figure 4-12: EE55 flux density (Tesla) vs frequency (Hz)

Shown in Figure 4-13 is core losses as simulated in EPCOS Ferrite Magnetic Design Tool® for the E55 transformer as a function of frequency at two different temperatures. The power losses of ferrites are usually calculated based on the amount of ferrite material (volume in m³) and gives the power loss in Watts per volumetric area. For the EE55 core used, the total volumetric area (for both core-halves) is 48444.9 mm³.

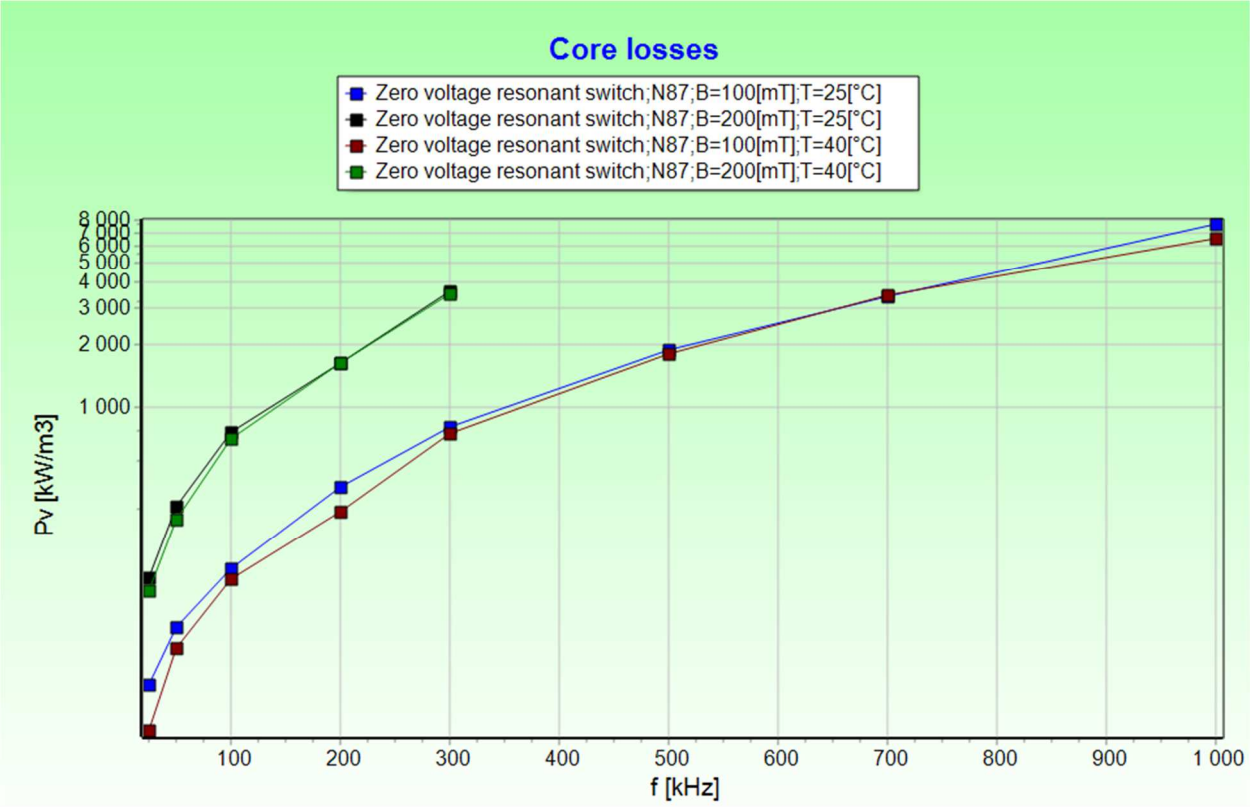


Figure 4-13: ZVS core losses (kW/m³) vs frequency (Hz)

A data-point is selected and the value is simply multiplied with the volumetric area to obtain the core loss in kilowatts. Note that because transformer core losses are highly dependent on temperature, flux swing density and frequency, it is difficult to predict the exact value of the core losses and therefore it is recommended to estimate it for the nominal operating point at which the converter will operate most of the time. Core-losses in the LLC resonant converter is not constant.

Table 4-1: Estimated transformer core loss (ZVS)

Transformer Core Parameters	Item
Switching Frequency	50-kHz
Saturation B [mT] @ Freq	0.15 T (flux swing)
Total Core Volume (mm³)	48444.9 mm³
Loss @ B[mT] & Freq	300 kW/m³
Power Loss @ 1-kW	14.54 W

Figure 4-15 illustrates the effect temperature has on the core losses for different frequencies and flux densities. At higher temperatures, the ferrite is more energy-efficient but the copper losses of the transformer will increase due to the copper having a positive temperature coefficient. Temperature also has a significant influence on the relative permeability of the air-gap as shown in Figure 4-15. It can also be observed that even the slightest addition of an air-gap will stabilize the permeability over a wide temperature range (s refers to air-gap in the figures). The effect of calculation error for core permeability (assuming a temperature of 25 °C) is negligible for an air-gap of 0.55 mm as shown in Figure 4-15.

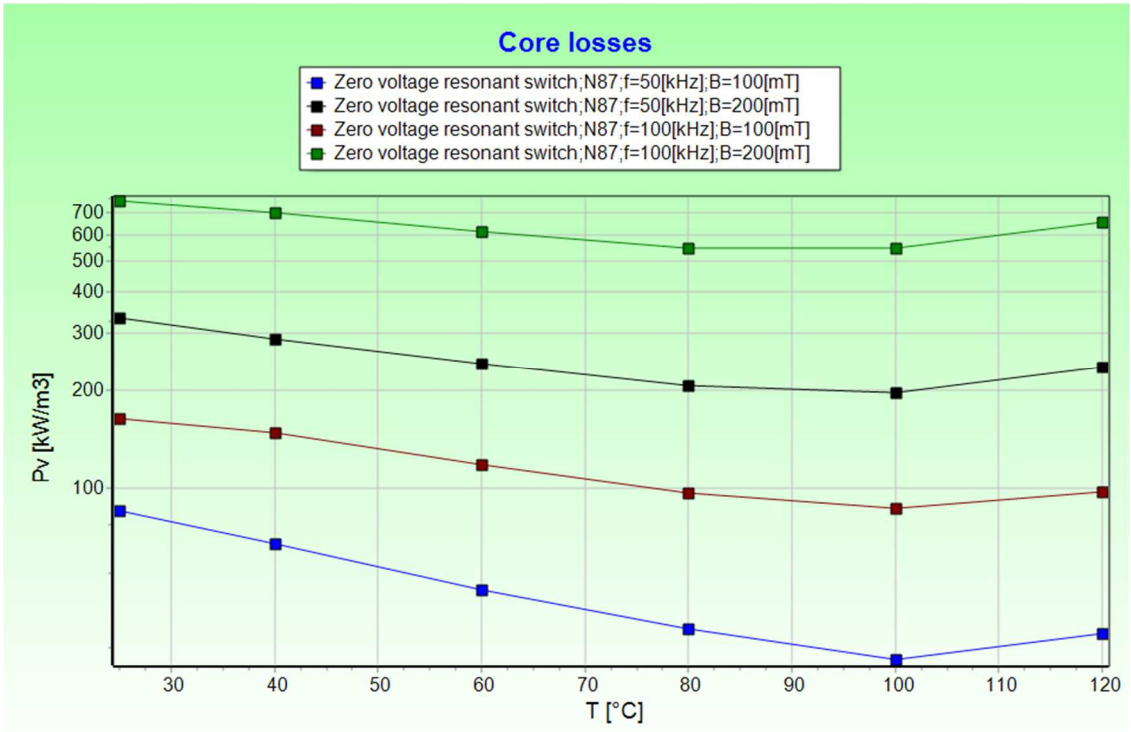


Figure 4-14: Core loss (kW/m³) vs temperature (°C)

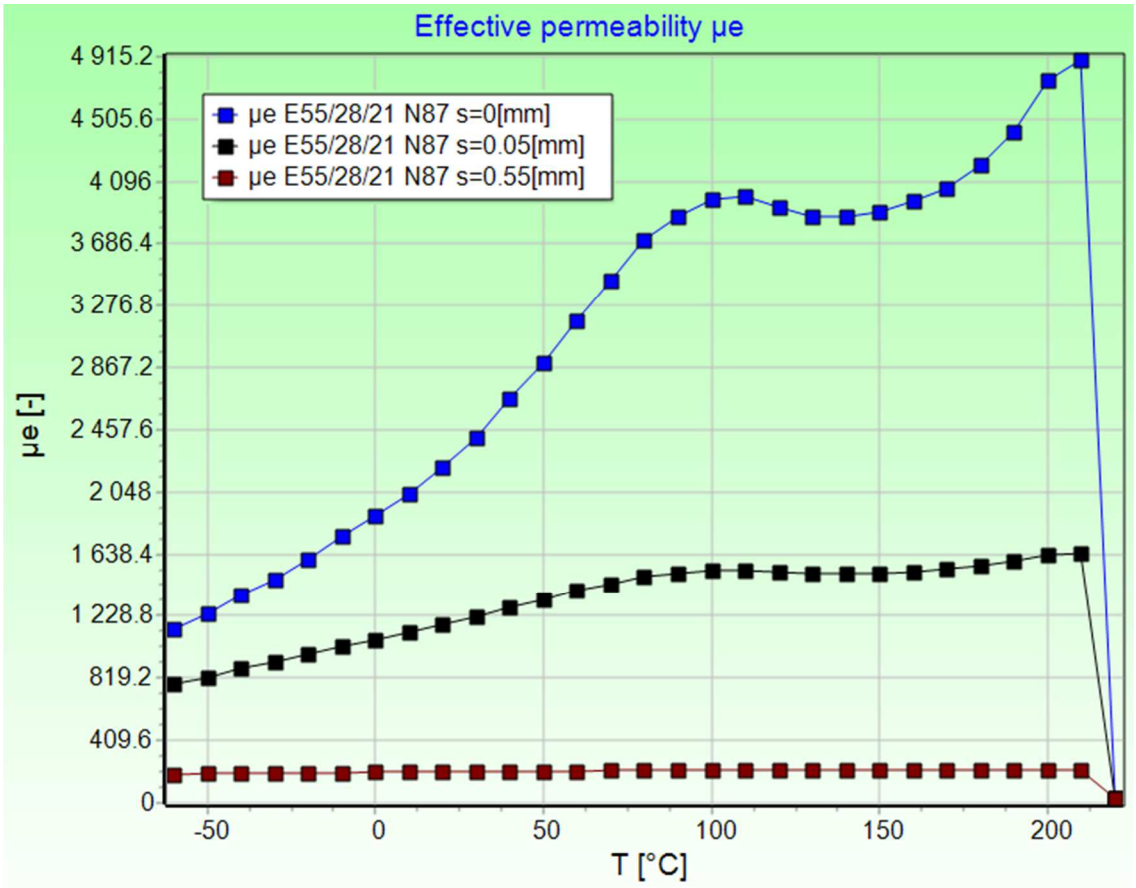


Figure 4-15: EE55 effective permeability vs temperature

4.1.6 Component Losses (ZVS)

The efficiency of the circuit has been determined by simulating the component losses such as the transformer core losses, the copper losses, the MOSFET conduction and switching losses, measured in LTspice® and verified using (4.6), the gate driver losses, using (3.18), and the diode switching losses. Diode switching losses can be obtained by multiplying the diode's forward voltage drop (V_f) with the RMS current and can be verified in simulation. Table 4-2 provides a breakdown of each component loss.

Table 4-2: Component losses (ZVS)

Component	Qty	Loss Per Item (W)	Total Loss With Diodes (W)	Total Loss With Synchronous Rectification (W)
Gate Driver	4	0.14	0.56	0.56
L_r + L_m Coil (Np Coil)	1	2.75	2.75	2.75
Transformer Ns Coil	2	1.73	3.45	3.45
HV MOSFET (80°C)	4	3.37	13.48	13.48
Transformer Core Loss	1	14.54	14.54	14.54
Output Diodes	2	13.034	26.068	N/A
Synchronous Rectification MOSFETs	2	2	N/A	4
Total Loss (W)	N/A	N/A	60.848	38.78

Table 4-3 gives an indication of the efficiency of the power converter with diode and synchronous rectification by taking into account all the losses listed in Table 4-2 as measured in LTSpice®. It can be seen that upgrading the diode rectification circuit shown in Figure 3-6 to synchronous rectification will greatly improve the efficiency performance of the power converter.

Table 4-3: Predicted efficiencies (ZVS)

Efficiency by Design	Pin	Pout	Theoretical Efficiency (%)
Diode Rectification	1060.848	1000	94.26
Synchronous Rectification	1038.78	1000	96.27

Component losses are shown in Figure 4-16 and Figure 4-17. The gate driver losses were not simulated but were calculated in section 3.1.2 as 0.14 W per driver using (3.18). This includes the switching losses caused the MOSFET's internal capacitances and internal gate resistance. For this reason, there is no need to include the switching losses a second time in calculation and the conduction loss can be calculated as $I^2 * R_{ds(ON)}$ where I is the RMS current for each MOSFET. It can be seen that the output diodes represent the highest power loss. Therefore it can be concluded that synchronous rectification will be advantageous to the efficiency of the circuit.

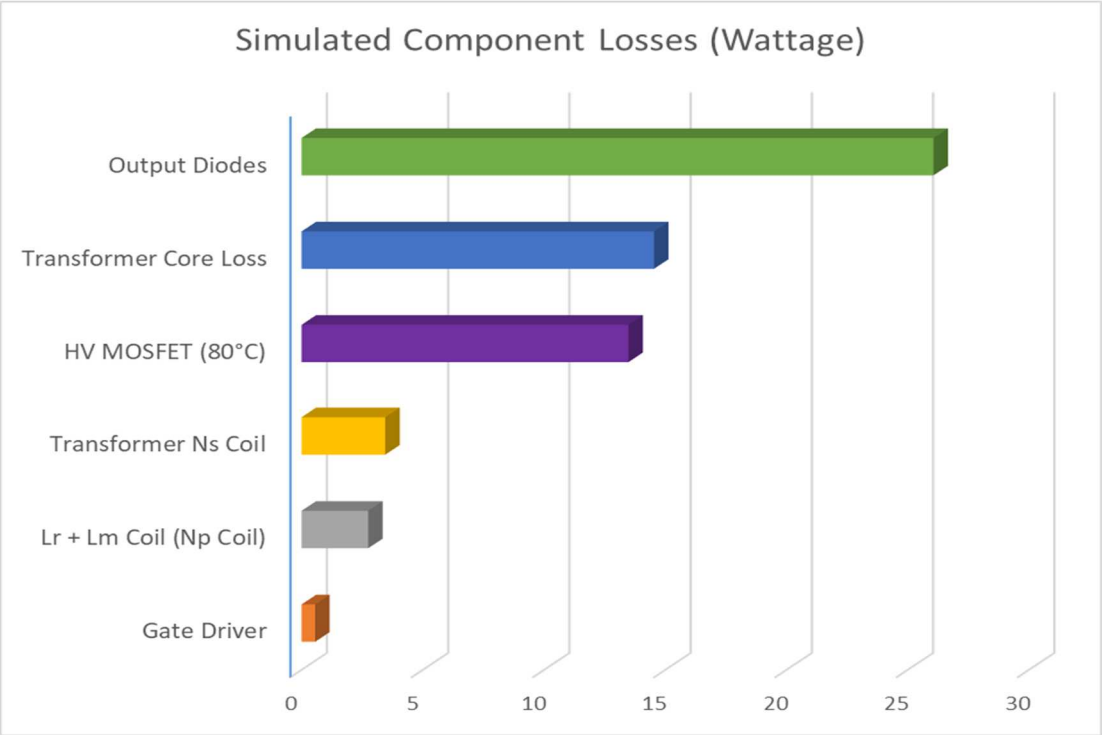


Figure 4-16: Simulated losses with ZVS (bar chart)

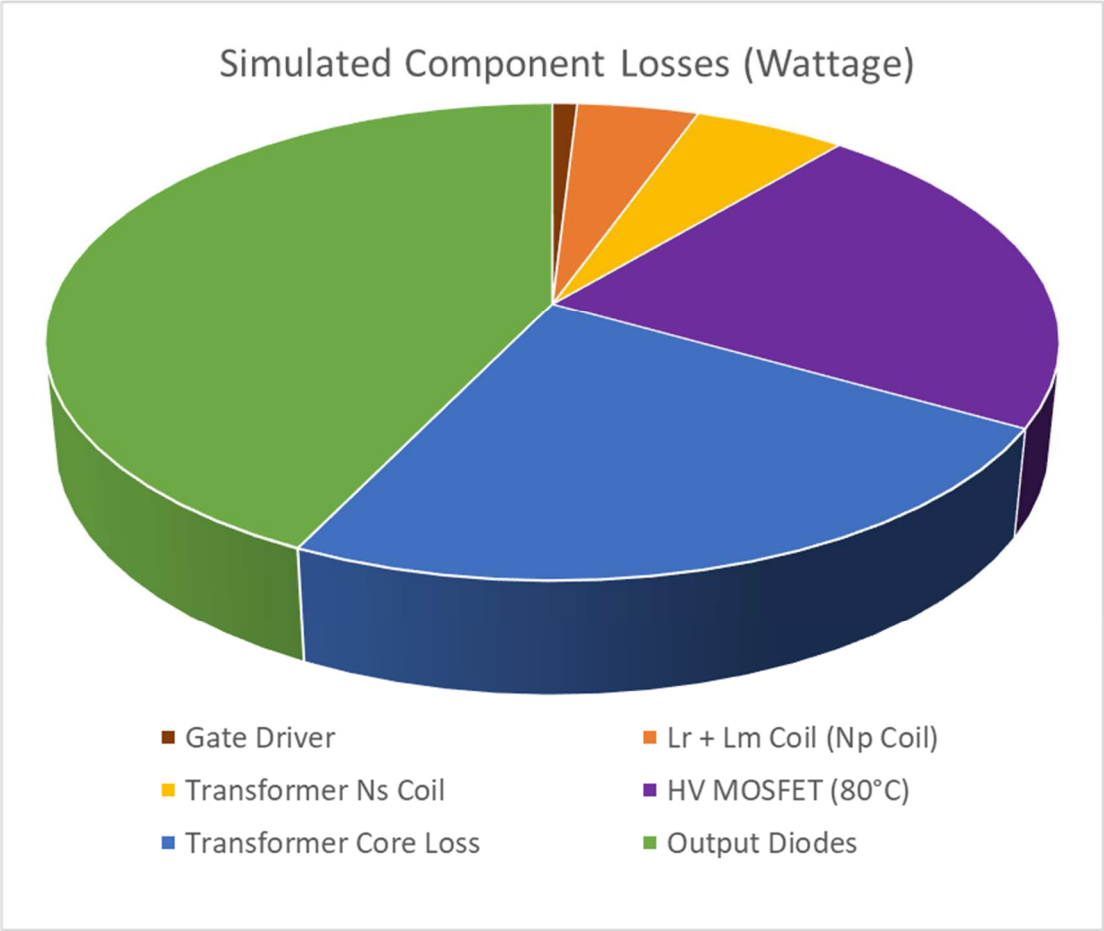


Figure 4-17: Simulated losses with ZVS (pie chart)

4.2 The Hard-Switching Converter

The hard-switching converter were simulated in LTspice® for its higher accuracy and simulation speed. It is known from the literature that this kind of converter have high switching losses caused by inductive voltage spikes. Snubber circuits are used to clamp the voltage levels down to below 600 V per MOSFET to prevent a MOSFET failure. The switching electronics are the same as for the LLC resonant converter, except the IXTH48N65X2 MOSFETS were replaced with IPW60R099CP MOSFETS due to significantly lower parasitic output capacitances.

In the hard-switching converter, timings are not critical because this converter makes use of a varying duty cycle PWM signal which operates at a constant frequency. This is in direct contrast to the resonant converter which makes use of a varying frequency with a constant duty cycle and dead time.

4.2.1 Circuit Simulation (LTspice®)

The hard-switch converter makes use of dissipative RC snubber circuits (shown as R12 to R18 and C4 to C10). The RC snubbers placed across each MOSFET makes use of a resistor and capacitor to limit the turn-off voltage spike down to below 600 V to prevent a component failure. Three additional RC snubbers are placed across each coil of the transformer to supress inductive ringing which can cause EMI.

Shown in Figure 4-18 is the circuit that was simulated, including the snubber circuits. The power loss in each snubber can be measured by measuring the power loss in each resistor of the snubber. A DC blocking capacitor (Cblock) is also included in the hard-switching converter to remove the DC components of the PWM waveforms supplied to the power transformer as the transformer does not operate well with DC components. The addition of the DC blocking capacitor will also help to prevent a continuous DC current in the event of a MOSFET failure.

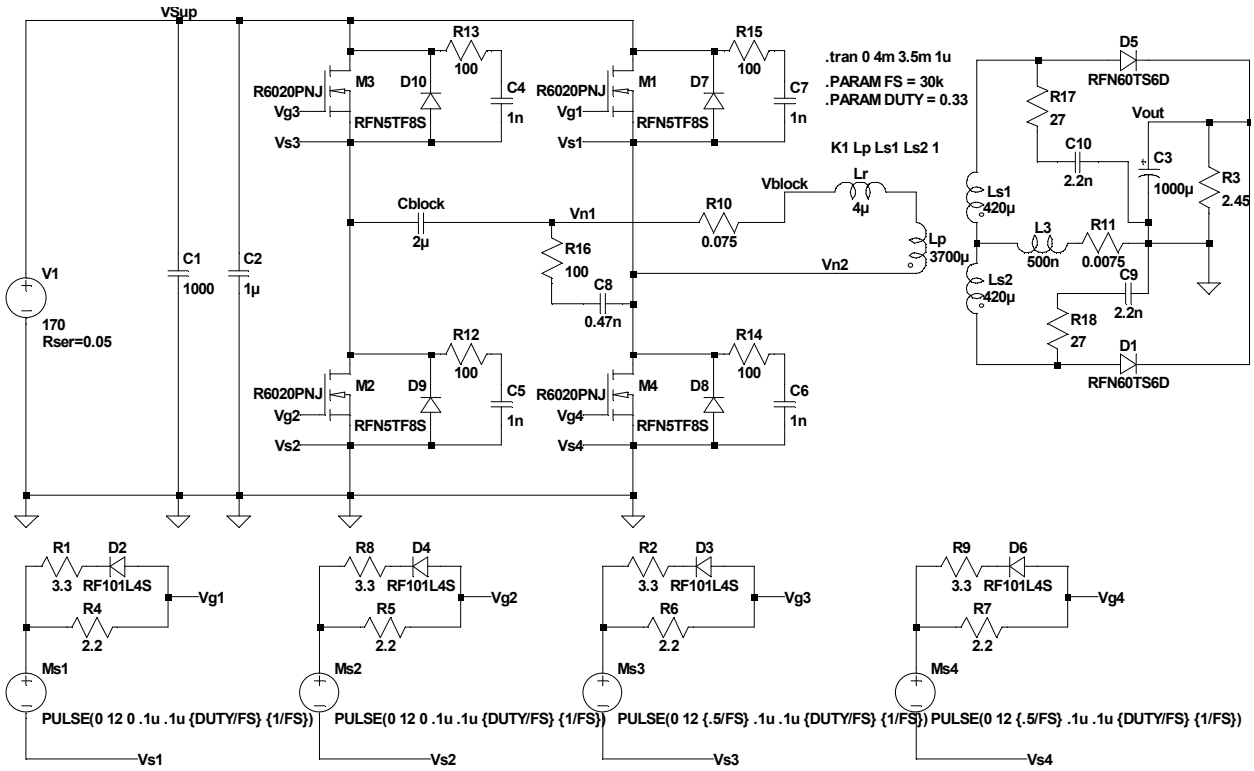


Figure 4-18: Hard-Switch converter model

Shown in Figure 4-19 is the simulated waveforms that were measured across the MOSFET (M1) of the circuit shown in Figure 4-18. The current waveform (red) flowing through the MOSFET internal body diode (including the externally added drain-source connected diode) reaches peak values of up to 18 A while the current flowing through the junction of the MOSFET while it is in the on-state (violet) also reaches peaks of up to 18 A. This is below the MOSFET rating and is still safe.

The areas encircled in yellow is where the body-diode of the MOSFET enters reverse-recovery due to energy being released from the parasitic inductances. This small current will flow through the MOSFET body-diode instead of the MOSFET junction to protect it from a voltage spike. This is the mode of operation that can cause the MOSFET to latch-up by causing an internal current to leak onto the gate pin and activate the parasitic BJT that is present inside of the MOSFET. If the rate of change is too quick (over 50 V/ns), the MOSFET may be damaged, even if the voltage and current ratings are not being exceeded. The externally added fast-recovery diodes (D7 to D10) helps to minimise the conduction time to prevent a shoot-through from occurring.

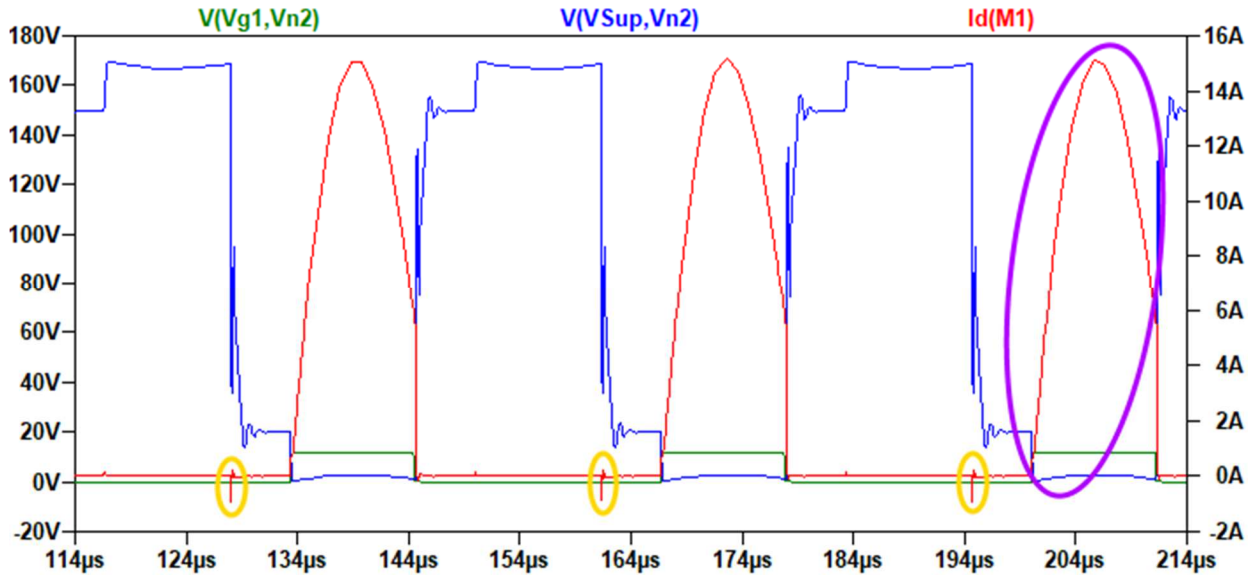


Figure 4-19: M1 voltage and current waveforms

It can be seen from Figure 4-20 that the MOSFET (M1) does not switch on at zero voltage because the gate waveform (green) switches on before the drain-source voltage (blue) of the MOSFET falls down to zero. The voltage ringing (yellow in Figure 4-20 below) that occurs on the drain-source pin after the MOSFET has been switched off is also indicative that not all the energy stored in the parasitic inductances has been recovered. The body diode can therefore be seen to enter reverse recovery mode after the turn-off event.

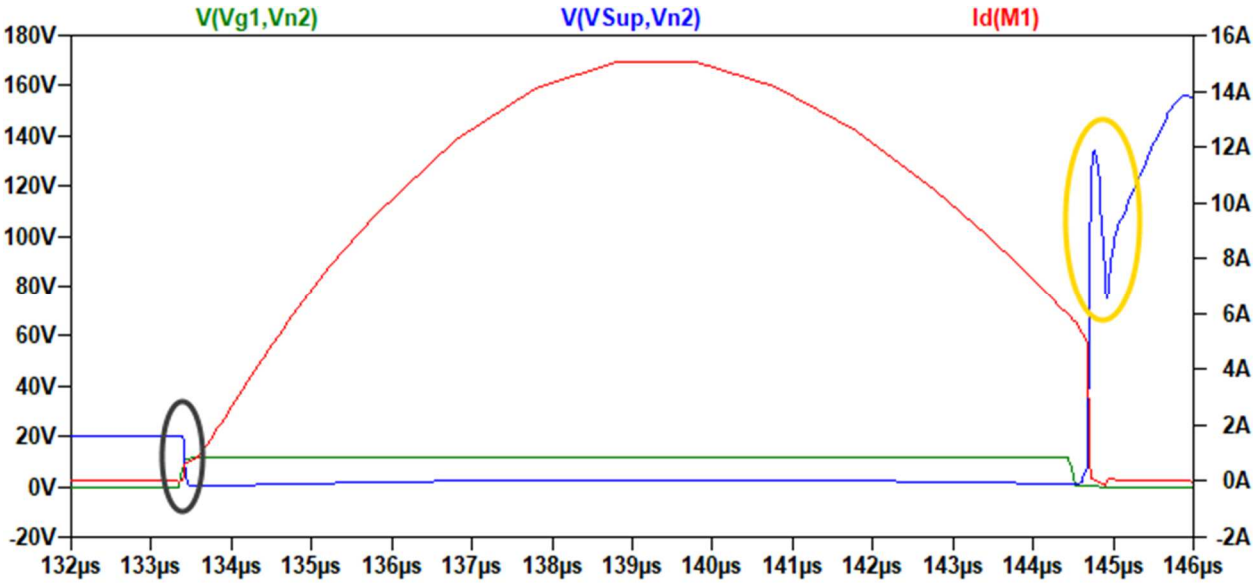


Figure 4-20: M1 Hard-Switching

MOSFETs M1 and M2 work together while M3 and M4 shown in Figure 4-18 work together. The waveforms for MOSFET M1 and M2 will look the same and is not shown separately because the waveforms lie on top of each other, making it difficult to distinguish between them. The same is true for M3 and M4. Figure 4-21 shows the gate waveforms for M1 and M3 (green and red) and

their corresponding drain-source waveforms (blue and gold). As can be seen, the voltage spikes occur on all MOSFETs as well as the absence of zero voltage switching.

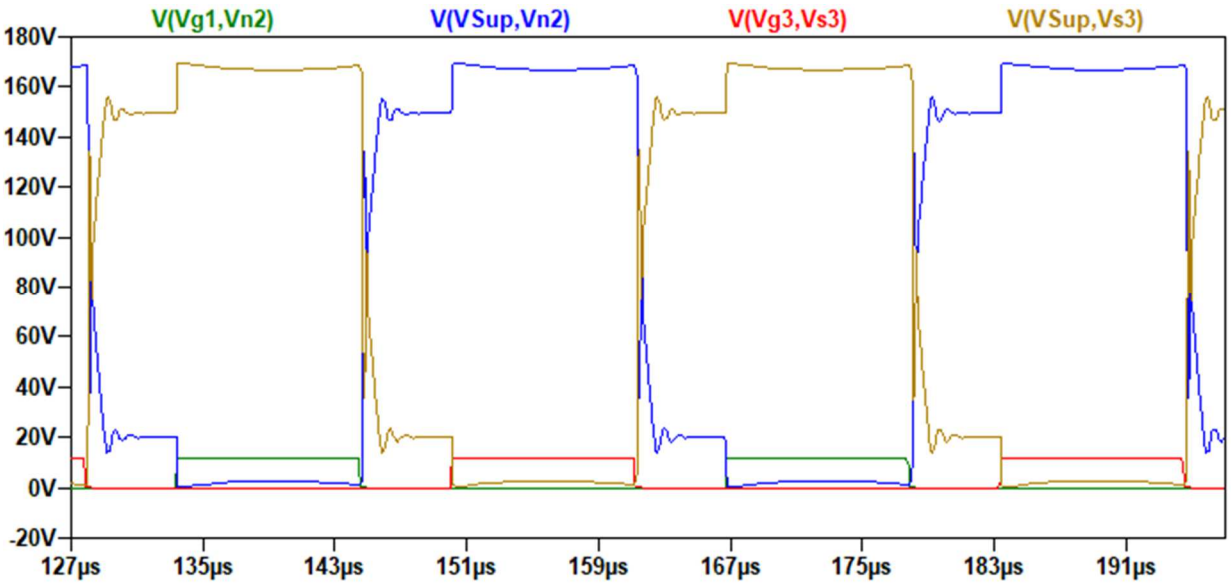


Figure 4-21: M1 and M2 Hard-Switching

The gate voltage (green), drain-source voltage (blue) and drain current (red) waveforms of M2 are shown in Figure 4-22. The current flows through the junction of the MOSFET in a forward direction (hence the positive value) while it is in the on-state. Current will flow in the reverse direction (through the body diode) both when the MOSFET switches off and when a complementary MOSFET (such as M1) switches off.

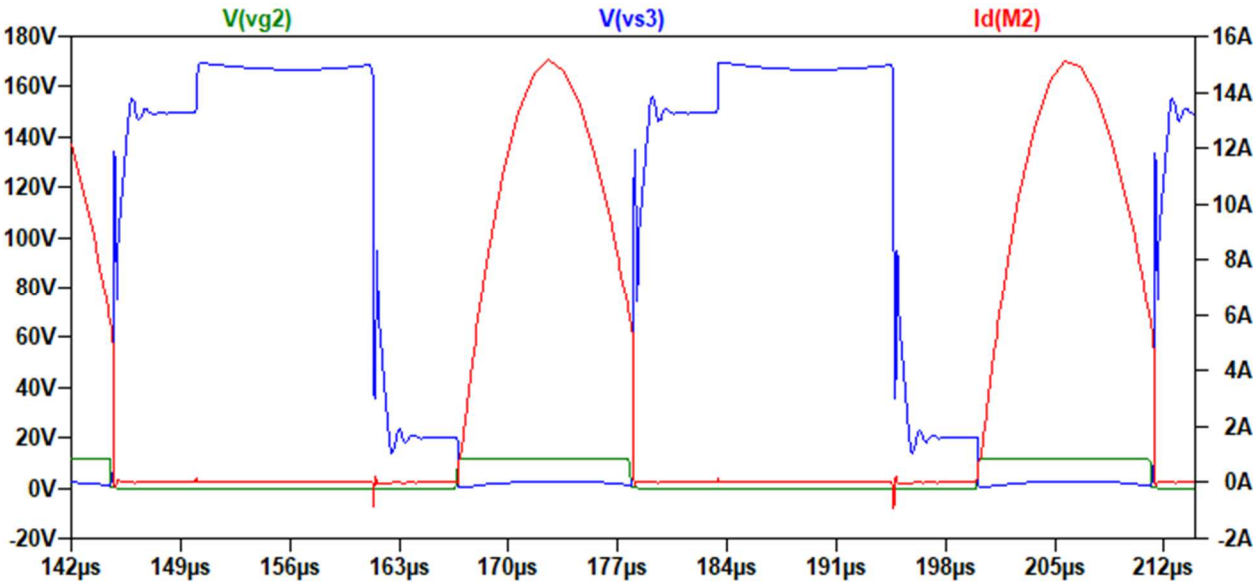


Figure 4-22: M2 voltage and current waveforms

Exceeding the rate of voltage change (not necessarily the magnitude) of a MOSFET can lead to a device failure as fully described in section 2.1.2.3. To ensure the dv/dt rating of M2 (as specified

in the datasheet) is not exceeded when M1 switches off, consider the waveform shown in Figure 4-23 which shows the slope of the voltage change in Figure 4-24.

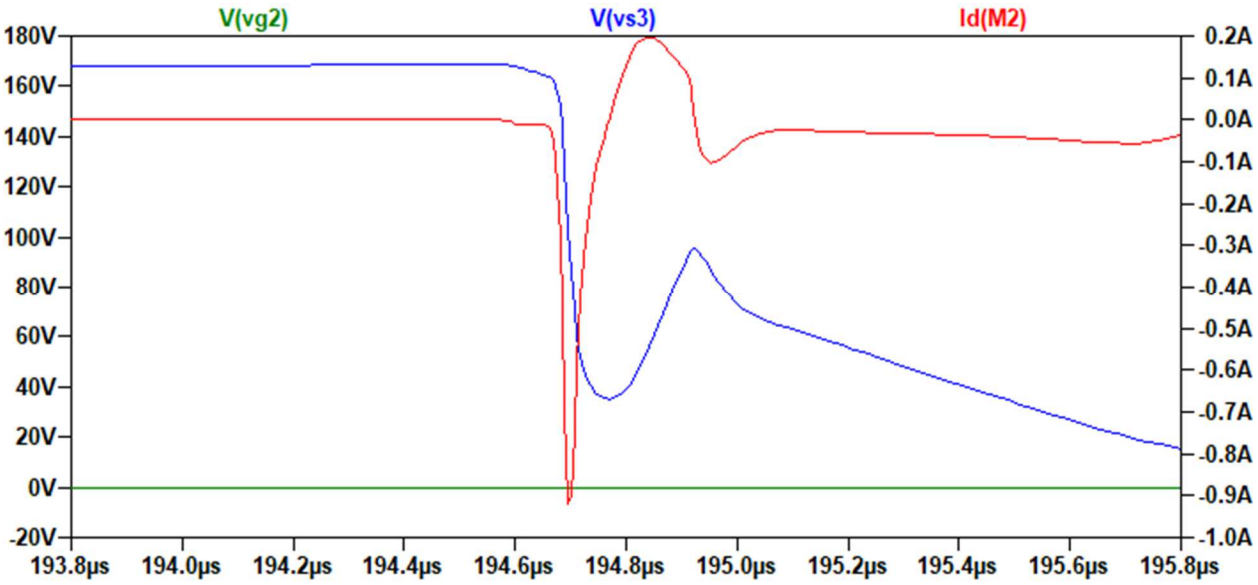


Figure 4-24: Body-diode reverse recovery action

To calculate the rate of change (dv/dt) shown in Figure 4-23, take the highest and lowest voltage of the drain-source transient and divide it by the time change. The dv/dt for M2 during a switching transit of M1 is then calculated as follow:

$$\mathrm{dv/dt} = \frac{V_{High} - V_{Low}}{T_2 - T_1} = \frac{160 - 40}{730 - 670} = 2\ \mathrm{V/ns} \tag{4.7}$$

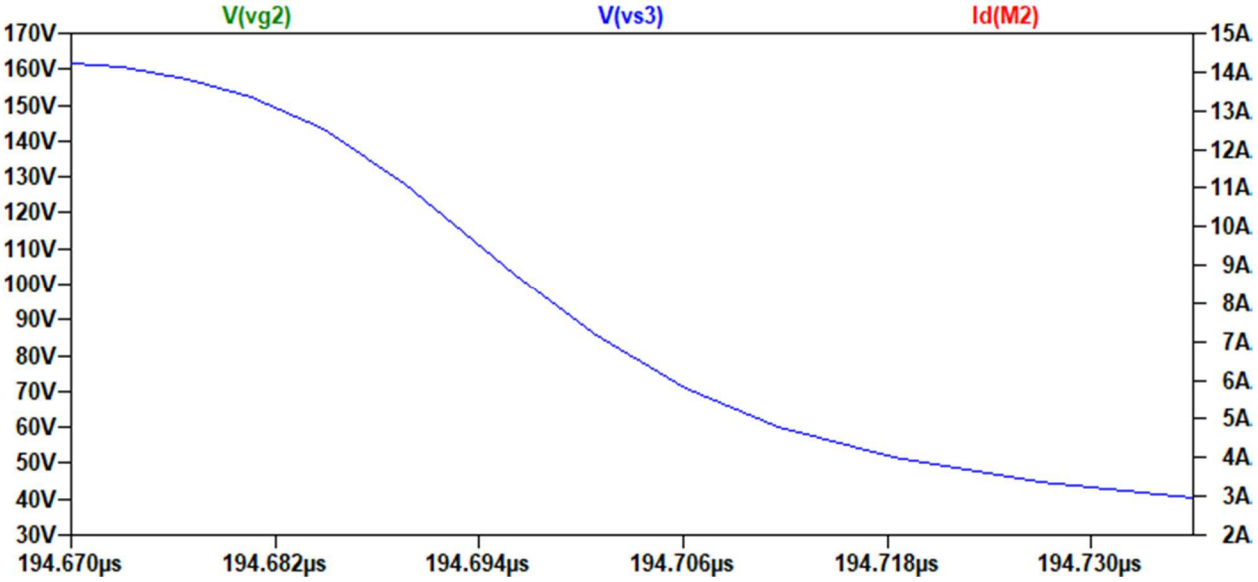


Figure 4-23: M2 diode reverse-recovery time

Leakage inductance on the primary side of a transformer also affects the secondary side and vice versa. This inductive spiking that causes the diodes to hard-switch during the turn-off cycle (when they enter reverse recovery mode) can also be seen on the current waveforms of the secondary side rectification diodes as shown in Figure 4-25. This also causes higher switching losses in the rectification diodes. Peak currents reaches up to 45 A during full-load, even though the RMS current is only 20 A.

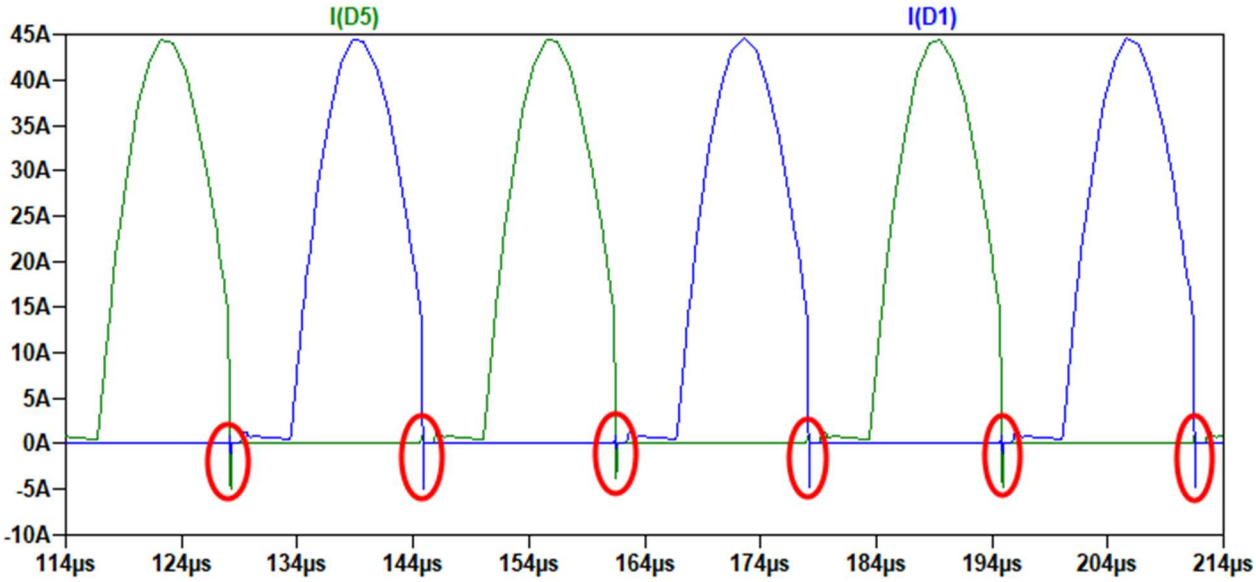


Figure 4-25: Rectification diode current waveforms

The voltage and current waveforms at the primary side of the transformer (Figure 4-26) were also measured to verify that the DC-blocking capacitor is of the correct value. The voltage drop across the DC-blocking capacitor (red) is below 30 V during full-load. All current supplied to the transformer flows through the DC-blocking capacitor (green). Inductive spiking across the transformer can also be seen (blue), but is greatly reduced due to the passive RC and RCD snubber circuits placed across each MOSFET and transformer coil.

The reverse recovery currents seen in the hard-switching converter is absent in the resonant converter because the resonant converter recovers all the energy stored in the parasitic inductances. This is also the reason why no EMI supressing components such as snubber circuits are required. Reliability is also greatly impacted in the hard-switching converter because components will heat very rapidly due to the voltage spikes.

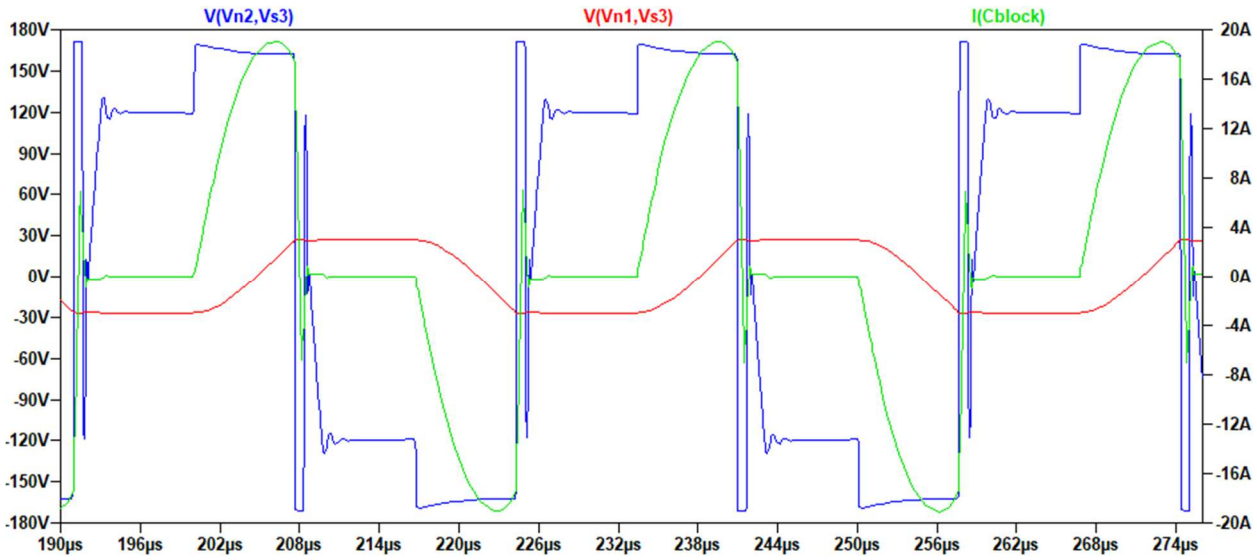


Figure 4-26: Transformer primary side voltage and currents

Figure 4-27 below shows the output voltage (green) and power (blue) waveforms. Ripple voltage during a full-load condition is approximately 300 mV, however voltage ripple alone is not an indication of a power converter's performance in terms of efficiency and reliability.

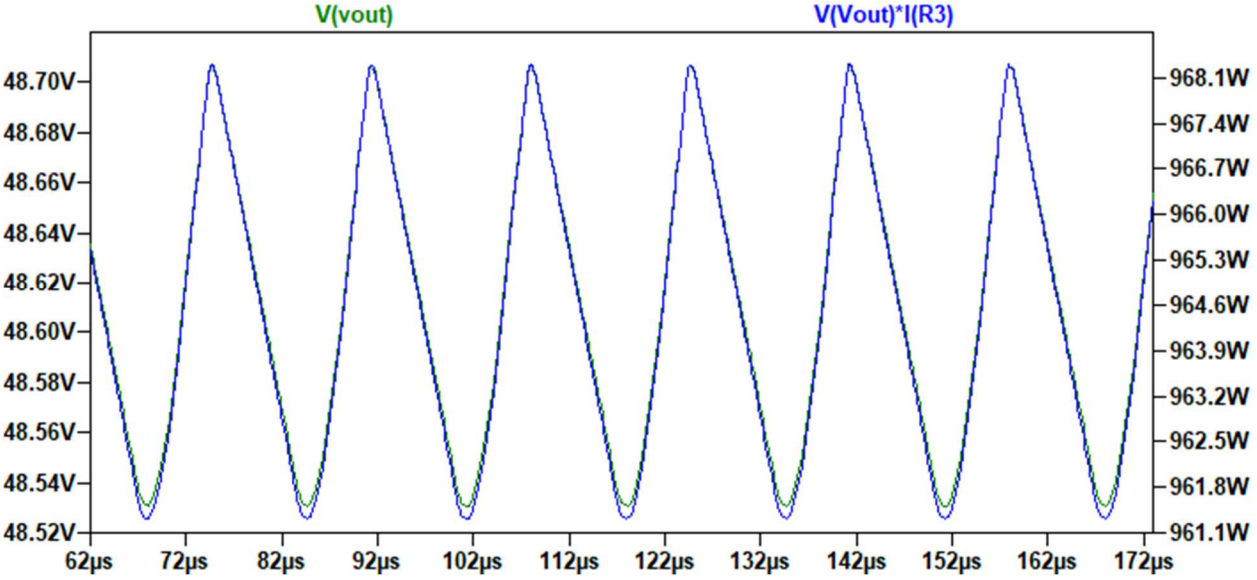


Figure 4-27: Output voltage and power

4.2.2 Transformer Utilization (Hard-Switching)

In the full-bridge hard-switching power converter, the transformer has no air gap in order to maximise the effective magnetizing inductance. Maximum flux density is easier to calculate because the core will only be used at a constant switching frequency, however the actual flux density in the core during operation may not be exactly as expected. This can be due to the presence of DC currents as well as other harmonics caused by the non-sinusoidal current waveforms. In this kind of converter the core is also more prone to flux walking which is a phenomenon that occurs when the next switching cycle takes place without removing all the energy stored in the core. This can happen if one coil is slightly longer than the other or has a different inductance due to the winding dimensions. The coils are wound on top of each other, so the most outer coil can have a different leakage and magnetising inductance than the inner coil. During a full-load condition, the core may slowly "walk" into saturation because not all the energy is recovered before the next switching cycle. After a few consecutive switching cycles (if the core did indeed walk into saturation) the converter may short-circuit because a saturated core will appear as a short circuit to the MOSFETs that generate the switching waveforms. The resonant converter is less prone to this because it recovers all the stored energy in each switching cycle.

Magnetic flux density (B) for the EE65 core is shown in Figure 4-28 as 0.12 T at 30-kHz. Magnetic flux density is a function of the number of windings (N), input voltage (V_{in}), switching frequency (f_s) and the cross-sectional area of the core (A_c). This means in the full bridge converter, the flux swing (ΔB) can be up to 0.24 T as calculated in section 3.2.1.

Shown in Figure 4-29 is the core losses for a transformer that uses N87 ferrite while operating is a hard-switching mode. Even though this is not a push-pull converter (transformer having two windings on the primary side with a centre leg), the transformer excitation is still the same. At 30-kHz the equivalent core loss will be 250 kW/m³. The total volume of the EE65×32.8×27.4 core is 87392.9 mm³. This results in a 21.85 W power loss when the transformer is operating at full capacity at 25 °C. Core losses will be lower at a higher temperature but the copper losses will increase rapidly with a temperature rise as copper has a positive temperature coefficient. The parameters used for calculating the core-losses are shown in Table 4-4.

Table 4-4: Estimated transformer core loss (Hard-Switching)

Transformer Core Parameters	Item
Switching Frequency	30-kHz
Saturation B [mT] @ Freq	0.25 T x 2
Total Core Volume (mm³)	87392.9 mm³
Loss @ B[mT] & Freq	250 kW/m³
Power Loss @ 1-kW	21.85 W

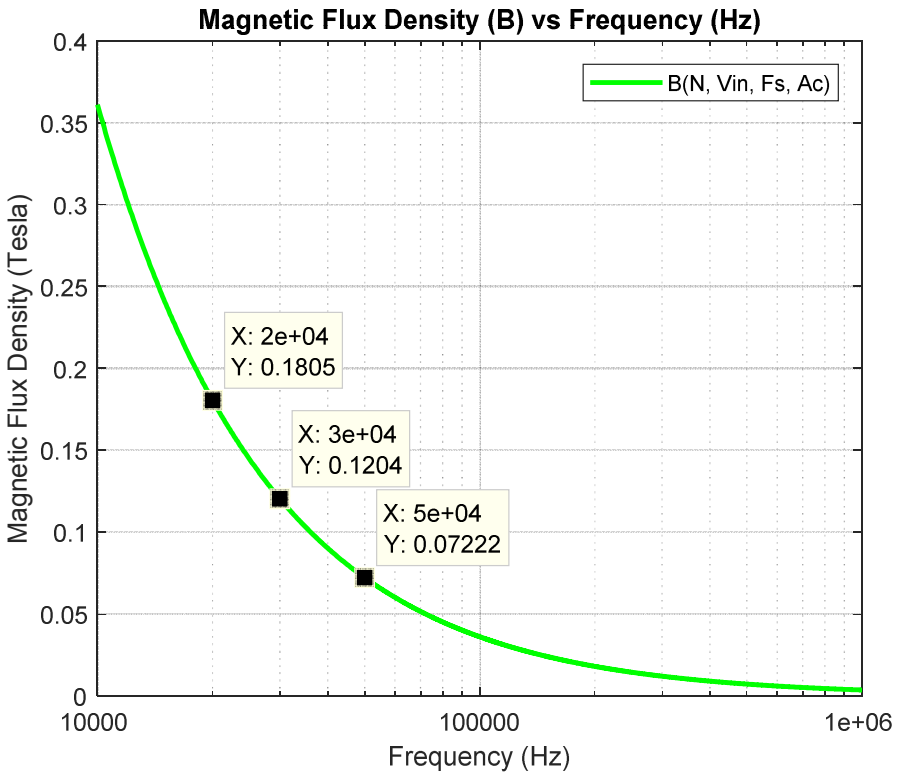


Figure 4-28: EE65 flux density (Tesla) vs frequency (Hz)

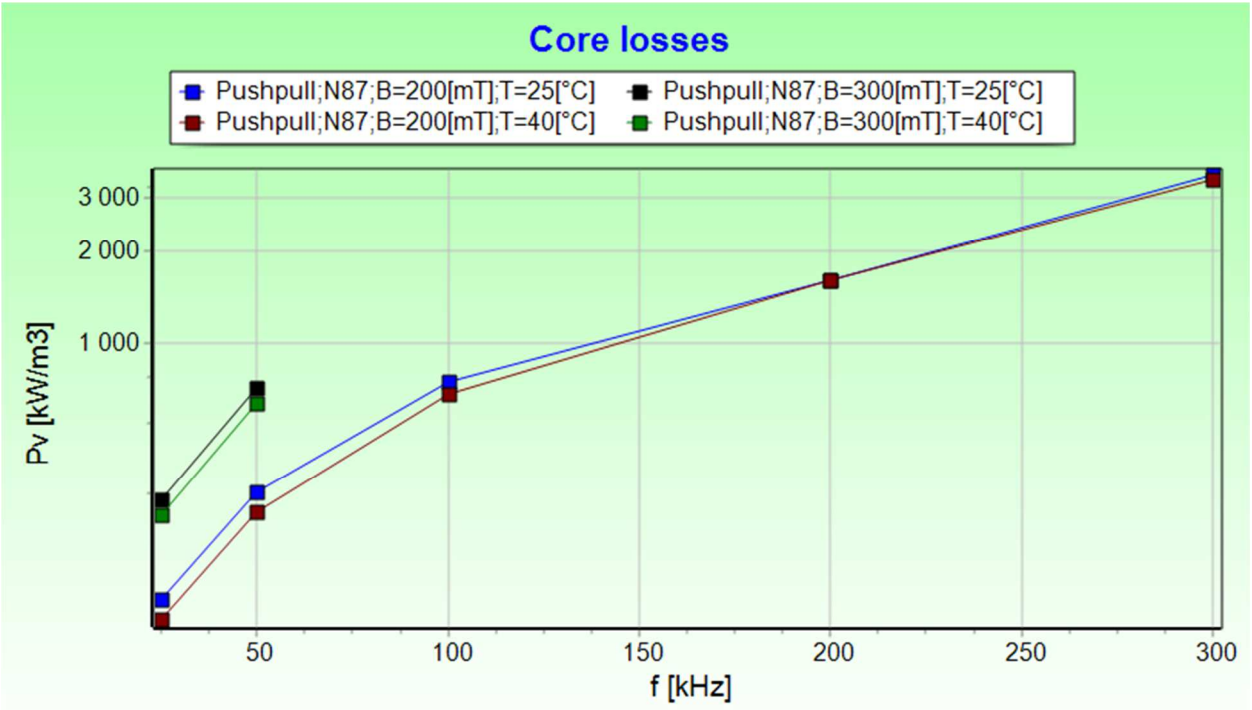


Figure 4-29: Hard-Switching core losses (kW/m³) vs frequency (Hz)

The stability of the effective permeability in a larger transformer core are more sensitive to an air-gap and will cause a larger error in calculated vs measured inductance due to the presence of a small but unwanted air-gap. The permeability of N87 ferrite is 2200 (at 25 °C), but drops to 1700 when a small air-gap of just 0.02 mm is added as seen in Figure 4-30. Some core manufacturers will amend the permeability (as was the case for this particular EE65 core) to compensate for a small air-gap that may be present due to surface roughness or thickness of the glue joint where the EE halves are joined together. The more windings there are on the core, the bigger the inductance error will be due to the air-gap because the inductance is determined by the AL value and the number of turns squared. For every turn of copper, the error will increase by a factor of 4 if a small unwanted air-gap is present, unless it is compensated for. The datasheet gives the permeability for the core as 1700 instead of 2200 because the manufacturer has compensated for an unwanted air-gap. It can be seen in Figure 4-30 that even with the compensation of an air-gap, the permeability is still not stable over a wide temperature range. This is in direct contrast with the resonant converter which utilises an air-gap in the core for higher stability.

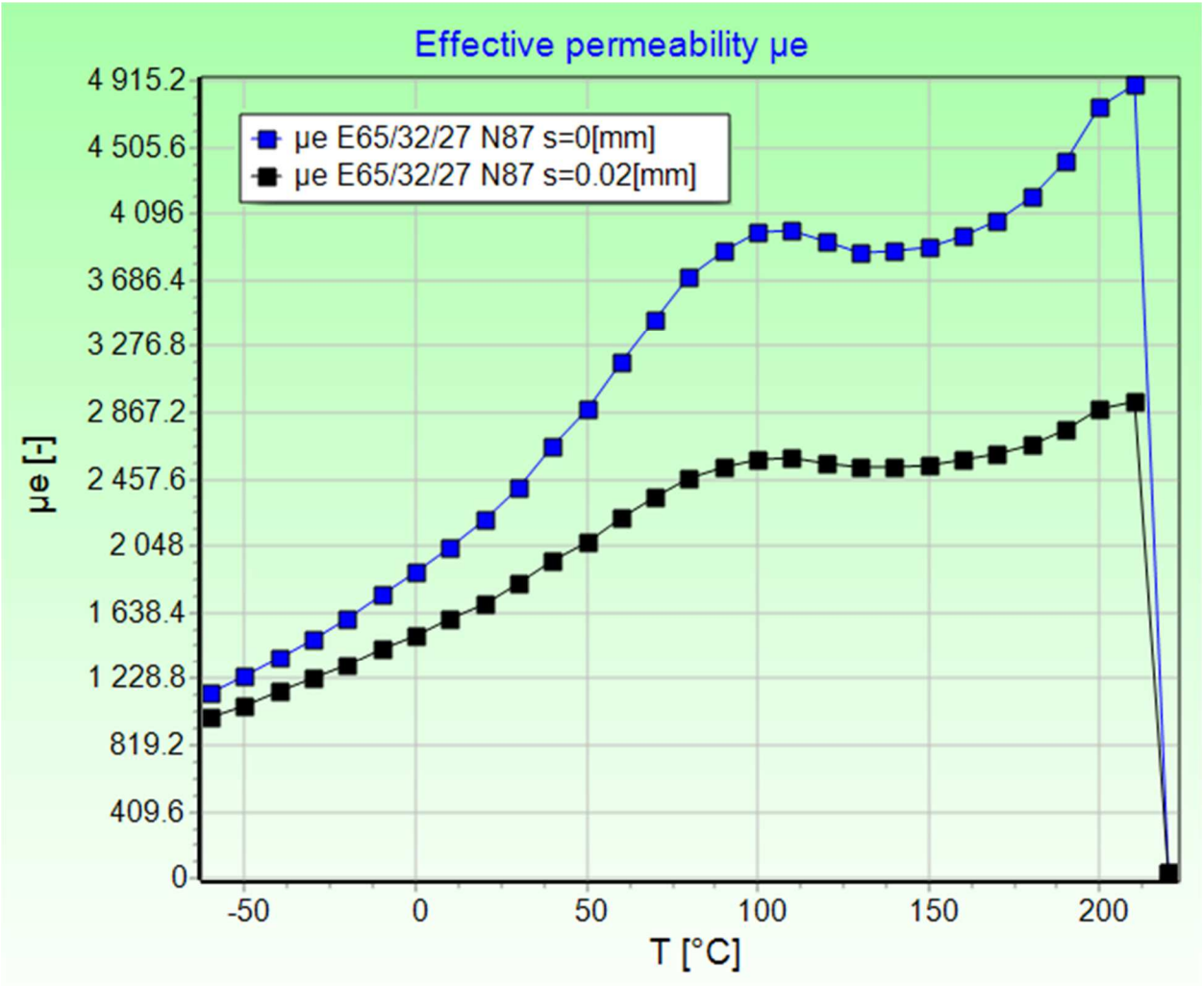


Figure 4-30: EE65 effective permeability vs temperature

4.2.3 Component Losses (Hard-Switching)

The hard-switching converter makes use of additional circuitry such as snubber circuits that assist in the reduction of EMI and transient voltage spikes. They are placed in parallel to the drain-source pin of each MOSFET as well as across each transformer coil. This leads to an additional power loss but will in turn help to prevent a larger switching power loss in each of the MOSFETS. It is preferred to select the snubber resistor so that the ringing frequency and oscillations are critically damped. This was however not possible as the power loss would increase dramatically and require resistors capable of dissipating over 10 W of power. The circuit was therefore simulated and a snubber resistance was chosen to damp the oscillations enough to prevent large transient spikes that will exceed the MOSFET voltage ratings. Due to the snubbers not being able to critically damp the circuit, synchronous rectification would not be possible on this kind of circuit since the oscillations will not trigger the synchronous rectification MOSFETs at the right times.

The larger ferrite core (E65) used in this converter has almost twice the volume of ferrite (87392.9 mm³) in the core than the E55 core (48444.9 mm³) and therefore requires a low switching frequency to keep the core loss to a minimum. The output diode losses were about the same as in the resonant converter, but the high voltage MOSFETS has almost twice the power losses and therefore will require forced air cooling during a full-load condition.

Table 4-5: Component losses (Hard-Switching)

Component	Number	Loss Per Item (W)	Total Loss (W)
Gate Driver	4	0.14	0.56
Transformer Ns Coil	2	3.35	6.7
Lr + Lm Coil (Np Coil)	1	7.7	7.7
Snubber Circuits	7	N/A	9.9
Transformer Core Loss	1	21.84	21.84
Output Diodes	2	14.4	28.8
HV MOSFET (80°C)	4	7.8	31.2
Total Loss (W)	N/A	N/A	106.7

Figure 4-31 and Figure 4-32 visualises the component losses as listed in Table 4-5. The high voltage MOSFETs (T_j = 80 °C) contributes to most of the losses while the gate driver circuits contributes only slightly. This is in contrast to the LLC resonant converter where the rectifying diodes have the highest losses. Table 4-6 shows the estimated efficiency during a full-load condition with the losses in Table 4-5 taken into account.

Table 4-6: Estimated efficiency (Hard-Switching)

Efficiency by Design	Pin	Pout	Theoretical Efficiency (%)
Diode Rectification	1106.7	1000	90.36

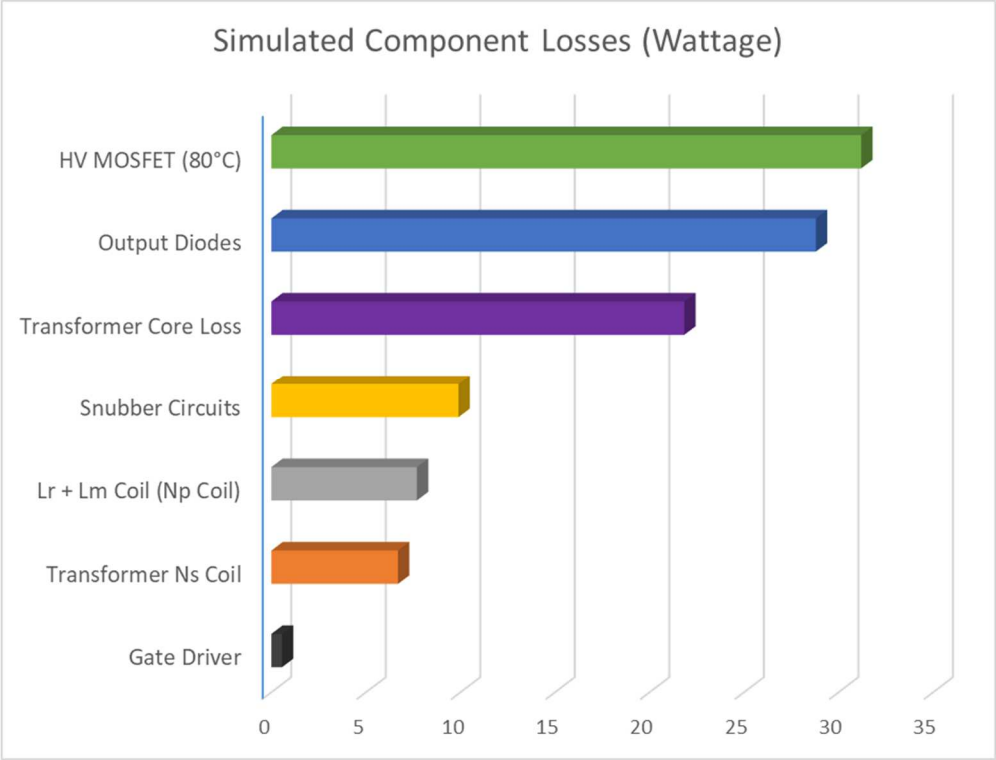


Figure 4-31: Simulated losses with Hard-Switching (bar chart)

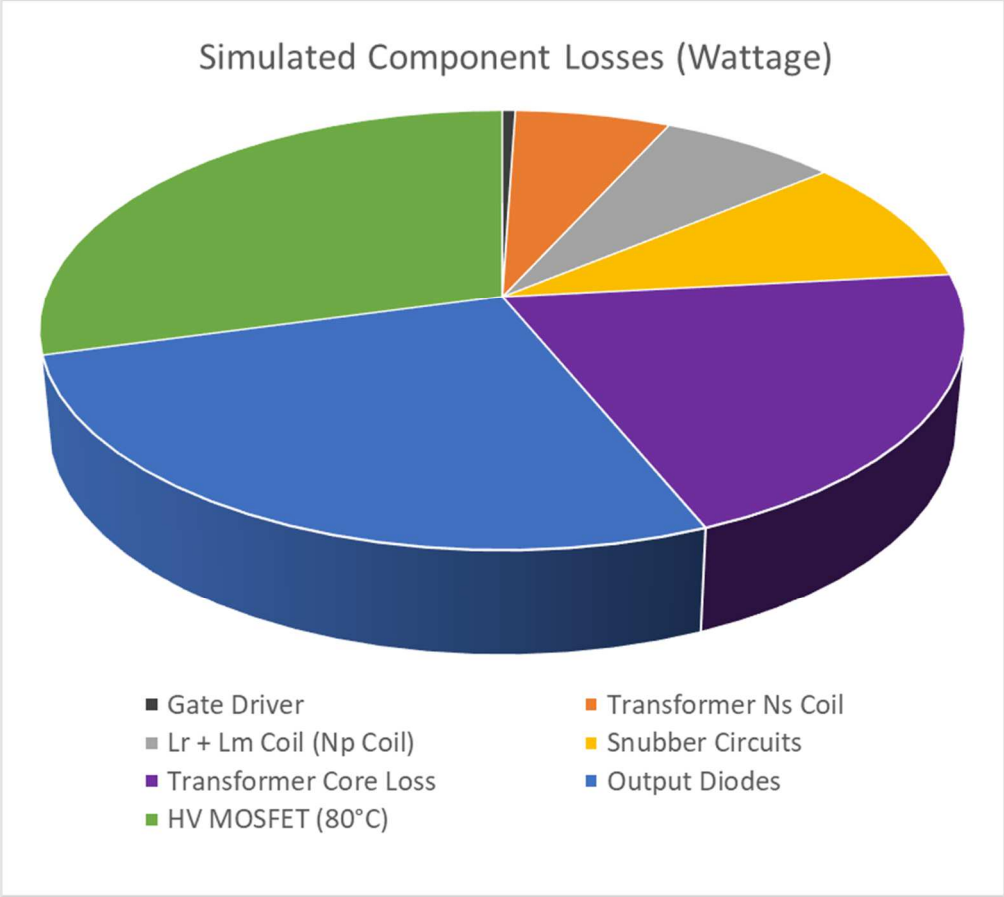


Figure 4-32: Simulated losses with Hard-Switching (pie chart)

Figure 4-33 shows a comparative summary of all the losses for each power converter. It can be seen that hard switching makes use of RC snubber circuits which is not used in a ZVS converter. Diode rectification as well as gate driver losses are assumed to be the same for both hard switching and ZVS (it is assumed, but in reality it is not). It is difficult to calculate the diode losses during reverse-recovery because in DCM mode, the reverse recovery-time, reverse recovery current as well as reverse recovery power loss is dependent on the duty-cycle. Gate driver losses have been calculated for a worst case scenario using the total gate charge for the MOSFETS as given in the datasheet.

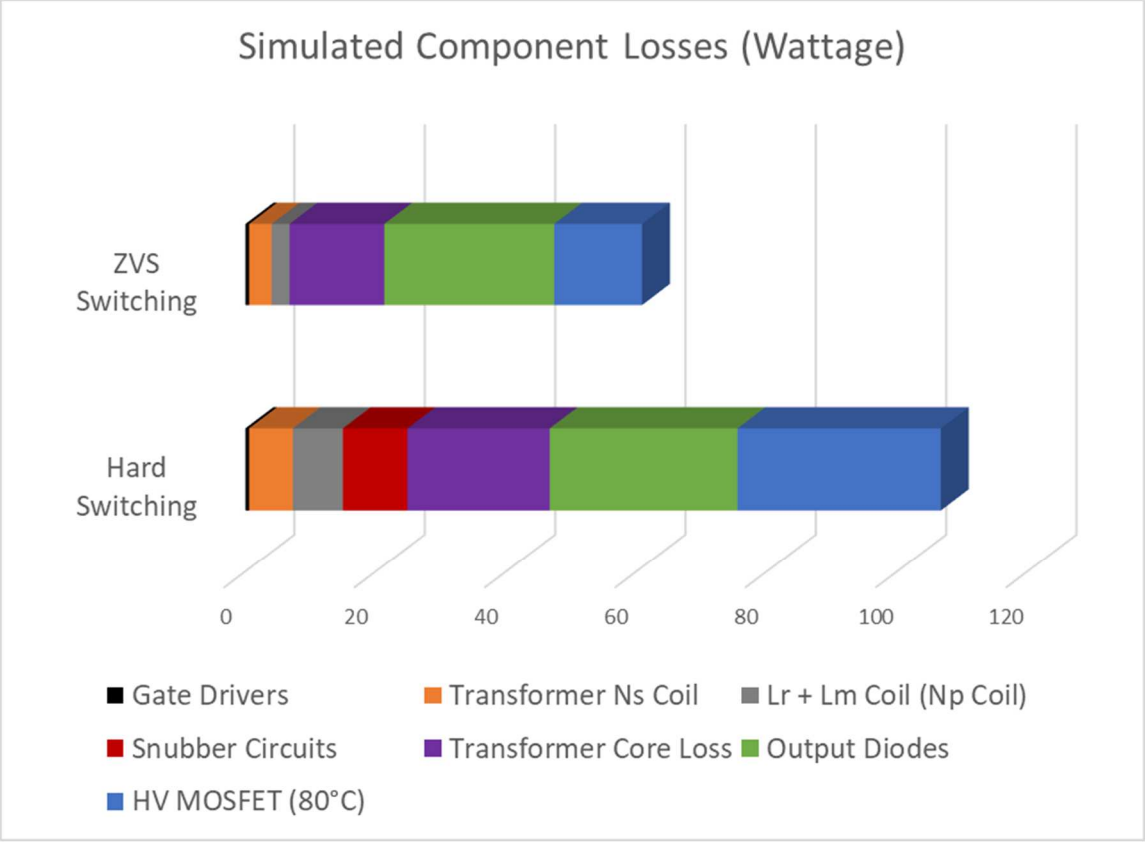


Figure 4-33: Component loss summary

4.3 Conclusion

The LLC resonant converter has a lower component count than the hard switching converter because it does not use snubber circuits. This leads to a reduction in cost. It is able to achieve soft switching on both the primary side of the converter as well as the secondary side, making it significantly more reliable (due to the absence of transient voltages and currents) and energy efficient. This is in direct contrast to hard switching where additional components (which can degrade and fail over time) are used to absorb the transients. The addition of the air-gap in the LLC resonant converter also makes the transformer's permeability more stable over a wide temperature range than hard switching which requires no air-gap. The overall higher efficiency of the LLC resonant converter, as well as its ability to operate at lower input voltages, makes it highly suitable for coupling a renewable energy source to an electrolyser.

CHAPTER 5: MEASUREMENT AND VALIDATION

This chapter presents the testing procedure and results of the two implemented converters. An adjustable three phase source was rectified to create a DC voltage source equivalent to the MPP voltage of the PV panels. A programmable electronic load was connected to each power converter during testing to mimic a resistive load. The characteristic waveforms of the ZVS converter as well as the hard switching converter were measured and compared to the simulated waveforms in order to validate the simulations and compare to the literature. The total efficiency of both systems is also measured to determine which converter is the most suitable for coupling an electrolyser to a renewable energy source. It is important to remember that this validation chapter focuses on finding the most suitable power converter for coupling a renewable energy source to an electrolyser. This does not necessarily imply that the most efficient converter is the most suitable because renewable energy sources like solar panels do not provide a constant voltage and the converter needs to be able to operate at a low input voltage to allow the electrolyser to operate (to capture and store the energy). The most suitable converter should be able to operate reliably and efficiently (hence the validation of soft-switching) and also needs to be able to cope with a dynamic input voltage range.

5.1 The Electrolyser Stack

In order to determine which converter is the most suitable, the electrolyser stack was characterised using an electrolyser test-station. Electrolysers will conduct no electrical current when the input voltage drops below a certain value – and consequently no energy storage will take place. The resistance of the electrolyser stack is also not linear and the characteristic V-I curve changes as the temperature changes, see Figure 5-1.

The power converter needs to be able to provide an output voltage of at least 35 V (independent variable that is adjusted by the power converter) to allow the electrolyser stack to start conducting. If the voltage is below this value, the stack will appear to the power converter as an open-circuit with an infinite resistance and consequently draw no current and therefore produce no hydrogen. The amount of hydrogen and oxygen (in litres) produced is directly proportional to the current drawn by the stack, multiplied with the amount of cells. A programmable electronic load will be used to emulate the load characteristics (V-I curves) of the PEM electrolyser stack as presented in Figure 5-1. Each power converter must be able to provide a minimum output voltage of at least 45 V to be able to deliver at least 1-kW of power to the programmable load without overheating or failing.

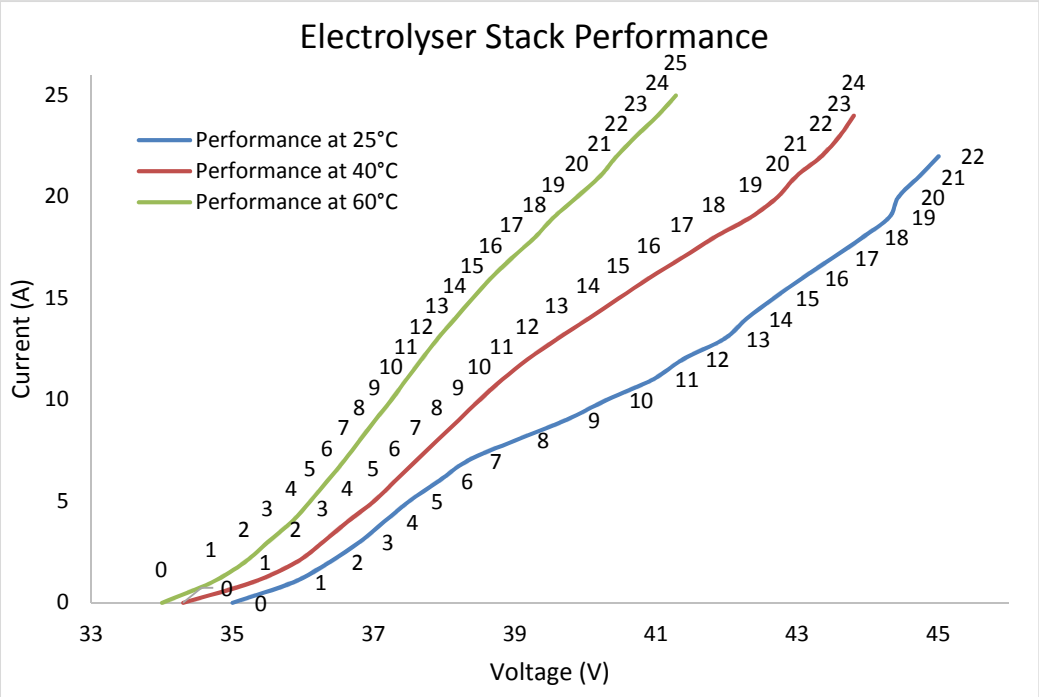


Figure 5-1: Electrolyser performance curves

Table 5-1 below shows the specifications of the electrolyser stack to be coupled to the PV array.

Table 5-1: Electrolyser stack specifications

Electrolyser Stack Specifications		
Model	Hydron EL100	
Electrolyser type	Polymer Electrolyte Membrane	
Number of Cells	24	
Rated power	4.8	kW
Power requirements	30-60 VDC / 0-150 A	
Nominal efficiency	84%	HHV
Temperature range	5-80	°C
Dimensions (HxWxD)	300 x 154 x 154	mm
Weight	30	Kg

5.2 The LLC Resonant Converter

In this section, the data from the LTspice® simulation was exported and imported into Matlab® and plotted on the same figure than the data obtained from the oscilloscope to allow an easy visual comparison. A 3-bit noise filter was applied to all oscilloscope channels to filter out any ADC noise. This improves the ADC resolution as well as the Signal-to-Noise Ratio (SNR) without affecting the measured information as would be the case with an averaging filter. It is required to visually see which signal turns on or off first and in the case of ZVS, a noisy signal will make this impossible to observe when zoomed into. This will allow zooming in to the vectorised images generated by the Matlab® script that is used throughout this chapter.

5.2.1 High-Voltage MOSFET Waveforms

Figure 5-2 indicates the locations where measurements were taken to validate the simulated waveforms. The green voltage probes indicate where the gate-source waveforms were measured, blue indicates the corresponding drain-source voltage locations and red indicates the position of the current probes. The red arrow indicates the direction of the current waveform.

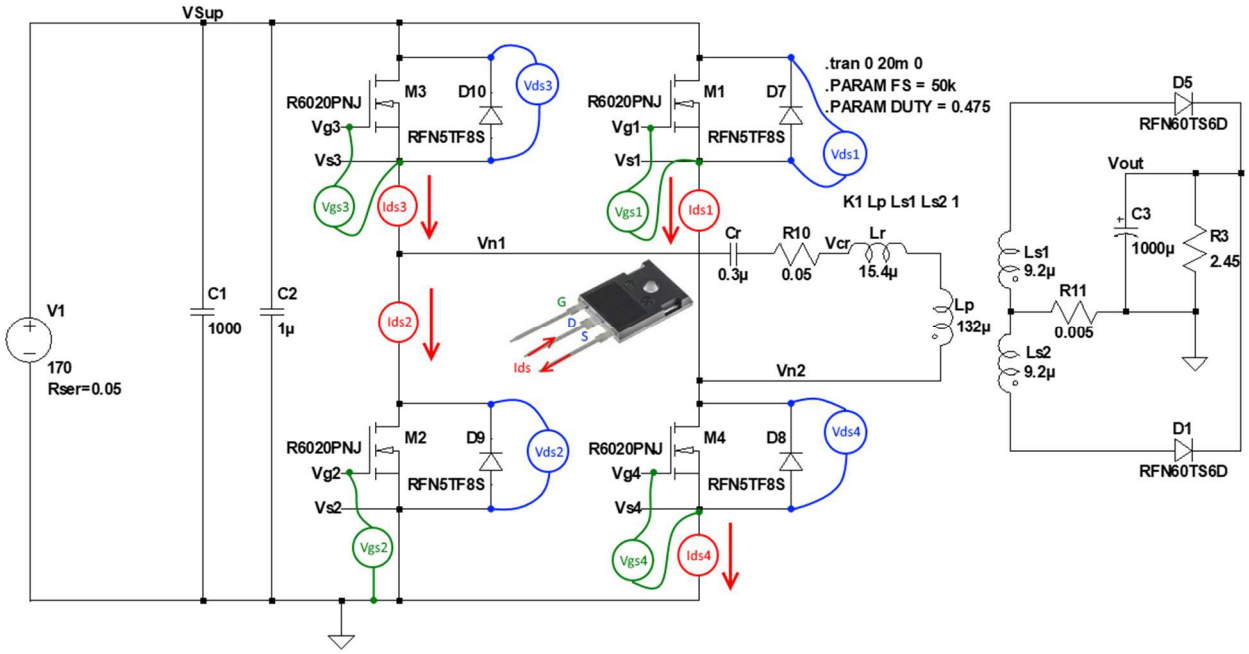


Figure 5-2: High-Voltage MOSFET measurement locations

Measurements were taken on the low side MOSFET (M2) shown in Figure 5-2 throughout this section. The waveforms for M1, M2, M3 and M4 in Figure 5-2 will look identical, except for shifting in the time domain as opposing switches do not conduct simultaneously.

Figure 5-3 shows the measured vs simulated waveform as measured at MOSFET M2. The gate voltage was measured over the gate-source pin of the MOSFET while the switching voltage was measured over the drain-source pin of the MOSFET. A current probe was placed over the drain leg of the MOSFET to measure the current. It clearly shows the absence of voltage and current transients as in the simulation. In ZVS mode of operation, the body-diode will start to conduct first, then the gate is forward biased and the current flows through the MOSFET junction instead of the body diode. At the end of the cycle, the body diode shall not conduct anymore and will not enter reverse recovery. This effect can be seen clearly in Figure 5-3 as indicated on the figure itself.

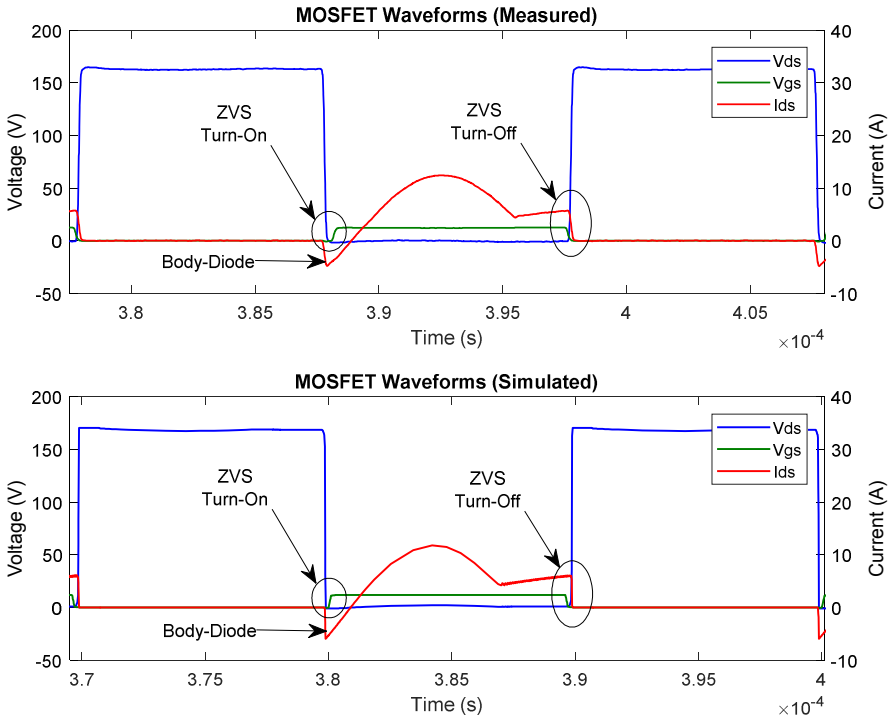


Figure 5-3: Measured vs simulated MOSFET waveforms (ZVS)

Figure 5-4 shows a zoomed-in version of Figure 5-3 where the ZVS turn-on and turn-off can be seen more clearly. It can be seen at turn-on that the body diode starts conducting first before the MOSFET is turned on.

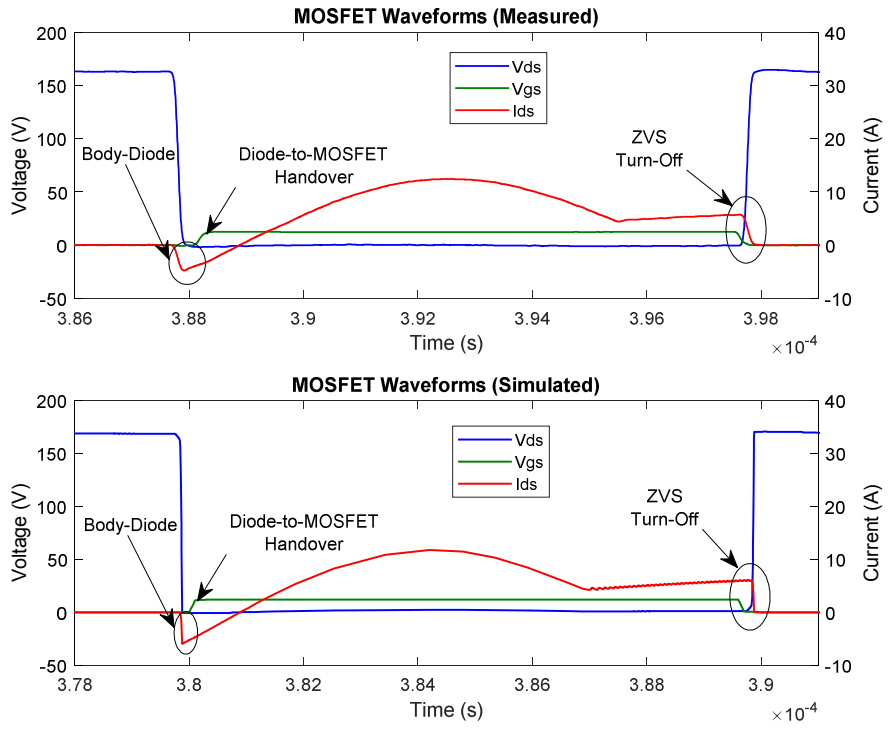


Figure 5-4: Measured vs simulated ZVS turn-off

To ensure the converter is able to achieve soft-switching over a wide input range, the input voltage supplied to the converter was changed from 170 V to 120 V. At this low voltage, the converter frequency was lowered from 50-kHz to 35-kHz. This was done to keep the output voltage steady at 48 V. Keep in mind that this is the equivalent of increasing the duty cycle in a PWM converter. The converter was able to draw up to 600 W of power while still maintaining ZVS. Output voltage dropped from 48 V to 46 V when the load was increased to 700 W but the converter still maintained ZVS. It can be concluded that the converter is able to operate reliably at low input voltages.

The input voltage was then lowered to an extremely low value of only 80 V and the frequency of the converter was changed to 30-kHz to keep the output voltage as high as possible. The electronic load was still able to draw 350 W from the converter while the converter is providing 42 V to the load. MOSFET waveforms were measured again to ensure the converter is still operating in ZVS mode. This shows that the converter will be able to deliver power to the electrolyser for a wide range of PV voltages. Thus the change in PV voltage due to shading will not cause the loss of ZVS.

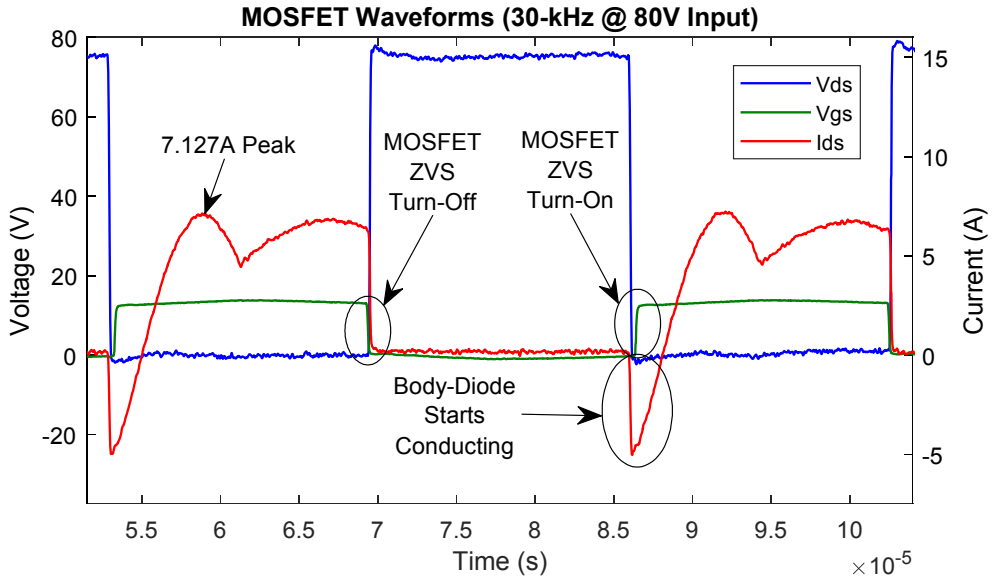


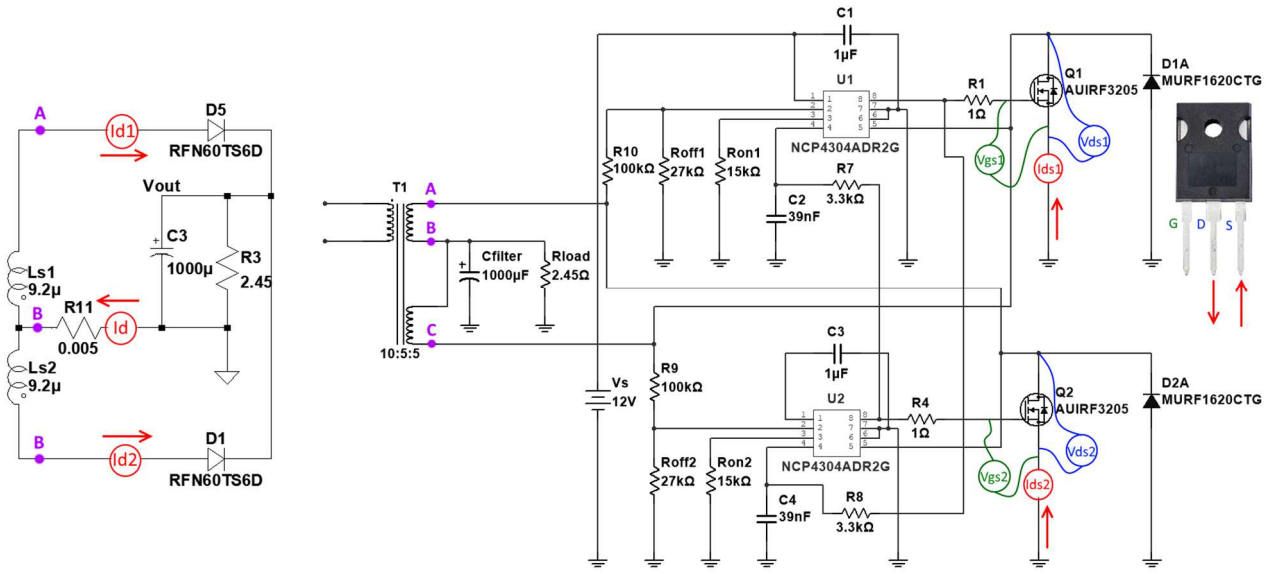
Figure 5-5: MOSFET waveforms at 80V input

As seen in Figure 5-5, the measured waveforms shows that the MOSFET is still achieving ZVS at both the turn-on and turn-off cycle. This is excellent, considering that most power converters will not be able to deliver any output at this very low input voltage.

5.2.2 Rectification Waveforms

It was decided to implement synchronous rectification to increase the efficiency of the converter. Synchronous rectification uses MOSFETs instead of diodes to convert the AC output from the high-frequency transformer back to DC. This requires that the MOSFET be turned on when the body-diode starts conducting while measuring the voltage drop over the MOSFET. When a

positive voltage of a few millivolts in magnitude is measured over the MOSFET, the controller keeps the MOSFET switched on. If this voltages drops below -1 mV, the controller switches the MOSFET off again. Two dedicated NCP4304 synchronous rectification controller ICs were used to manage this automatically. Figure 5-6 shows the rectification circuits as it was implemented, including the points where the current and voltage waveforms were measured. The equivalent circuit for diode rectification is shown in (a) while the synchronous rectifier is shown in (b) to illustrate the difference in implementation and complexity. There are no simulated results for the synchronous rectifier because there is no standard SPICE model for the NCP4304 IC in any of the software that was used. The location points marked as A, B and C shows the equivalent connection points to the ferrite transformer when swapping the diode rectifier with the synchronous rectifier for testing and measuring. To measure the diode waveforms using a single current probe, the current probe can be attached to the location marked as Id in the bottom left corner. If it is desired to measure the two diodes separately, two different current probes can be placed in the locations marked as Id1 and Id2. Note that the direction of current flow for measuring with two probes are different.



(a) Diode rectifier (b) Synchronous rectifier

Figure 5-6: Rectification measurement locations

The current waveforms (for the diode rectification) are shown in Figure 5-7 as measured over the centre leg of the transformer. This was done to eliminate the need for two different current probes. It is indicated on the figure which one of the two diodes are switching at each cycle. It can be seen that the diodes are also soft-switching because the current is always positive and never flows in the reverse direction as is usually the case when a diode is entering reverse-recovery. It can also be seen that the synchronous rectification MOSFETs are achieving ZVS while the diodes are achieving ZCS. This not only results in soft-switching at the primary side, but also the secondary side, regardless whether diodes or MOSFETS are used. Testing was done at a load of 1-kW and an output voltage of 48 V.

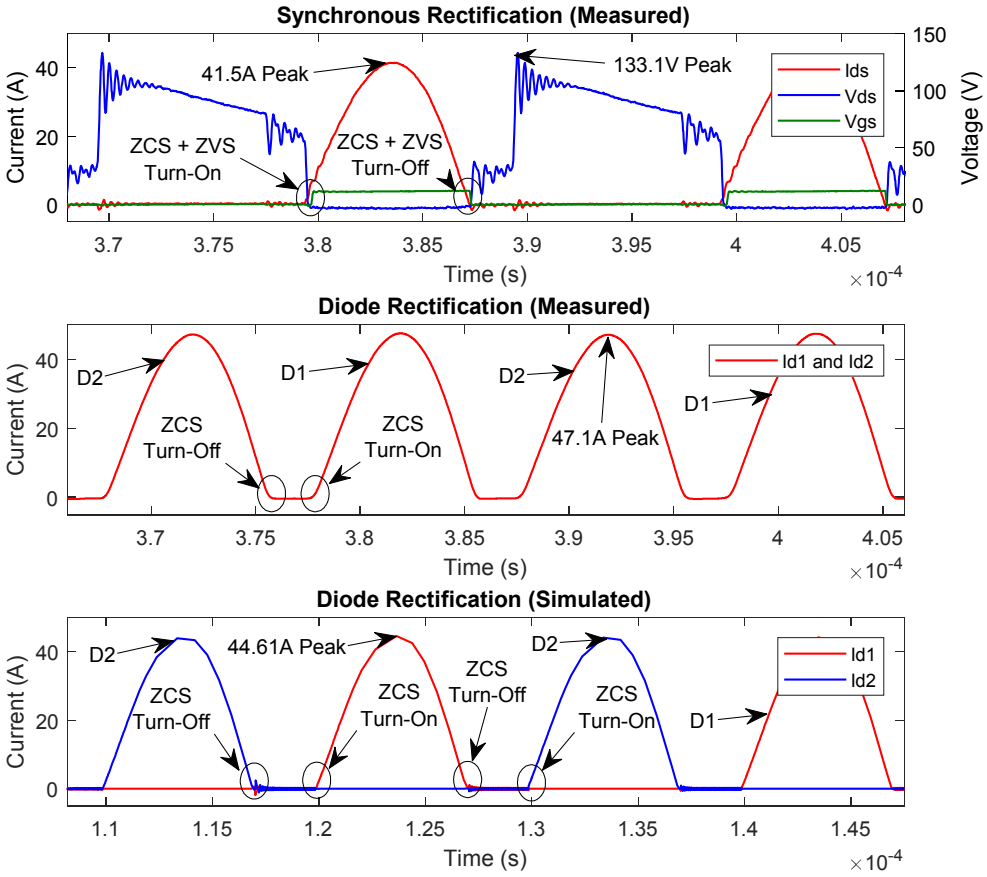


Figure 5-7: Measured rectification waveforms

Figure 5-8 shows the zoomed-in MOSFET waveform for the synchronous rectification. The body-diode starts conducting first (ZCS) which causes the voltage across it to drop to a value close to zero. Then the controller turns-on the MOSFET which causes the current to flow through the MOSFET junction instead of the diode. This increases efficiency because the turn-on resistance of a MOSFET is significantly lower and more temperature stable than that of a diode. At the end of the current waveform, the MOSFET is switched off.

It can be seen that there are voltage ringing at the drain-source of the synchronous rectification MOSFETs. This is caused by the transformer's leak-inductance at the secondary side as well as the MOSFET output capacitance. It forms a parasitic LC circuit that resonates at 3-Mhz. This is not a problem and can be minimised by using an RC snubber, however the voltage rating of the synchronous rectification MOSFETs are not exceeded (200 V) yet, so this is not a requirement.

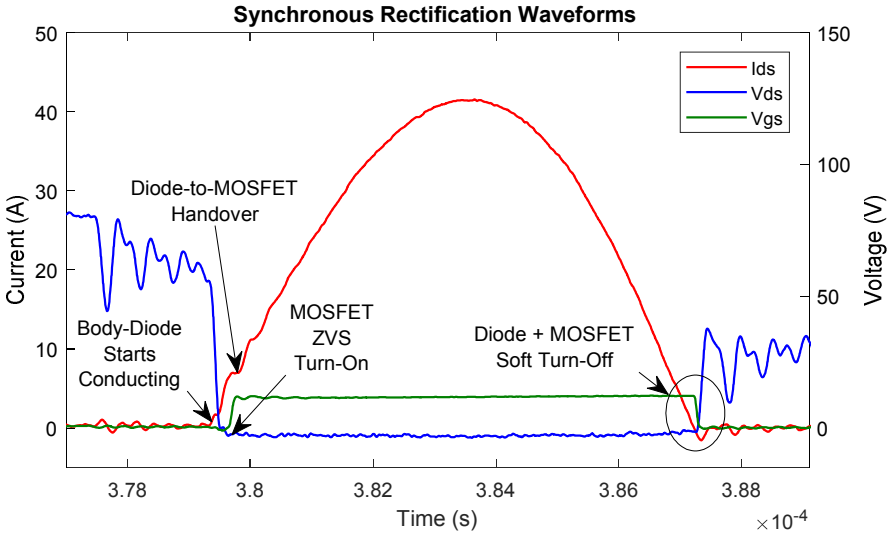


Figure 5-8: Synchronous rectification waveforms

5.2.3 H-Bridge Waveforms

Figure 5-9 shows the measurement locations where the high-voltage waveforms generated by the MOSFETs are measured. This is used to determine if the power factor is leading, unity or lagging in order to determine if the converter is operating in the capacitive (ZCS), resistive (ZCS + ZVS) or inductive (ZVS) region.

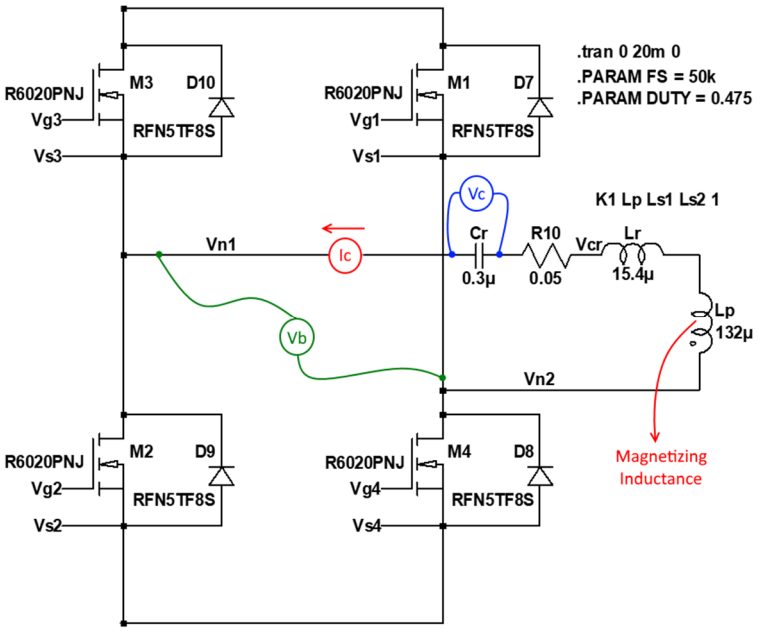


Figure 5-9: H-Bridge measurement locations

The voltage and current waveforms at the H-bridge circuit were also measured to verify that the LLC resonant converter is indeed operating in the inductive region where it will always achieve ZVS. In ZVS mode, the current will always lag the voltage waveform. This is shown in Figure 5-10 where it was measured on the actual circuit and compared with the simulated waveforms. The peak voltages over the resonant capacitor was measured at 120.9 V. It can also be seen that the converter is operating in deep Continuous Conduction Mode (CCM). This means that the current waveform is never interrupted and therefore no energy is released in the form of harmful voltage spikes. The magnetizing inductance currents can be seen, indicating that the converter can easily do more than 1-kW.

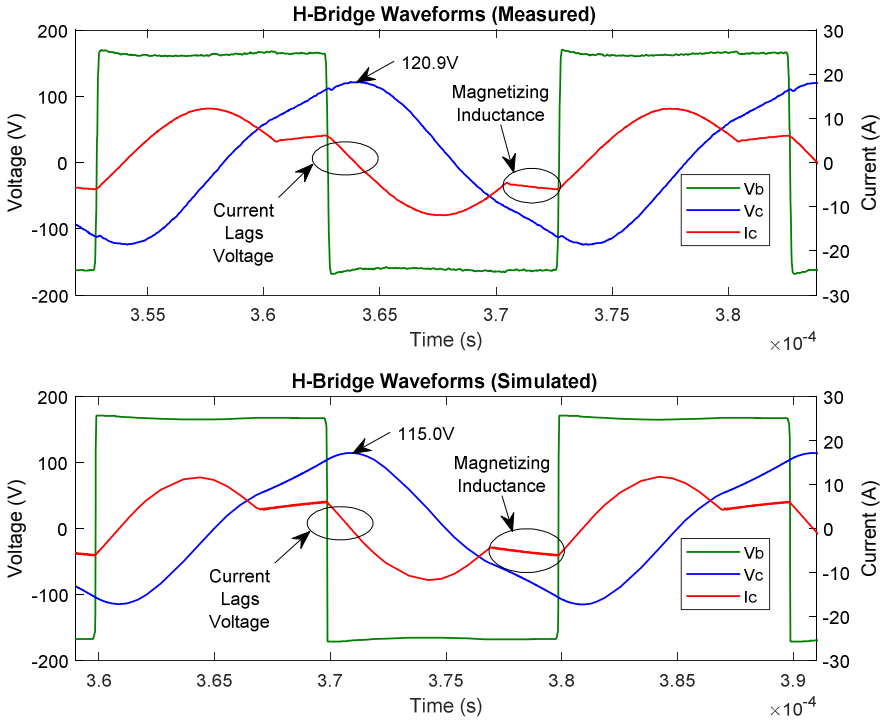


Figure 5-10: Full-Load H-Bridge waveforms (resonant converter)

After testing at full-load, the no-load waveforms were also measured as shown in Figure 5-11 to ensure that the converter is still able to achieve ZVS at zero load. From the literature, it is known that the LLC resonant converter is able to achieve ZVS at zero load. This validates the literature and is required for the use with an electrolyser stack because this condition will occur if the output voltage of the converter is lower than the minimum voltage required by the electrolyser stack to start conducting. It can be seen that the current waveforms are triangular in shape, which indicates that the magnetizing inductance is unloaded. In a SMPS the value of the magnetizing inductance will drop as the load is increased. If this converter is overloaded, the magnetizing inductance will short-circuit and the converter will shut-down because short-circuit protection was implemented in this converter by monitoring the value of the peak currents in the primary tank circuit.

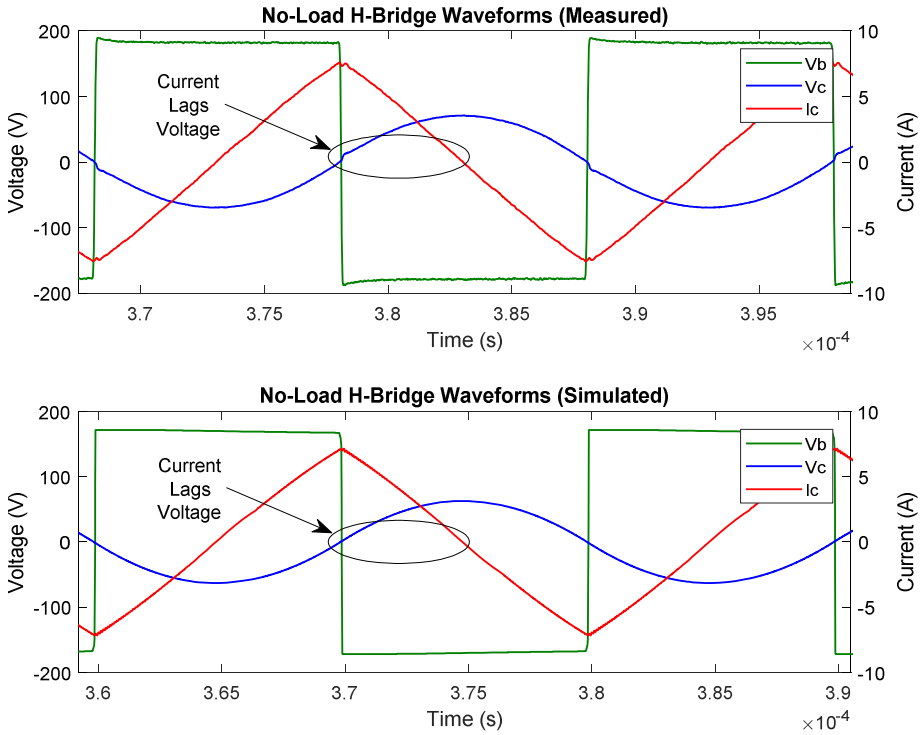


Figure 5-11: No-Load H-Bridge waveforms (resonant converter)

5.2.4 Temperature Measurements (Resonant Converter)

In this section, the temperature of each component was measured after running the converter at 1-kW load for an hour. This is to ensure the heatsink requirements (applicable to the MOSFETs) are met and also that the transformer winding insulation does not degrade due to high temperatures.

5.2.4.1 High-Voltage MOSFETs

The MOSFET case (black Epoxy encapsulation) temperature was measured at 54.2 °C as shown in Figure 5-12. With a junction-to-case temperature coefficient of 0.19 °C/W and an average power dissipation of 3.5 W, this means the junction temperature is at 54.87 °C.

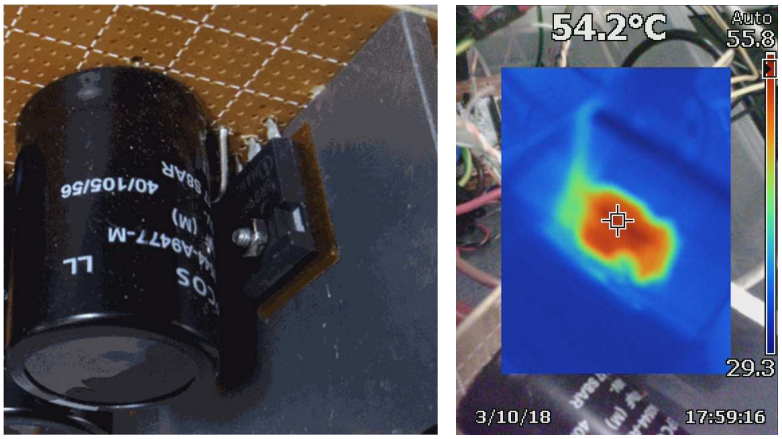


Figure 5-12: High-Voltage MOSFET temperature

5.2.4.2 Synchronous Rectifier MOSFET

The left-most image in Figure 5-13 shows the two synchronous rectifier MOSFETs (IRFP4668PbF) while the image in the middle shows the MOSFET case temperature and the right-most image shows the heatsink temperature. Air-cooling (computer CPU cooler) was used on the synchronous rectifier to keep the temperature as low as possible. At a case temperature of 61.4°C (junction to case thermal resistance is 0.29 °C/W) and a power dissipation of 2 W per MOSFET ($P = I^2 \times R = 10^2 \times 0.02 = 2\,W$), the junction temperature will be at 62 °C. At this junction temperature, the synchronous rectifier is able to deliver over 90 A (peak) per MOSFET.

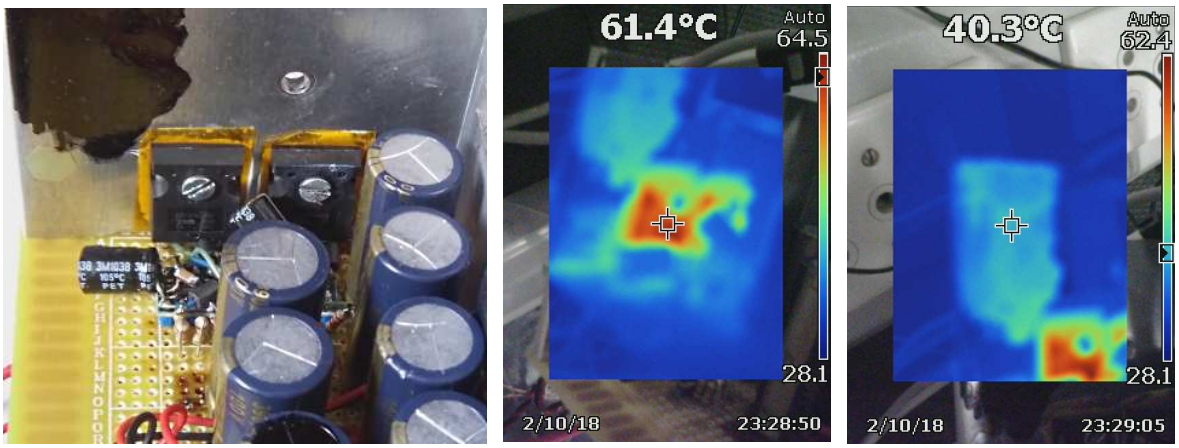


Figure 5-13: Synchronous rectifier MOSFET temperature

5.2.4.3 Diode Rectifier

The diode rectifier shown in Figure 5-14 also makes use of a small cooling fan mounted on the heatsink. The diode (DSEI60-06A) case temperature is at 48.3 °C. At a power dissipation of 11.3 W and a junction-to-case thermal resistance of 0.75 °C/W, the junction temperature is at 56.78 °C which is below the maximum allowable value of 150 °C.

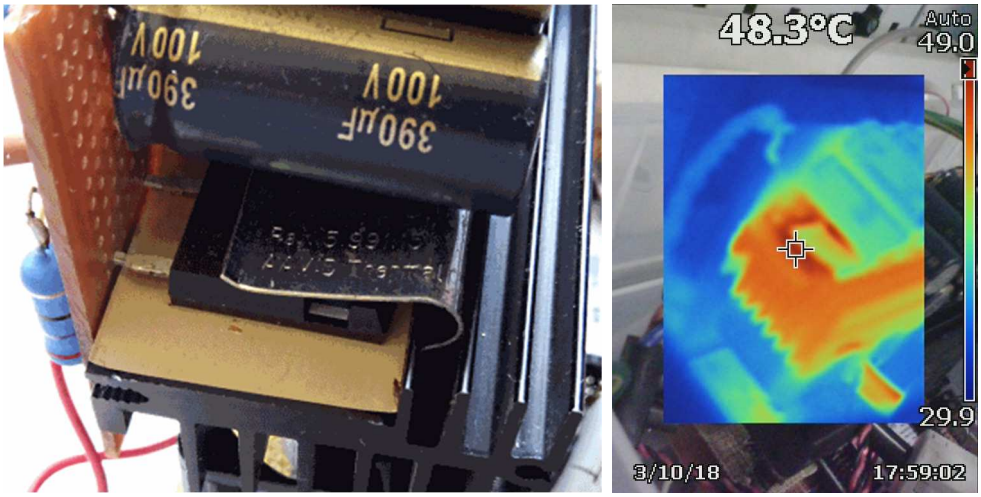


Figure 5-14: Diode rectifier temperature

5.2.4.4 Ferrite Transformer

Figure 5-15 shows the actual ferrite transformer on the left-hand side and the corresponding temperature readings on the copper in the middle while the right-most image shows the temperature of the ferrite core. The transformer windowing area was not filled with copper, it was only optimized to give the proper inductance and air-gap. The copper foil that was used were 0.125 mm thick. This was optimized in Figure 5-16 by using 0.25 mm copper foil to fill the windowing area and to reduce the resistance (which will also reduce the power dissipation and heat generated) of the copper for improved efficiency. The image on the left-most side of Figure 5-15 shows the actual image of the transformer after optimization. The maximum temperature measured on the copper reached 84.2 °C while the ferrite reached a temperature of 69.8 °C. This is well below the temperature that the Kapton® insulation material can handle which is 260 °C.

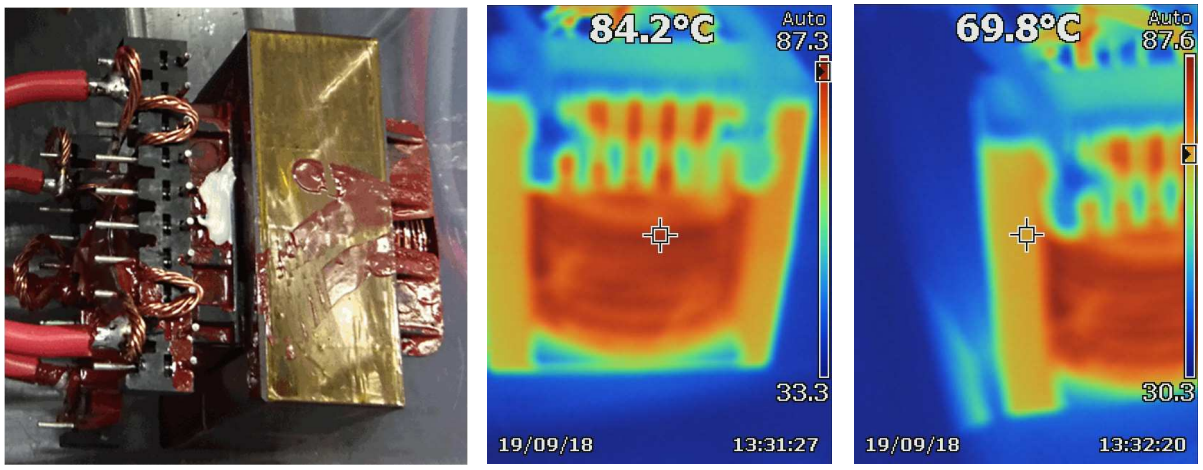


Figure 5-15: Transformer temperature

The optimized transformer's temperatures are shown in Figure 5-16. The left-most image shows the temperature measured at the front, the image in the middle shows a hot-spot where some of the copper windings are exposed and the right-most image shows the temperature of the ferrite.

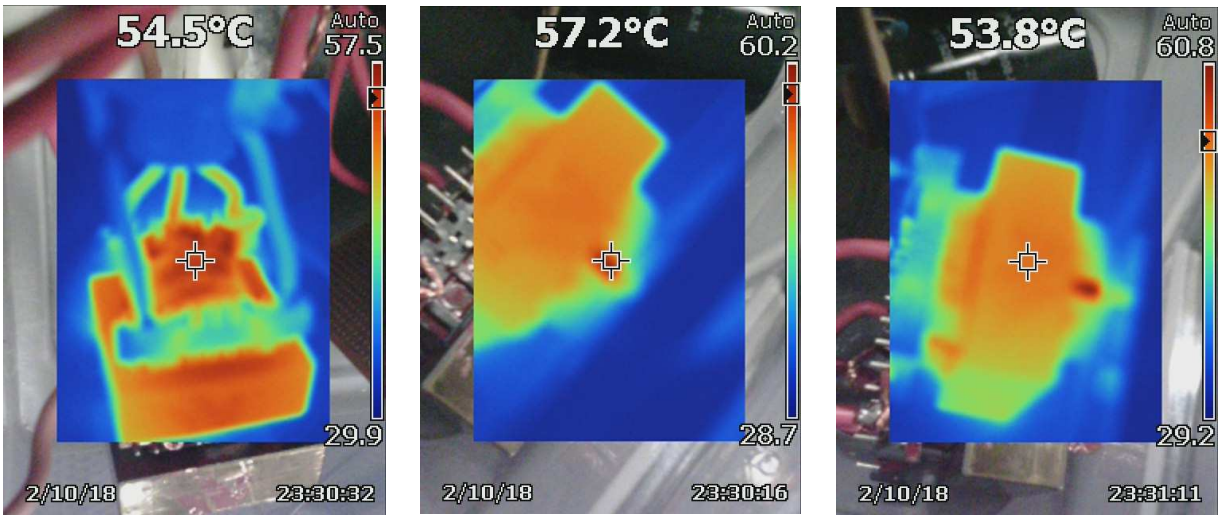


Figure 5-16: Optimized transformer temperature

5.2.4.5 Resonant Capacitor

The temperature of the polymer capacitor is shown in Figure 5-17 as 44.6 °C. This is the 300 nF resonant capacitor that is used in series with the external leak-inductor and transformer that forms the resonant tank circuit.

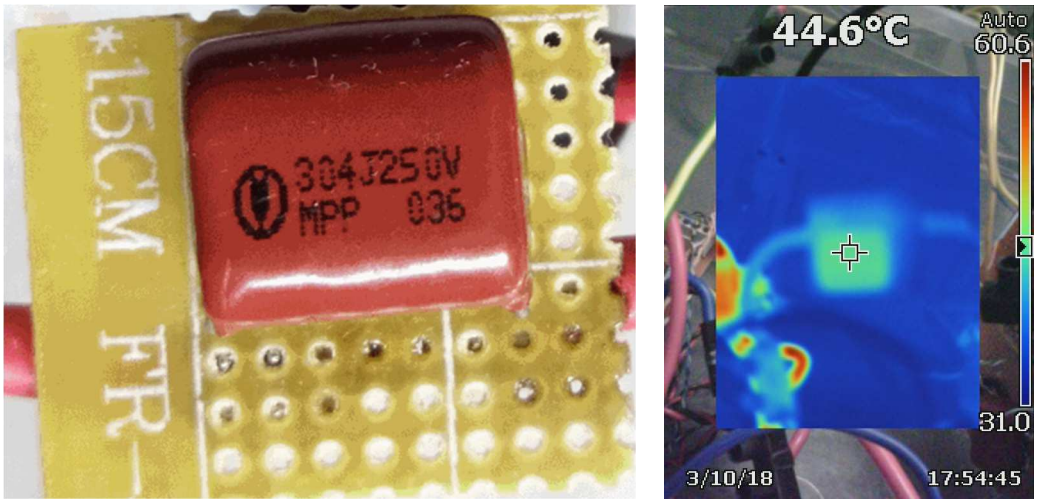


Figure 5-17: Resonant capacitor

5.3 The Hard-Switching Converter

The hard-switching converter were tested under the same conditions than the LLC resonant converter, except PWM mode was used instead of PFM mode. The input voltage supplied to the converter was adjusted to 170 V and the duty cycle for the converter was set to 33.2 % at a fixed frequency of 30-kHz.

5.3.1 High-Voltage MOSFET Waveforms

Figure 5-18 shows the locations where the measurements were taken for the high-voltage MOSFETs. All symbols indicated in green is where the MOSFET gate-source voltages were measured while the blue indicates the measurement location for the corresponding drain-source voltage. The red symbols indicate the drain-source currents while the arrows point in the direction of the current flow. The hard-switching converter makes use of seven snubber circuits, they are encircled in violet in Figure 5-18 and shows where each snubber circuit is connected.

Low input voltage waveforms were not measured because the hard-switching converter could not deliver the same power to the load than the LLC resonant converter. At 120 V input, the maximum power the converter could deliver to the load while having an output voltage higher than 40 V was 150 W vs the 700 W of the LLC resonant converter at 46 V. At 80 V input, the hard-switching converter could not deliver any power to the load and has an open-circuit output voltage of 26 V.

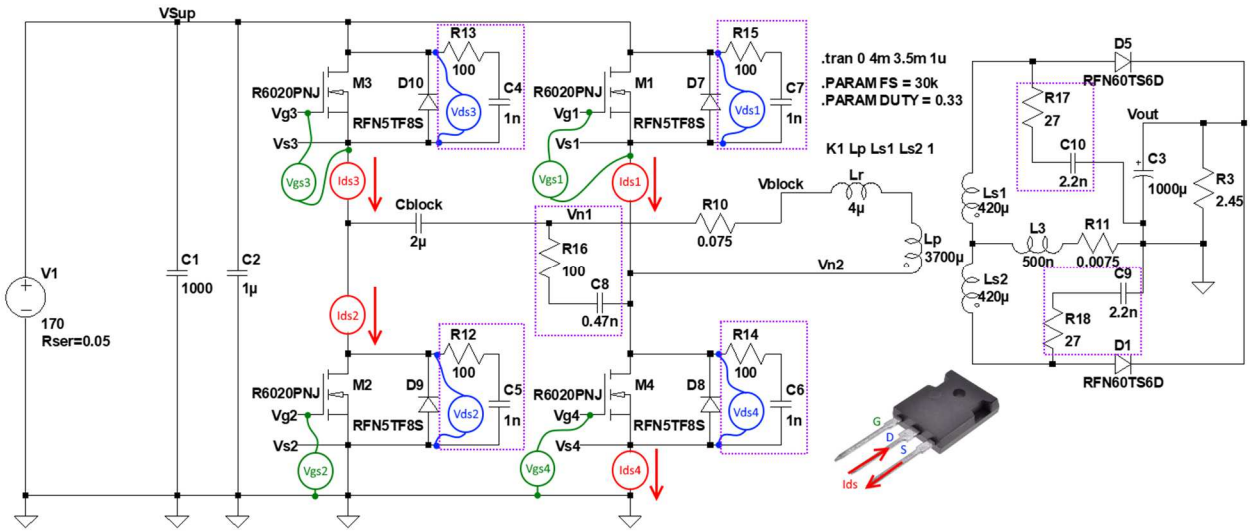


Figure 5-18: High-Voltage MOSFET measurement locations

Figure 5-19 shows the measured vs simulated waveforms. It can be seen that the drain-source waveforms have voltage spikes. This is because the converter is operating in Discontinuous Conduction Mode (DCM) and the current waveform is interrupted before completing its full cycle. The effect of the snubbers can also be observed because it is supressing the voltage spikes and keeping them from exceeding the MOSFET ratings. This shows that the snubber circuits are performing as designed. It can also be seen that the body-diodes of the MOSFETs are activating and entering their reverse-recovery modes. True ZVS is also absent because the gate is not forward biased before the drain-source voltage reaches zero which leads to hard-switching.

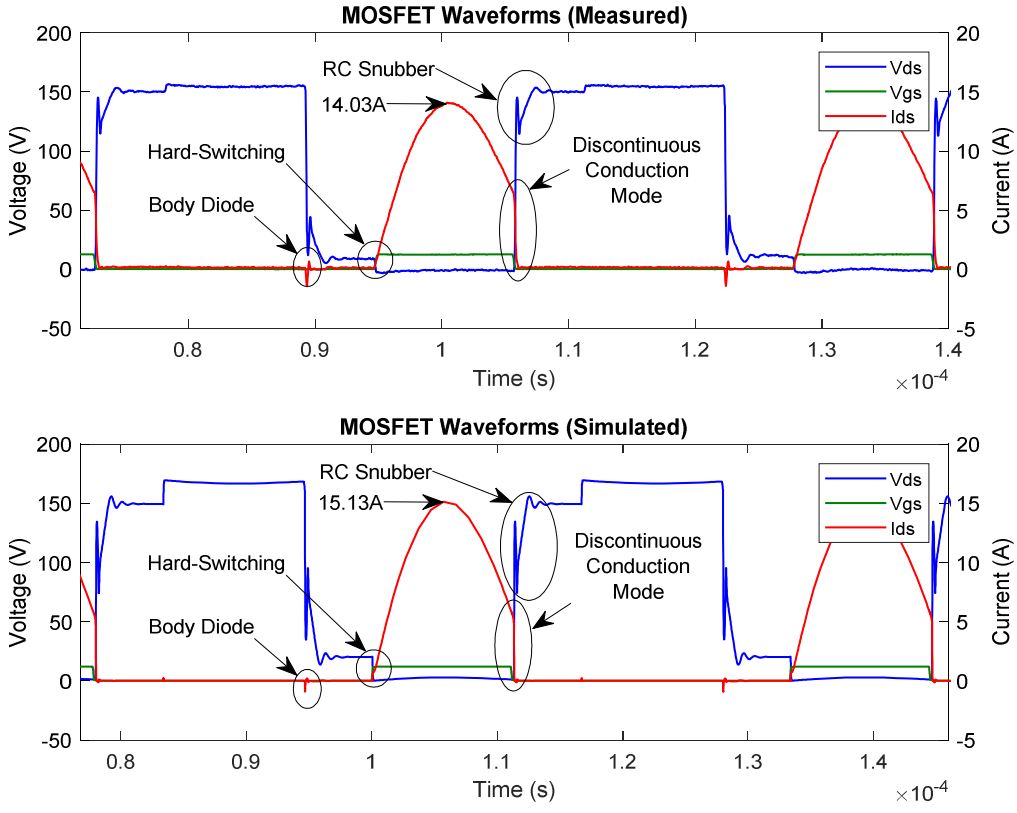


Figure 5-19: Measured vs simulated MOSFET waveforms (hard switching)

A more detailed version of Figure 5-19 is shown in Figure 5-20. The effect of hard-switching can be seen during the turn-on and turn-off cycles. The Miller effect cannot be seen clearly because the gate drivers used are capable of sinking and sourcing gate-source currents (turn-on and turn-off of the MOSFET) of up to 4 A. This forces the parasitic gate capacitances to charge instantly even if the Miller effect is present. The assistance of the RC snubber circuits in damping the oscillations also helps to reduce the Miller effect because the drain-source voltage is already very low by the time the MOSFET is turned on.

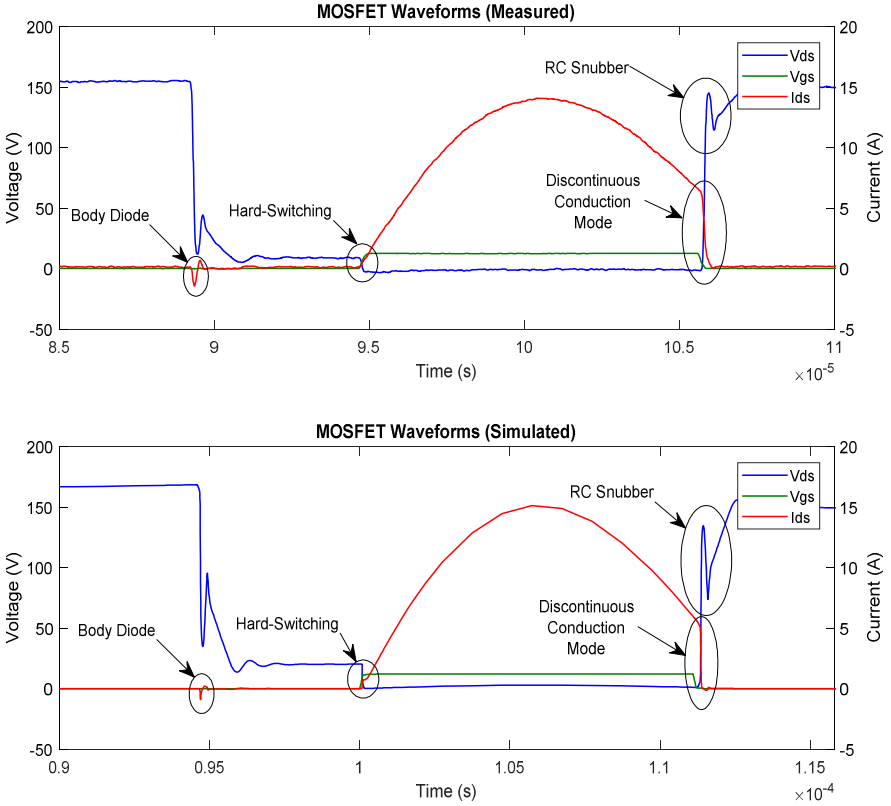


Figure 5-20: Measured vs simulated hard switched turn-off

5.3.2 Rectification Waveforms

Synchronous rectification was not tested in the hard-switching converter because of the voltage spikes that will be present on the output of the transformer. This may cause false triggering of the synchronous rectifier and may cause the rectification MOSFETs to turn-on or off at the wrong times. The same diode-rectifier used in the LLC resonant converter was used to test the hard-switching converter, except two snubber circuits were added to protect the rectifier diodes from high-voltage spikes by damping the voltage transients. Figure 5-21 shows the locations where the diode currents were measured. The direction of the current flow as well as the placement location of the probes are shown in red. In order to measure the current flow of both diodes using a single current probe, the current probe can be placed on the centre leg of the transformer. This is indicated as Id in Figure 5-21. To measure them separately, two current probes can be used in locations Id1 and Id2. The snubber circuits are encircled in violet.

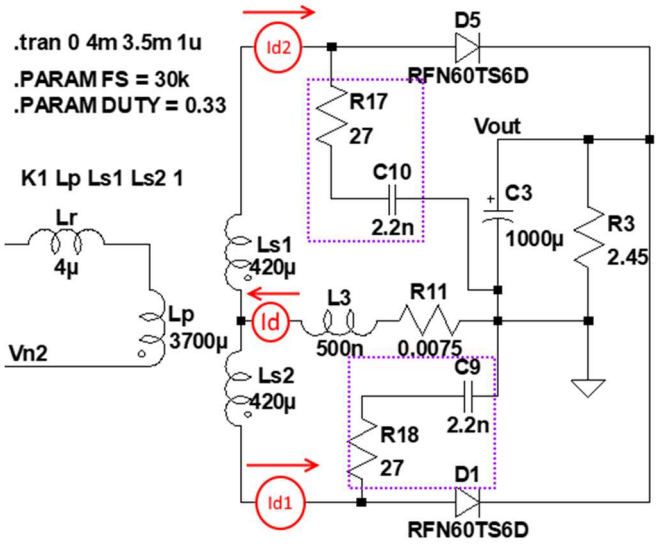


Figure 5-21: Rectification measurement locations

The diode waveforms shown in Figure 5-22 were measured using a single current probe. Both diodes enter reverse-recovery mode at the end of each switching cycle with a peak reverse-recovery current of 4.51 A. ZCS only takes place during the turn-on cycle. This reverse-recovery current leads to additional power losses because the diodes will conduct in the reverse direction for a few nanoseconds.

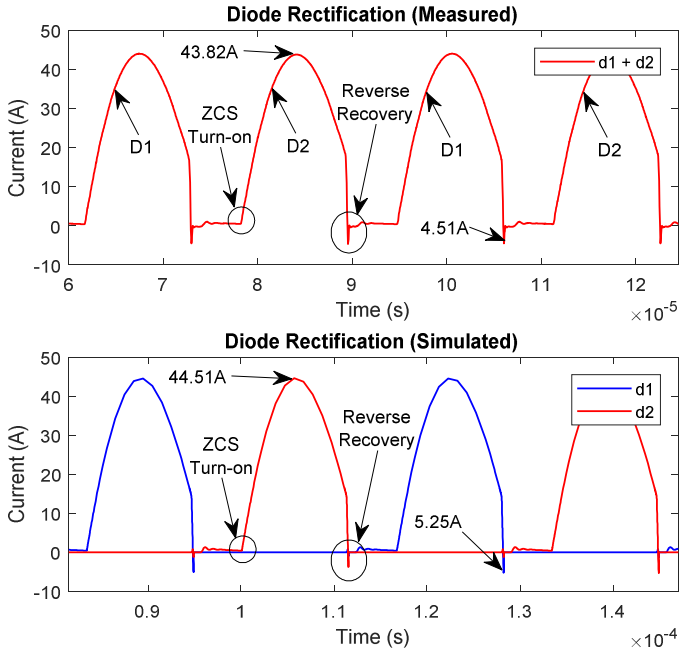


Figure 5-22: Measured rectification waveforms

5.3.3 H-Bridge Waveforms

The H-bridge waveforms were also measured at the locations shown in Figure 5-23 during full-load and no-load. The DC-blocking capacitor voltage waveforms was measured (measurement location shown in blue) as well as the current flowing through the DC-blocking capacitor (measurement location shown in red). Because the capacitor is placed in series with the transformer, the current waveforms passing through the capacitor is the same as the current waveforms sourced to the transformer. The high-voltage PWM waveforms generated by the H-bridge was measured in the location marked in green.

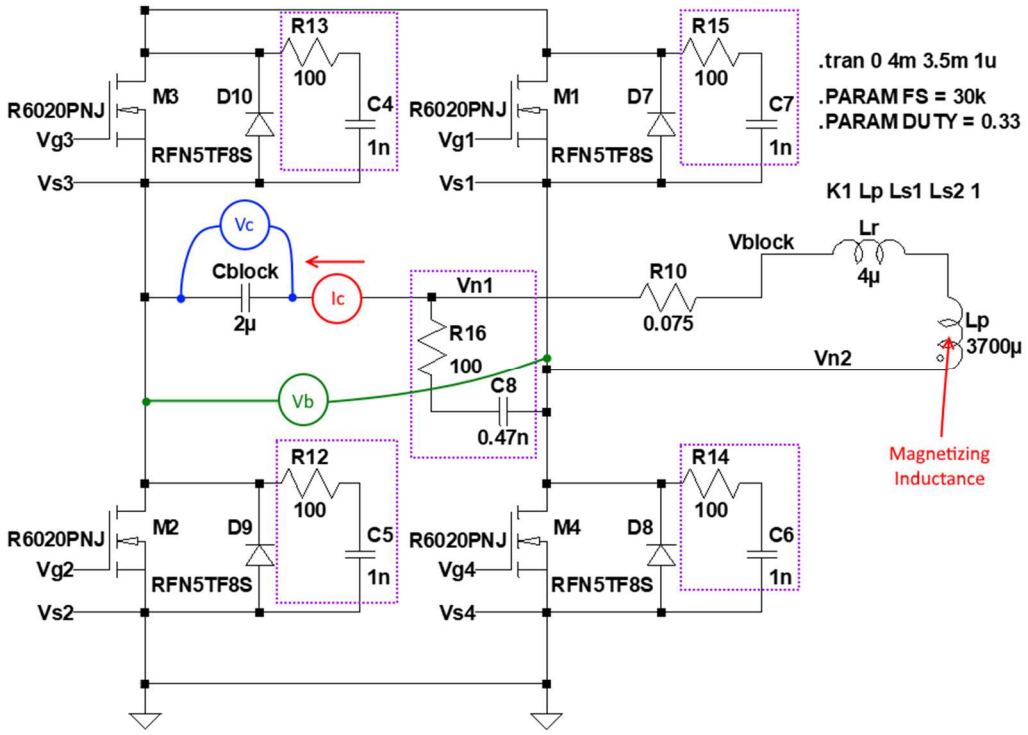


Figure 5-23: H-Bridge measurement locations

During a full-load condition the capacitor voltage reaches a peak value of 33.2 V while the peak current reaches 15.13 A as shown in Figure 5-24. During these peak current cycles, the peak-instantaneous power in the primary bridge reaches a value of 2.57-kW. The effect of DCM can also be seen in the current waveforms. During each of the turn-off cycles, the current and voltage waveforms can be seen overlapping. This causes a voltage spike (which is mostly absorbed by the snubber circuits shown in Figure 5-23).

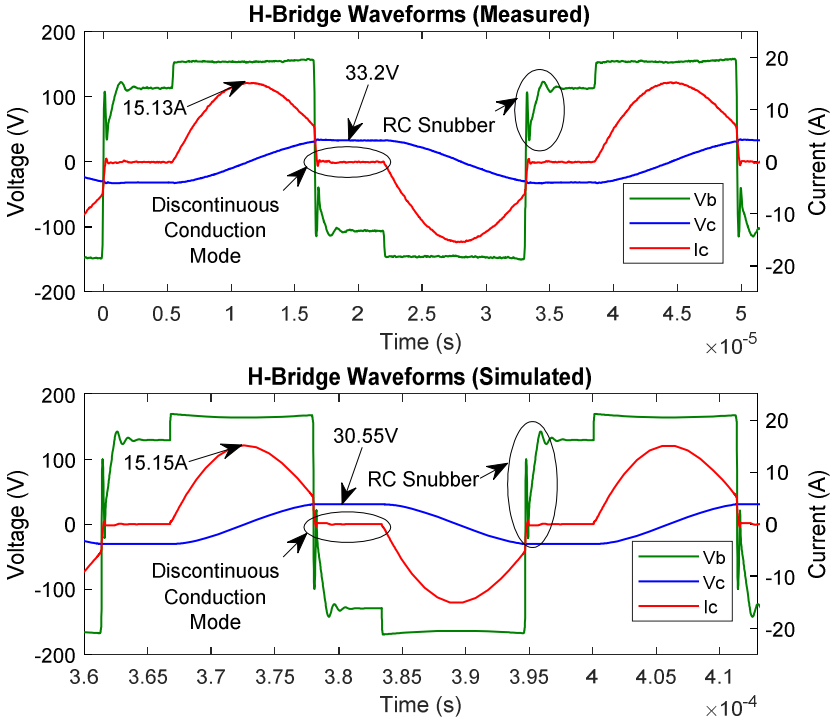


Figure 5-24: Full-Load H-Bridge waveforms (hard switching)

Under no-load, the current in the H-bridge will lag the voltage as shown in Figure 5-25. Small voltage spikes will be fully absorbed by the snubber circuits during no-load. This means that under no-load, the hard-switching converter will also perform ZVS, but ZVS performance will progressively become worse as the load is increased. The capacitor voltage doesn't change much because the current flowing through the H-bridge is too small. In the LLC resonant converter, the peak currents reaches 5 A at no-load while the capacitor voltage is sinusoidal.

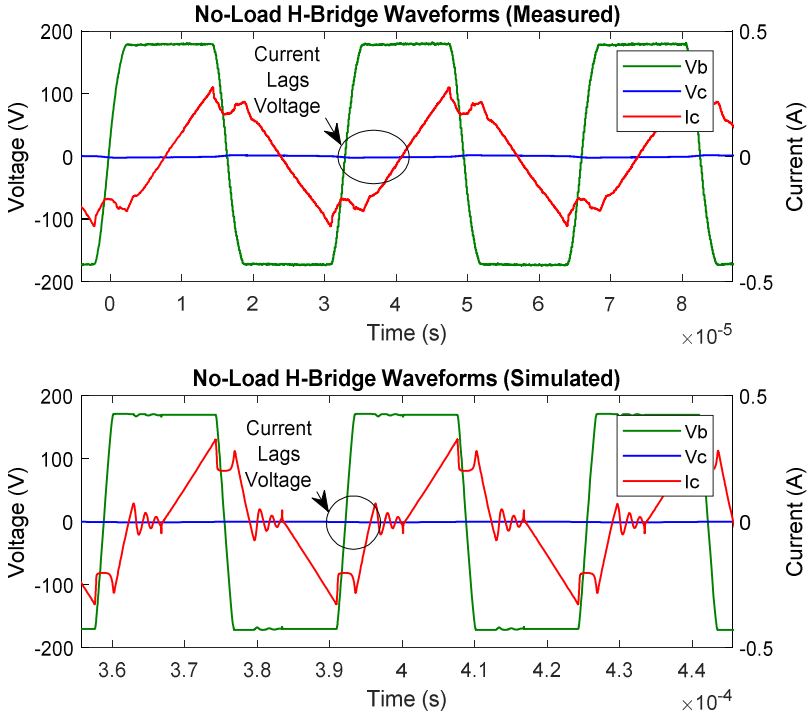


Figure 5-25: No-Load H-Bridge waveforms (hard switching)

5.3.4 The Miller Effect

The high-voltage MOSFET waveforms were measured again at 30-kHz with a 20 % duty cycle and a load of 450 W. During this condition, the Miller effect could be observed at both turn-on and turn-off. Figure 5-26 shows the Miller effect when the MOSFET is switched on when its drain-source voltage is at 20 V. If no snubber circuits were used, then this turn-on condition would have been worse because the drain-source voltage would have oscillated before it is turned on. During the Miller plateau, the capacitance seen by the gate driver increases suddenly. This is the reason why the characteristic curve of a charging capacitor can be seen after the point where the MOSFET junction starts to conduct (Vth). The current and voltage waveforms can also be seen to overlap, which leads to additional turn-on switching losses.

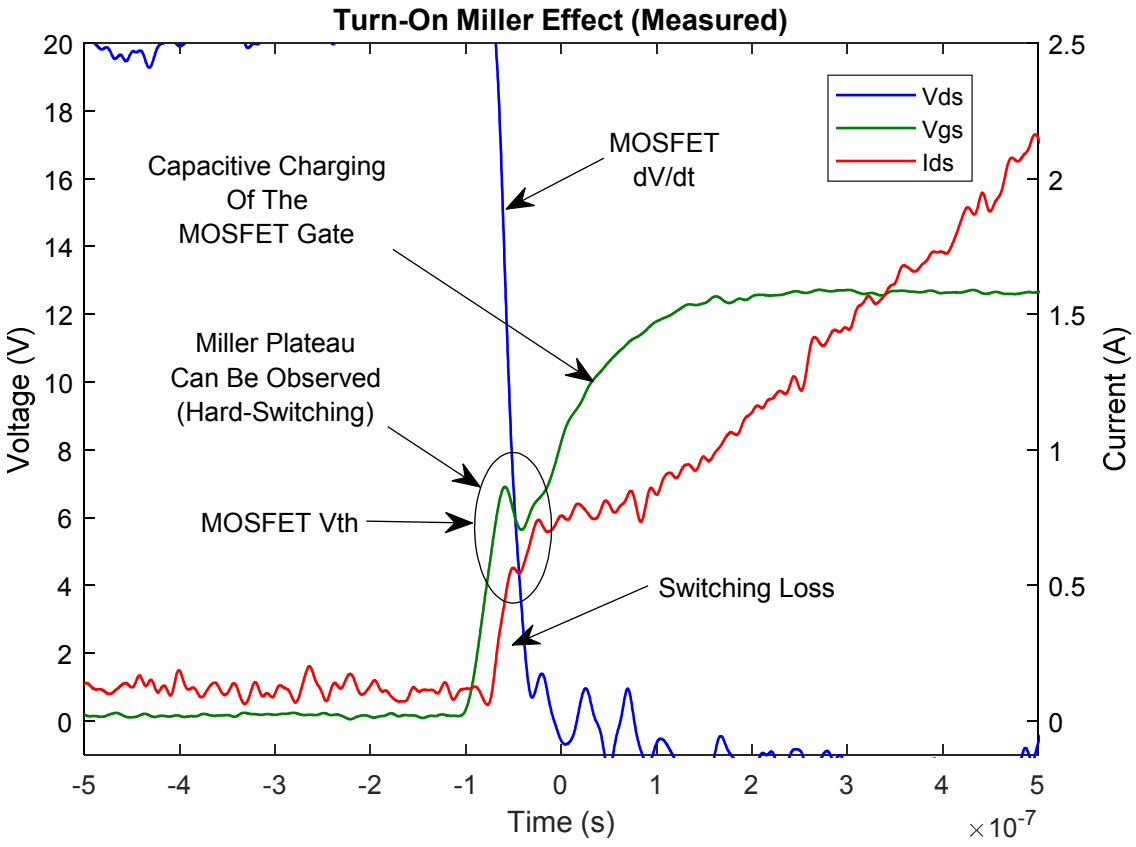


Figure 5-26: Miller effect during turn-on

The Miller effect is greater during the turn-off cycle (Figure 5-27). The time delay when the gate driver discharges the gate capacitance and the actual steady state turn-off time is about 300 ns. This is caused by the large overlap of the drain-source voltage and current, which reaches a peak power of 200 W in Figure 5-27. The voltage ringing on the gate of the MOSFET can also lead to a false turn-on condition and a shoot-through if the dead time is not large enough.

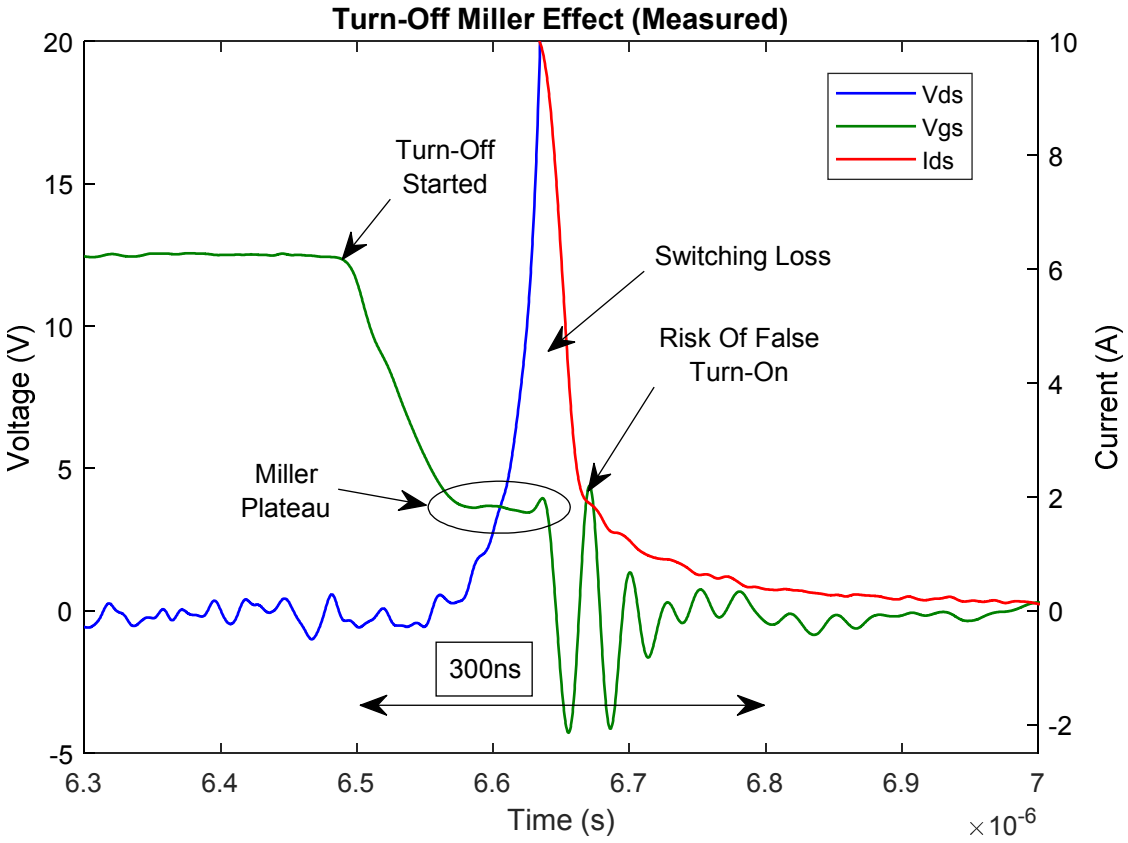


Figure 5-27: Miller effect during turn-off

5.3.5 Temperature Measurements (Hard Switching Converter)

Temperature measurements were taken at the MOSFETs, diode rectifier, transformer, snubbers and DC blocking capacitor after one hour while the hard switched converter was running at a load of 1-kW.

5.3.5.1 High-Voltage MOSFETs

The left-most image in Figure 5-28 shows the actual MOSFET where the measurement was taken while the image in the middle shows the MOSFET case temperature. The right-most image shows the temperature of the heatsink. A CPU cooler and fan was mounted on the aluminium heatsink to prevent the MOSFETs from overheating. The heatsink in this converter was not optimized because this converter will not be used in an actual system and was just used to validate the simulated waveforms of a hard-switching converter.

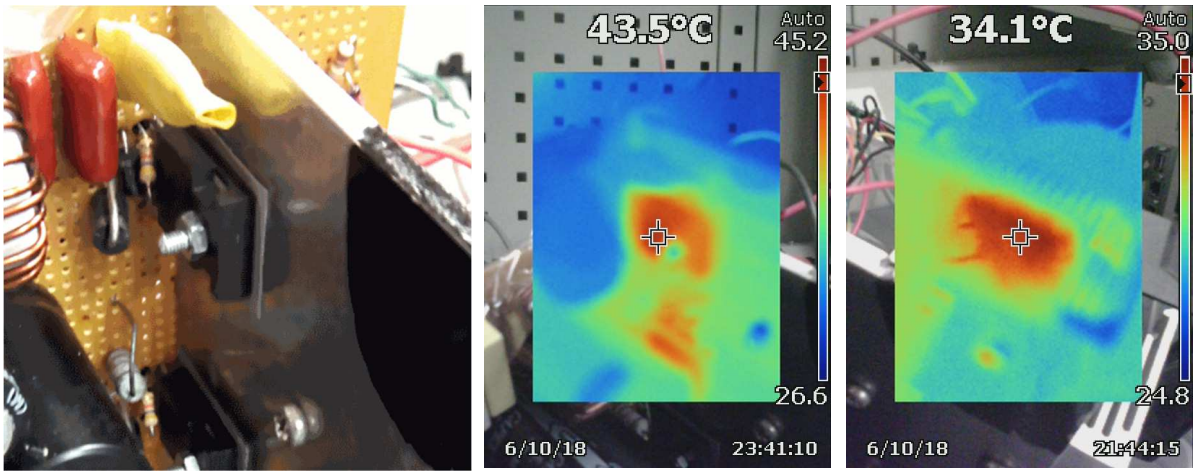


Figure 5-28: High-Voltage MOSFET temperature

5.3.5.2 Diode Rectifier

In the hard-switching converter, the diode rectifier operated at a temperature of 53.7 °C (compared to 48.3 °C in the LLC resonant converter). The junction temperature of the diodes (thermal resistance of 0.75 °C/W) will be 62.18 °C when each diode is dissipating 11.3 W of power.

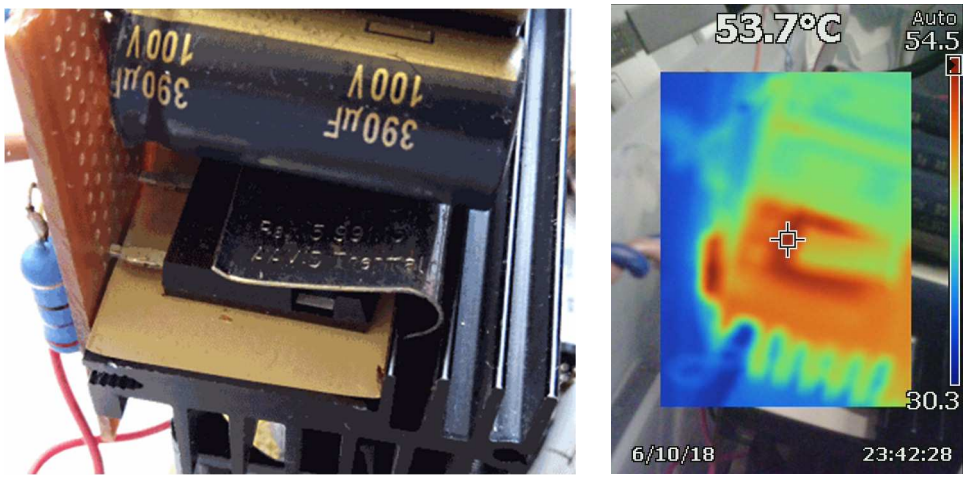


Figure 5-29: Diode rectifier temperature

5.3.5.3 Ferrite Transformer

The left-most image in Figure 5-30 shows the EE65 transformer that was used while the image in the centre shows the temperature of the exposed copper foil. The peak temperature of the copper reached 78.6 °C while the ferrite reached a temperature of 52.6 °C. This high-temperature of the copper will lead to additional power losses because the copper has a positive temperature coefficient.

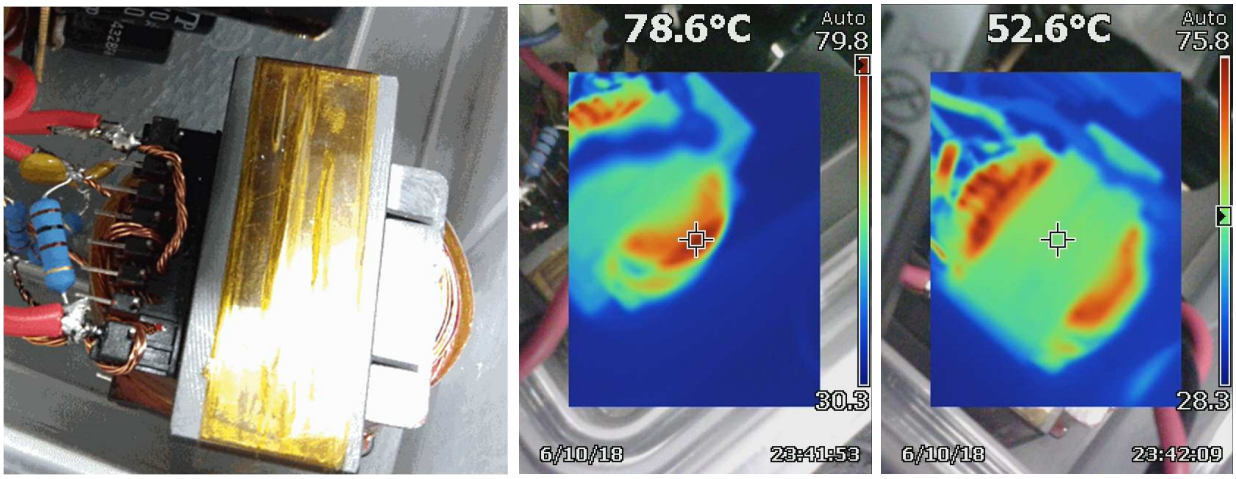


Figure 5-30: Transformer temperature

5.3.5.4 RC Snubbers

Figure 5-31 shows the resistor of each RC snubber used. The left-most image is the resistor used in the MOSFET snubbers, the image in the centre shows the resistor used in the diode rectifier's snubber and the right-most image shows the resistor of the RC snubber used on the transformer. All snubber resistors used were blue. Figure 5-32 shows the corresponding thermal images in the same order.

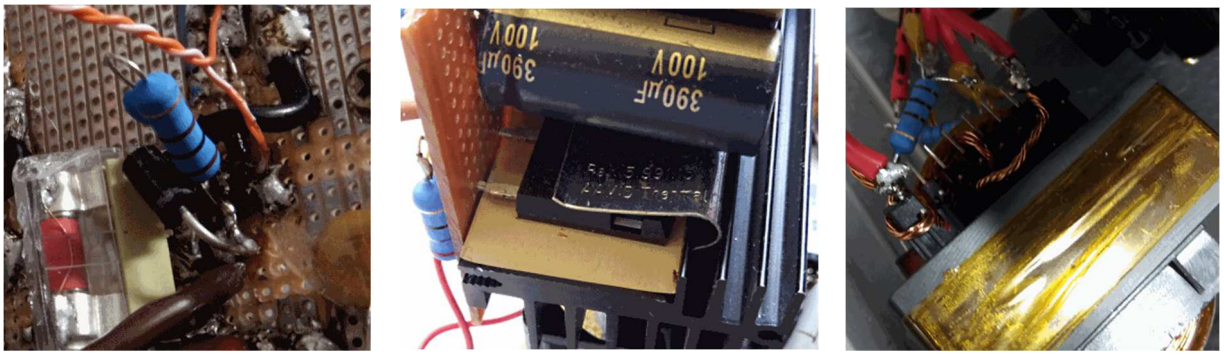


Figure 5-31: RC snubber circuits

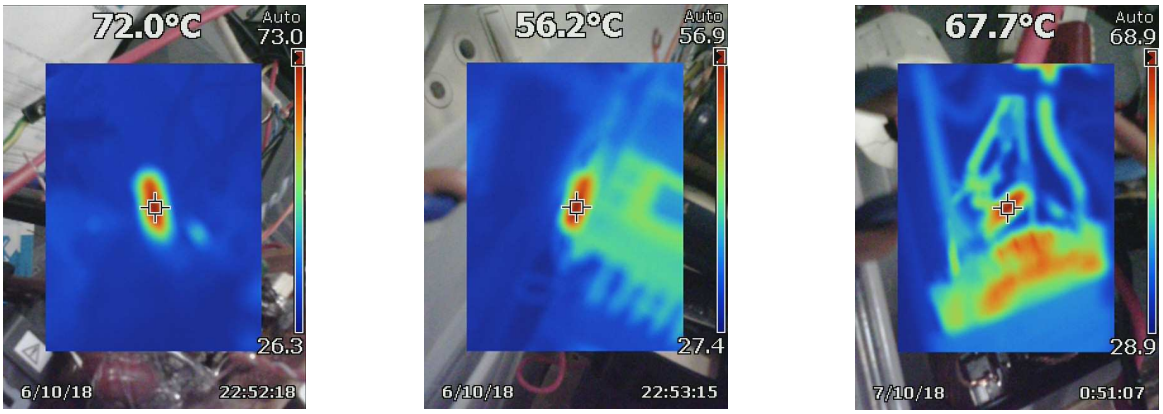


Figure 5-32: RC snubber temperatures

5.3.5.5 DC Blocking Capacitor

Figure 5-33 shows the temperature of the DC blocking capacitor at 84 °C. This unusually high for a polymer capacitor and may be because it is a no-name brand. It is recommended to replace the capacitor with a higher quality one or to parallel multiple capacitors to reduce the ESR because it will not last very long at this high temperature.

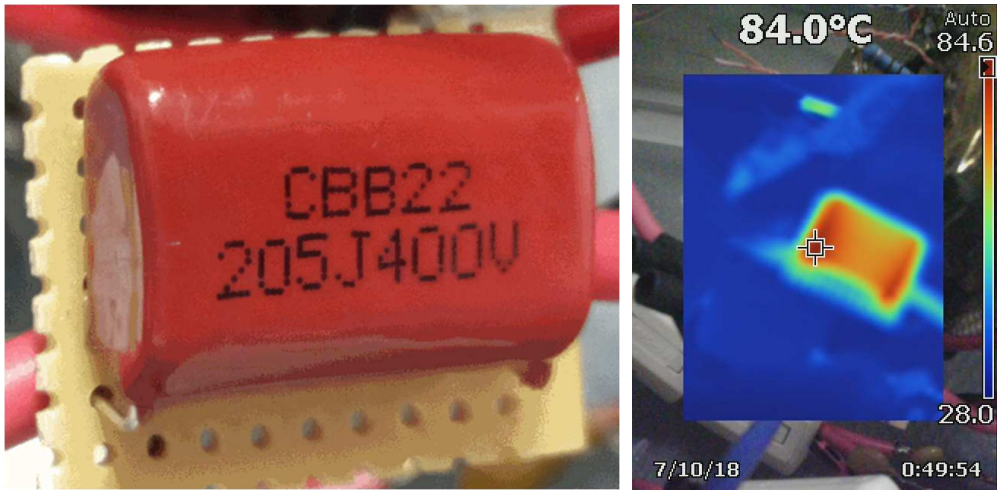


Figure 5-33: Capacitor temperature

5.4 Efficiency Comparison

Efficiency was measured using two voltage and current probes. A voltage probe was attached to the input of the converter, as well as a current probe. The same was done at the output of the converter. Efficiency is calculated by multiplying the output voltage and current waveforms and then obtain the average (average instantaneous power). The same was done at the input side to obtain the real power only. Efficiency is then calculated by dividing the output power with the input power and multiplying with 100 %. To verify this, the average of the input and output current and voltage were waveforms were obtained first and then multiplied to obtain the input and output power. Individual component losses could not be measured due to limitations of the current probes. To compensate for this during total efficiency measurement, the DC-offsets of the current probes (input and output) were measured first and then multiplied with the average of the voltage (input and output). This power-offset was then subtracted from the final input and output power. It was also verified using multi meters as well as the values displayed on the digital electronic load. Each of the DC/DC converters (LLC and hard-switch converter) had four sensors that measured input voltage and current and displayed the power as well as real-time efficiency on a laptop. All efficiency calculations are accurate up to a certainty of +-2 %.

The efficiency curves shown in Figure 5-34 was measured using the diode rectifier on the output. Measurements started at 50 W which was increased to 100 W up to 1-kW in 100 W increments. The peak efficiency of the LLC resonant converter was achieved at 800 W with a value of 93.8 % while the full-load efficiency was 93.26 %. During light-load conditions (below 450 W), the hard-switching converter achieved higher efficiencies. This is because pulse skipped switching was not implemented on the LLC resonant converter. If pulse skipping was implemented, it would have obtained higher efficiencies below 450 W but this involves very complicated and time consuming programming on the embedded controller because most controllers are designed for PWM and not PFM.

The hard-switching converter achieved its highest efficiency at 500 W (91 %) while the full-load efficiency dropped to 89.7 %. Synchronous rectification was not tested on the hard-switching converter because voltage transients may trigger incorrect switching times on the synchronous rectification controller and cause a short-circuit. At 50 W load, the hard-switching converter achieved a 12 % better efficiency than the LLC resonant converter. The purpose of Figure 5-34 is to compare the efficiencies of the two power converters under the same operating conditions using the same type of rectifier.

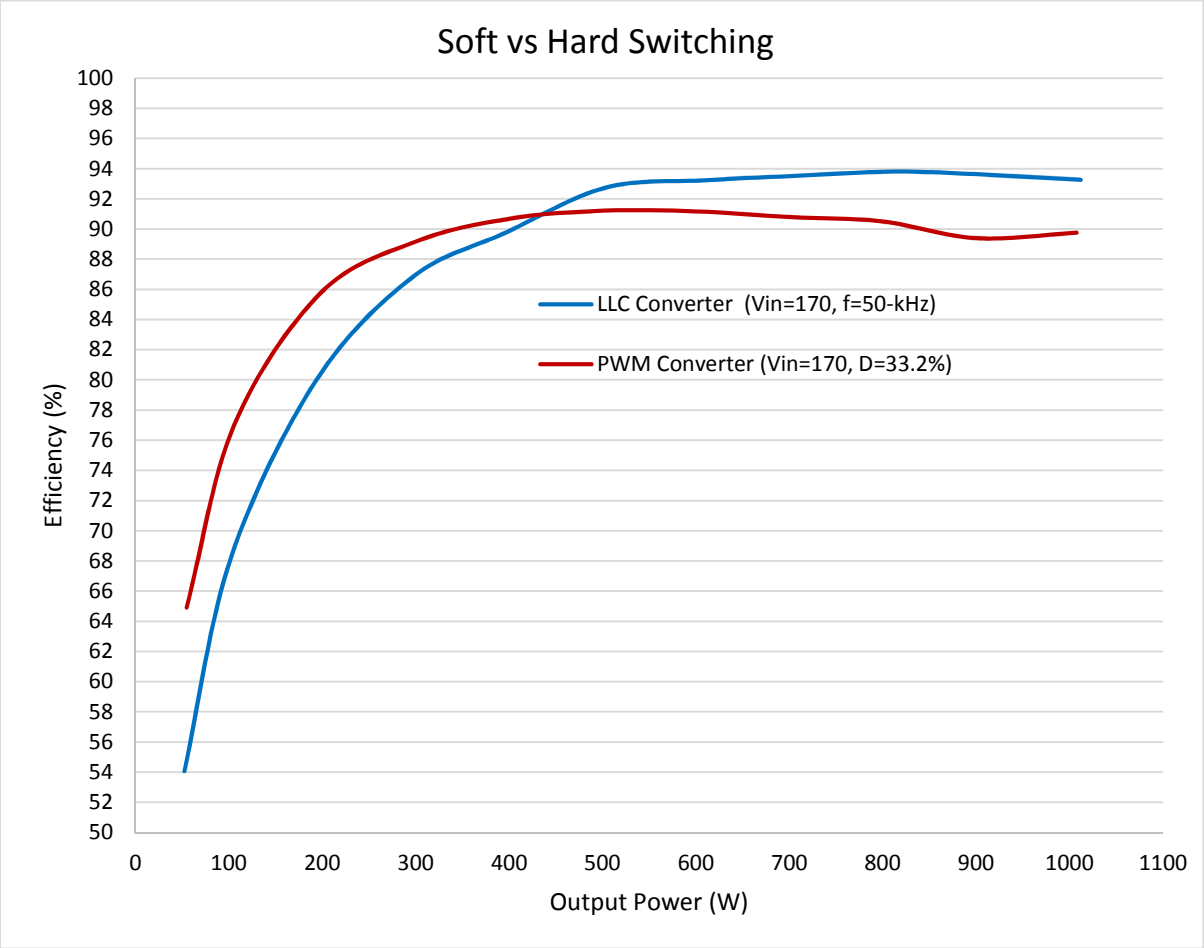


Figure 5-34: LLC Resonant Converter vs Hard-Switching efficiency

Figure 5-35 compares the efficiency performance of synchronous rectification vs diode rectification. All efficiency curves were measured on the LLC resonant converter, starting at 50 W which was then increased to 100 W up to 1-kW in increments of 100 W. The synchronous rectifier controller performs intelligent pulse skipping at the output during light load conditions below 200 W to maintain a high efficiency. If this had been applied to the high-voltage switching section in the embedded code, then the efficiency below 450 W (Figure 5-34) would have been higher.

Figure 5-35 proves that synchronous rectification is always better than diode rectification (from an efficiency point of view) because it improves the efficiency throughout the entire load range. This will result in better energy storage (Hydrogen production) over the course of a year if the system is operated on a daily basis. The peak efficiency of the LLC resonant converter (using synchronous rectification) was 97.1 % at 900 W. At 1-kW, the efficiency dropped by only 0.1 %. The efficiencies at low input voltages (120 and 80 V) were also measured using the synchronous rectifier. At 120 V input, the peak efficiency was 96 % at 700 W while at 80 V input, the efficiency was 92.4 % at 350 W load.

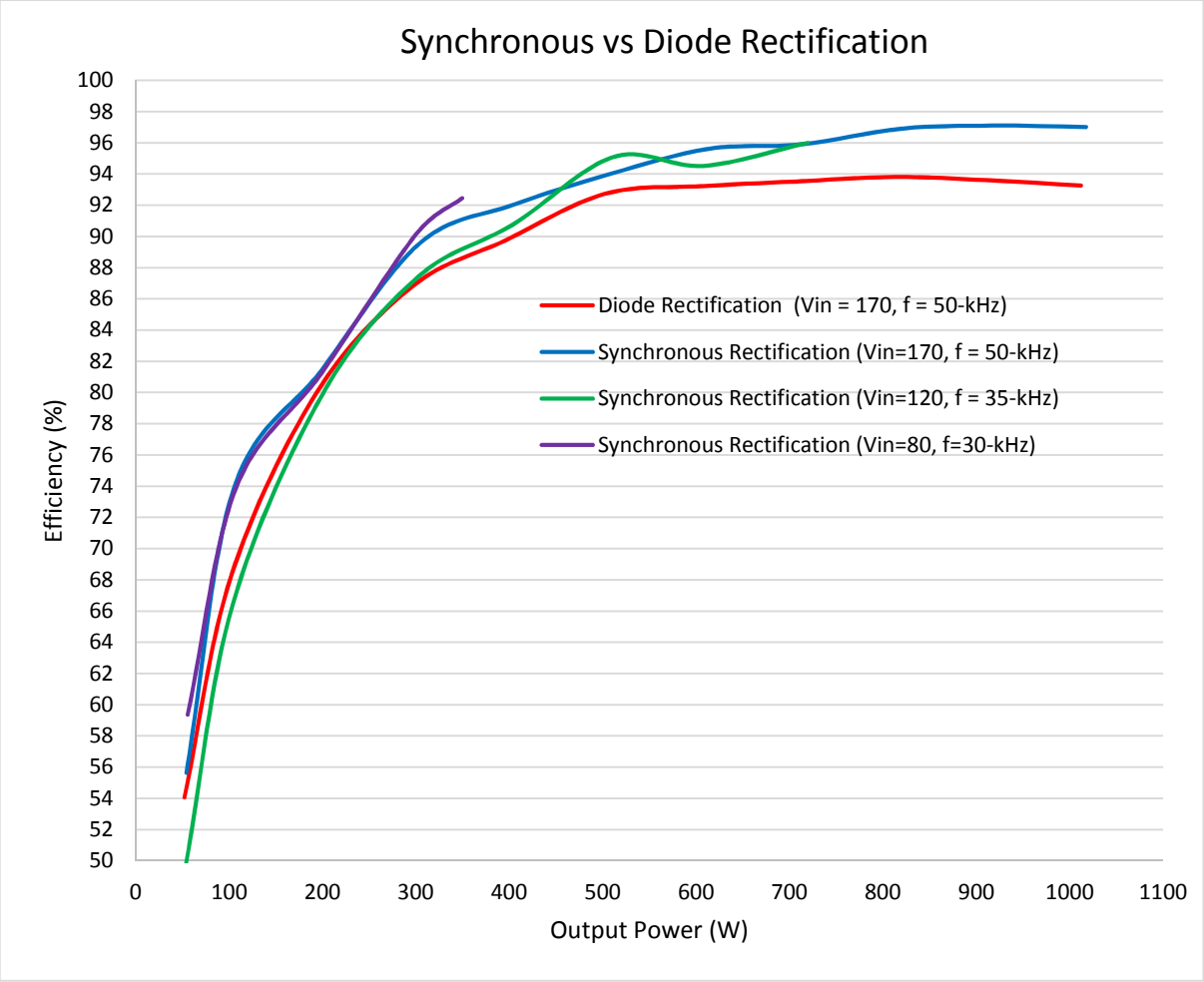


Figure 5-35: Measured dynamic efficiency at 80, 120 and 170 V input

5.5 Conclusion (Validation)

5.5.1 The LLC Resonant Converter

This chapter validates the two simulated models (Matlab® and Ltspice®) for the LLC resonant converter and proves that this type of converter is able to achieve ZVS across the entire load range, even during a no-load condition. It also validates that the LLC resonant converter has a very high efficiency (above 90 %) which can be improved further by upgrading the diode-based rectifier to a synchronous rectifier. Soft switching happens on both the primary side as well as the secondary side, regardless whether diode (ZCS) or synchronous rectification (ZVS) is used. The instant reverse recovery of the body diode for the MOSFETs (both in the H-Bridge as well as the synchronous rectifier) could be seen because the diode starts conducting first, causing a very low forward voltage drop which is then followed by the turn-on of the MOSFET. This sweeps out any charges left in the diode which causes the diode to reverse-recover instantly. For this reason, this converter does not require the use of fast-recovery diodes (which was validated in the ZVS and ZCS waveforms). Current waveforms are never interrupted and the converter can be seen operating in CCM. No current spikes in the form of reverse-conduction (caused by reverse-recovery currents) could be seen at the end of each switching cycle. The Miller effect could not be observed, which also validates the soft-switching mode of this type of converter.

5.5.2 The Hard-Switched Converter

The presence of voltage and current spikes could be seen in the H-Bridge of this converter. Cross-conduction currents could be observed, indicating that the body-diodes of the MOSFETs are entering reverse-recovery mode due to the current waveform being interrupted at the end of each cycle, without completing a full current waveform (DCM). This leads to additional switching losses, which could be seen in the MOSFET waveforms which validates the presence of the Miller effect because it could be clearly seen in both the turn-on as well as the turn-off cycle of the MOSFETs. Hard switching could also be seen at the secondary side where diode rectification is used (absence of ZCS) because the rectification diodes entered reverse-recovery at the end of each switching cycle. The snubber circuits as well as the transformer operated at temperatures above 70°C, which proves high amounts of power dissipation.

5.5.3 Suitable Converter

The LLC resonant converter was able to operate at a low input voltage (80 V) compared to the Hard-Switching converter's 170 V while having an output voltage above 42 V. This makes the LLC resonant converter more suitable for coupling a renewable energy source to an electrolyser as it is able to operate at a high efficiency at a much lower input voltage.

CHAPTER 6: PRACTICAL IMPLEMENTATION RESULTS

In this chapter, the LLC resonant converter were connected to a PV array (capable of up to 1.6-kW) and a 24 cell electrolyser. Two MPPT algorithms were implemented in the software, they are:

- Perturb and Observe with a constant increment / decrement frequency and
- Variable-Step Incremental Conductance which varies the increment / decrement frequency step size.

The software application that was written in Embarcadero RAD Studio® (Delphi 10.2) connects to the STM32F411RET6 controller via a USB-to-USART and can select between open-loop (unregulated) and closed-loop (MPPT) control. It is able to switch between the two different MPPT algorithms in real-time without having to stop and restart the system. The system were run for a few days using both algorithms, the results are discussed throughout this chapter.

6.1 Software Application Interface

Figure 6-1 shows the software application interface. It shows the input and output voltage and current and also calculates the power and real-time efficiency using a moving average filter (implemented in the embedded firmware). It is also able to calculate the energy (in kWh) and continuously logs the data to a .csv file every second.

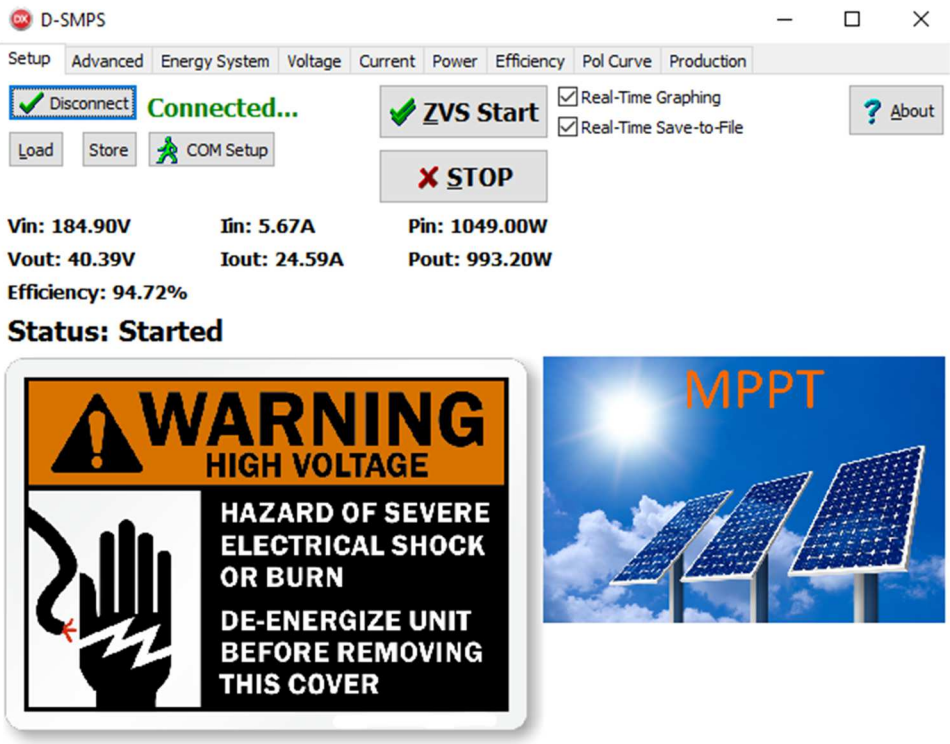


Figure 6-1: Software application interface

Figure 6-2 shows additional information that is calculated (and logged) by the system. Because power changes intermittently, it is preferred to calculate the energy efficiency using integration (programmed into the application using fast-timers). The system is then able to calculate the amount of energy extracted from the solar panels, the amount of energy used by the power converter and the amount of energy supplied to the electrolyser stack. If the information of the stack is known, it can be entered into the fields on the right-hand side and the system will then also estimate the amount of hydrogen and oxygen produced in normal litres per minute. Time-based integration is applied to calculate the total amount of hydrogen produced as well as the total efficiency of the system (by taking the efficiency of the electrolyser stack into account). The electrolyser stack was characterised beforehand in order to determine the amount of nLPM it produces per cell per amp. Note that this image was taken at the end of the day after the system was shut down (hence the reason the real-time hydrogen and oxygen generation shows 0 nLPM).

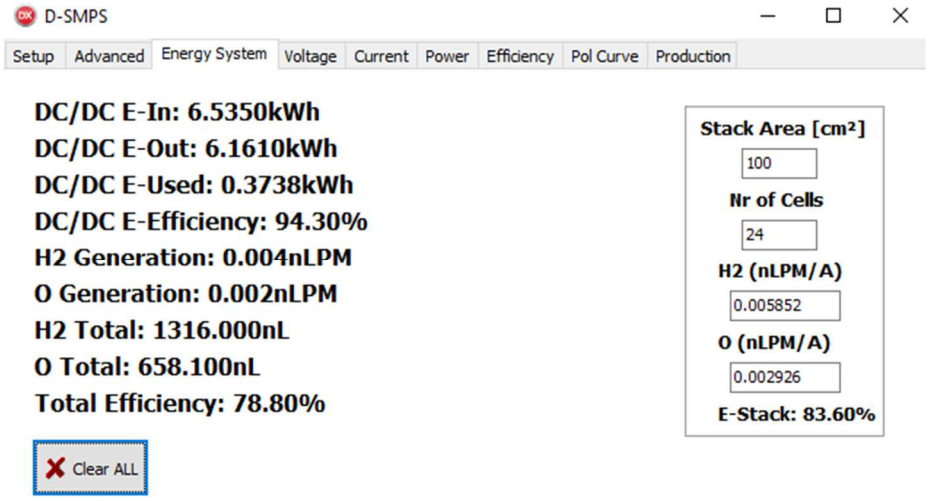


Figure 6-2: Energy logging system

6.2 MPPT Comparison

The MPPT algorithms were modified because they are designed to work in the embedded firmware of a PWM converter that uses a linear load instead of a resonant converter that is coupled to an electrolyser. In a PWM converter, the duty cycle is expressed as a ratio of power (and is assumed to be perfectly linear) whereas in a resonant converter it is expressed as a frequency which is not linear at all. To increase power in a PWM converter, the duty cycle is increased and the frequency is kept constant. In resonant mode power converters, to increase power, the frequency is decreased and the duty cycle is kept constant. Output power does not increase linearly with frequency because the gain of a resonant converter is also dependent on the load and a large electrolyser cell (like the one that was used) represents an electrical circuit that is very similar to a super capacitor. Increasing the gain too quickly will result in a short-circuit of the power supply whereas adjusting it too slowly will result in poor MPPT performance.

6.2.1 Perturb and Observe

In this implementation, the frequency increment / decrement rate was chosen to be 500 Hz (0.5-kHz). This was determined using an iterative process to optimize the MPPT tracking speed. The electrolyser stack makes the MPPT implementation more difficult than usual because the electrolyser stack has a non-linear response and will cause current surges while the MPPT makes adjustments. As can be seen in Figure 6-3 (data from 07 November 2018), the sudden change in solar irradiance early in the morning triggers the power supply's Overcurrent Protection (OCP) due to the electrolyser causing a surge current when the sun re-appears behind a cloud. When the OCP activates, it increases the resonant frequency with 1-kHz (and reduces the duty cycle) for every switching cycle up to a maximum of 250-kHz. If the OCP still detects current spikes greater than 13 A in the primary tank circuit, it will shut down. Total energy drawn from the solar panels were 6.3 kWh while the system consumed only 0.41 kWh of this energy. This resulted in an energy efficiency of 93.5 % for the DC/DC converter. The electrolyser stack produced a total of 1265 litres of hydrogen (at atmospheric pressure).

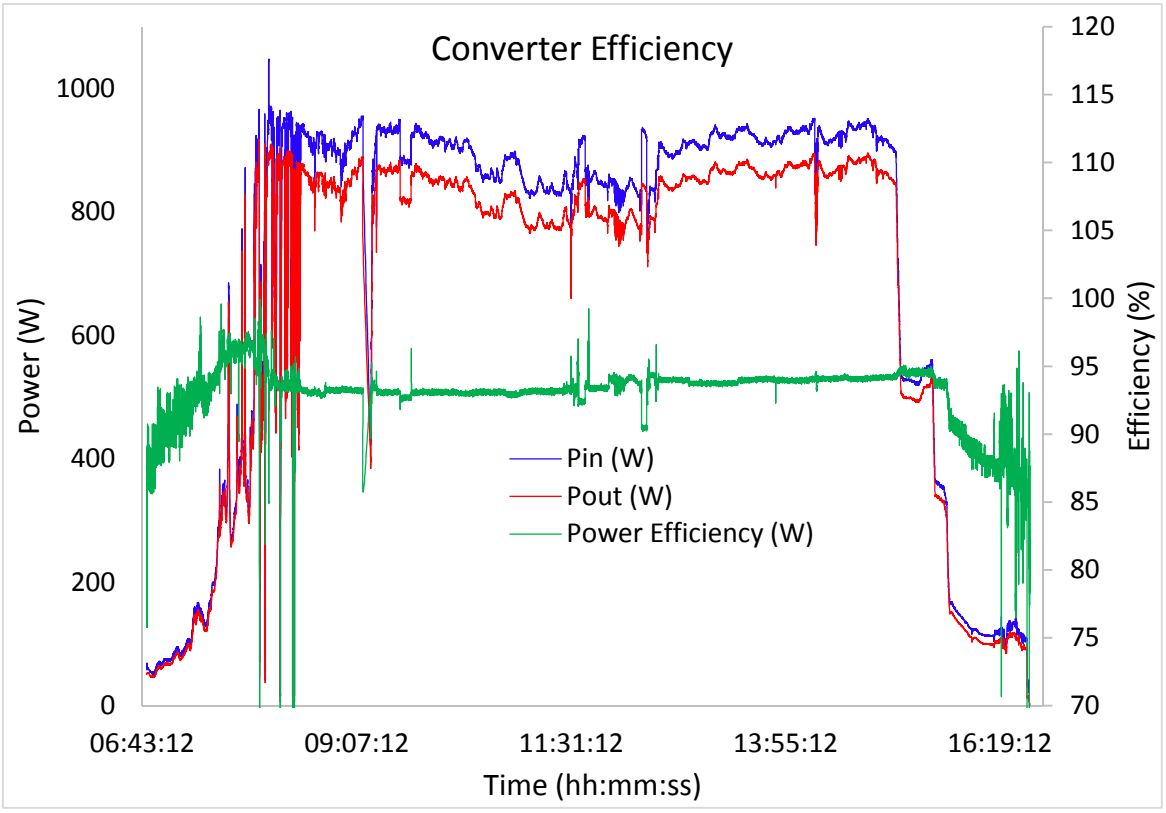


Figure 6-3: Perturb and Observe performance

The Perturb and Observe algorithm will perform better if variable stepping is implemented. Power levels of 1-kW or more were never achieved because solar irradiance changes too quickly for the algorithm to adjust to the optimal switching frequency. If a constant increment factor of 0.5-kHz is used, it can take the system up to 440 seconds (30 to 250-kHz) after start-up to find the MPP point.

6.2.2 Variable-Step Incremental Conductance

The variable step incremental conductance algorithm allows the microcontroller to track the change in solar irradiance quickly because it measures the magnitude of the change in power, voltage and current and allows the system to calculate the new set point precisely without introducing a large set point error. Because of this, the change in power seen by the electrolyser stack is the same as the change in input power. Solar irradiance changes slowly and because the output is in phase with the input (due to faster MPPT), the stack does not cause a current surge that can set off the OCP of the power supply. This increases the total system efficiency because the MPPT does not need to "search" for the MPP again. As seen in Figure 6-4, this algorithm is able to track the change in solar irradiance quickly and reaches the designed power level of 1-kW. During this test, the system was able to extract 6.535 kWh of energy from the solar panels while consuming only 0.374 kWh of this energy. The total amount of hydrogen produced at atmospheric pressure was 1436 litres and the overall energy efficiency of the power converter was 94.2 %.

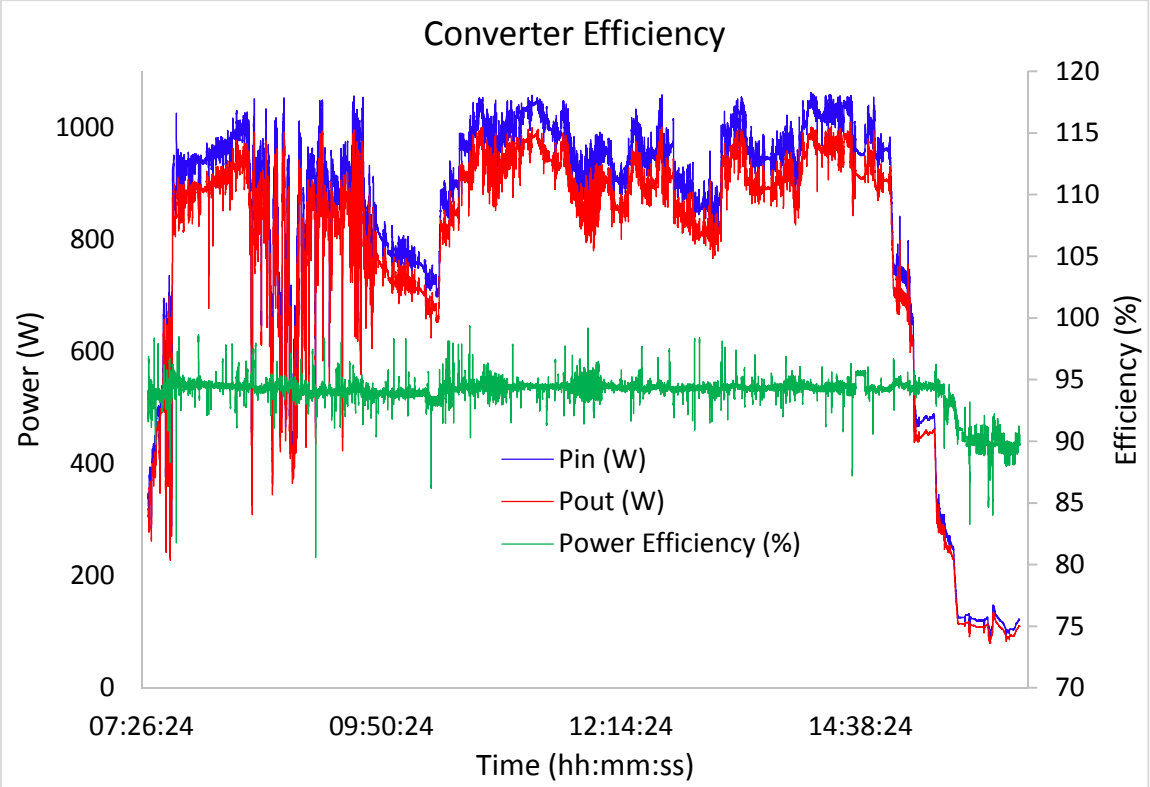


Figure 6-4: Variable-Step Incremental Conductance performance

The varying efficiency spikes seen in Figure 6-4 is caused by the varying frequency adjusting factor implemented in this MPPT algorithm. When solar irradiance reduces, the electrolyser stack is charged like a capacitor which causes a small reverse current to flow back to the power supply. If the solar irradiance increases, it will cause a large current to flow into the electrolyser stack and efficiency will drop for a moment. Integrating input and output power over time to obtain energy and then calculate the overall efficiency results in a more accurate overall efficiency calculation.

6.3 Energy Storage (Solar to Hydrogen)

In this section, the total efficiency of the solar to hydrogen system is calculated. This will take into account the estimated efficiency of the electrolyser stack and will show how the electrolyser stack efficiency was estimated. The weight (in kg) of the total amount of hydrogen produced for this test will also be calculated. Hydrogen has a calorimetric value with a lower heating value (LHV) of 120 MJ/kg [56]. When converting this to kWh, it is $\frac{120\times10^6}{60\times60\times1000} = 33.334$ kWh of energy per kg of hydrogen [57]. The data presented throughout this chapter was obtained using the Variable-Step Incremental Conductance MPPT algorithm.

6.3.1 Flow Rate

Figure 6-5 shows the output power and current of the power converter. This is the power and electrical current supplied to the electrolyser stack which was logged on a per second basis. It also shows the total amount of hydrogen produced in litres (at atmospheric pressure) and the real-time flow rate in nLPM. There is a direct correlation between the hydrogen flow rate and the electrical current supplied to the electrolyser stack.

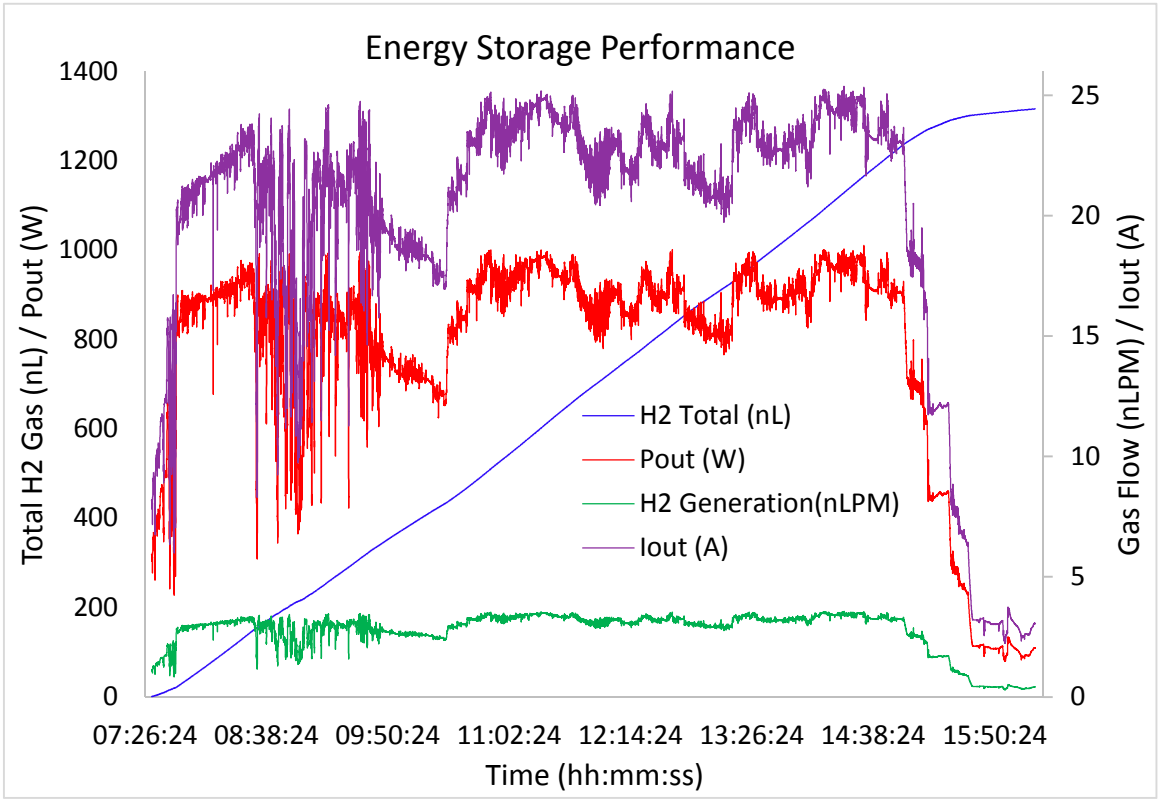


Figure 6-5: Energy storage performance

6.3.2 Energy Storage Efficiency

The purpose of this section is beyond the scope of this study, but was included to illustrate the importance of a high efficiency DC/DC converter and how it relates to the total energy efficiency of the system. By using the ideal gas law in conjunction with Faraday's law of electrolysis (mass and mole form), the total theoretical amount (in normal litres at 1 atm) of hydrogen produced by the electrolyser stack is estimated. This value is then compared to the calculated (using the current) gas flow rate which is then integrated in in real-time by the microprocessor using Euler's method of integration to obtain the total amount in normal litres per minute (nLPM). The procedure was done as follow:

Step 1: Characterizing the electrolyser flow rate

A power supply, operating in Constant Current (CC) mode, were connected to the electrolyser stack (which were connected to an electrolyser test station) and run at values between 1 to 20 A at 25 °C. The average flow rate was then divided by the average current to estimate the flow rate in nLPM per amp for each cell. The test was repeated at 40 and 60 °C to observe the effect that temperature has on the flow rate. No significant effect could be observed because the flow rate below 20 A is very low and affects the signal-to-noise (SNR) ratio of the mass flow sensor. The average of the recorded flow rates were divided by the average current and number of cells. It was then determined that the electrolyser stack will produce 0.0059 nLPM for each cell (per amp).

Step 2: Determine the theoretical flow rate

The theoretical flow rate is calculated using the ideal gas law equation:

$$P \times V = n \times R \times T \tag{6.1}$$

where P is the atmospheric pressure in Pascal, V is the volume in m^3, n is the number of moles, R is the universal gas constant in n.m.kmol^{-1}.K^{-1} and T is the temperature in Kelvin.

Faraday's law of electrolysis (molar form) is also used as follow:

$$n = \frac{Q}{2 \times F} = \frac{I \times t}{2 \times F} \tag{6.2}$$

where Q is the total charge ($Q = \int_0^t I(t).dt$), I is the current, t is the time the current was applied and F is the Faraday constant. If a varying current is applied over a total time (t) in increments of $t_2 - t_1$, then the sum of integrals must be calculated over the total time to obtain the total charge. If a current sensor was used, then the values must be integrated using Euler's method of integration.

To calculate the theoretical amount of hydrogen produced in nLPM per amp, substitute (6.2) into (6.1) to obtain:

$$\frac{I \times t}{2 \times F} = \frac{P \times V}{R \times T}$$

The equation is then re-written to obtain volume in decimetre per second as follow:

$$\frac{V}{t} = \frac{I \times R \times T}{2 \times F \times P}$$

Where $\frac{V}{t}$ is multiplied by 1000 dm³/s × 60 s to convert to nLPM.

$\frac{V}{t} = \frac{I \times R \times T}{2 \times F \times P} = \frac{60000 \times 1 \times 8.3145 \times 298}{2 \times 96485.33289101325} = 7603188.267 \times 10^{-9}$ nLPM for every 1 A (per cell).

It is important to include as many digits after the comma as possible because if this is implemented in conjunction with Euler's method of integration on a microprocessor, the estimated total amount of hydrogen produced may be greatly miscalculated over the course of a few months.

Step 3: Estimate the efficiency of the electrolyser stack

The efficiency of the stack is then calculated as follow:

$$\eta_{stack} = \frac{measured\ gas\ flow}{theoretical\ gas\ flow} \times 100\ \% \tag{6.3}$$

It was found that the electrolyser stack used has an efficiency of 77.6 %.

Step 4: Verify the estimated efficiency

By using the theoretical gas flow rate as calculated in Step 2, the total (theoretical) amount of hydrogen was calculated as 1865 litres. The measured value was 1436 litres. This results in an estimated efficiency of 77 %.

Step 5: Calculate the total weight

The total weight can be calculated using Faraday's law of electrolysis in mass form [58], the number of cells in the electrolyser stack and the total charge supplied to the stack:

$$\dot{m} = \frac{Q \times M \times x}{2 \times F} = \frac{I \times t \times M \times x}{2 \times F} \tag{6.4}$$

where M is the atomic mass of a hydrogen atom (note that in molar form it should be multiplied by 2) and x is the amount of cells in the electrolyser stack.

The theoretical weight of hydrogen (using the measured current) is 153.84 grams. To calculate the actual total weight of hydrogen produced by the electrolyser stack, the ideal gas flow equation can be re-written as follow to calculate the number of moles:

$$n = \frac{P \times V}{R \times T} = \frac{1.01325 \times 1436}{0.08206 \times 298} = 59.51\ moles$$

Note that P is given in bar and the unit for R is in L.atm/K. Also note that there are two hydrogen atoms per mole which weighs 1.008g (per atom).

The total weight produced by the electrolyser stack is then calculated from the total amount of hydrogen produced (as measured). This was found to be 119.89 grams.

Step 6: Calculate energy storage

In order to calculate the amount of stored energy, divide the weight of the measured total amount of hydrogen by 30 (equal to 1 kWh). This gives a total amount of stored energy (in hydrogen gas form) equal to 4 kWh.

6.3.3 Summary

Table 6-1 summarises the total energy conversion efficiency of the entire system.

Table 6-1: Efficiency summary

Item	E-In (kWh)	E-Out (kWh)	Efficiency (%)
DC/DC Converter	6.535	6.161	94.3
Electrolyser Stack	6.161	4	77
Total System	N/A	4	72.61

6.4 Conclusion

The conclusion can be made that the high efficiency of the LLC resonant converter makes a dramatic improvement in the overall system efficiency. If a PWM converter was used (with an overall efficiency of 85 %), the total system efficiency would have dropped to 65.5 %. The addition of synchronous rectification will improve the power converter efficiency to 97 % which would result in a total system efficiency of 74.7 %.

It should be noted that the estimates presented in this section (measured flow rate and total amount of hydrogen produced in litres) can be affected by the following factors and should be regarded as an estimate only:

- The accuracy of the mass flow meter installed on the electrolyser test station;
- Variations in the outlet temperature of the electrolyser stack;

- Resolution of the current sensors used in the power converter;
- Timer resolution implemented on the microprocessor and software application that performs Euler's method of integration on a per second basis instead of every millisecond and
- The rounding of hard-coded theoretical values programmed into the timer service routines to perform Euler's method of integration.

The implementation of ZVS based power converter proved to be a reliable option for coupling a renewable energy source (PV panels) to an electrolyser. It was also found that the OCP implementation proved to be useful when designing such a converter because a programming error will not lead to a MOSFET failure in the system. This also allows the extension of this research with minimal risk of converter failure because the non-linear behaviour of the electrolyser stack cannot cause any damage to the converter, should current surges occur during imperfect MPPT adjustments due to the system limiting the MOSFET current on a per cycle basis.

CHAPTER 7: SUMMARY, CONCLUSION AND RECOMMENDATIONS

7.1 Dissertation Summary

The purpose of this research was to test two different power converter topologies for an application specific purpose, which is to couple an electrolyser to a renewable energy source. Because renewable energy sources do not deliver constant power, a suitable power converter must be used to ensure high reliability and efficiency. In the literature study, the different topologies were researched and it was found that the full bridge topology is suitable for high power densities. The MOSFET was also researched and the main causes of failure (steep dv/dt slopes, activation of the parasitic BJT, slow reverse recovery of the body diode, voltage and current transients) were fully investigated and documented. Snubber circuits were implemented and tested on the hard switching converter to avoid the causes of MOSFET failure from occurring. It was determined that a soft switching technique will not only increase the efficiency, but also the reliability of a power converter. A PWM and PFM converter was designed, simulated, built and tested using the full bridge configuration and the corresponding waveforms associated with poor efficiency and low reliability could be observed in the hard switching converter. In the soft switching converter, a higher efficiency (compared to hard switching) was validated and the absence of the Miller effect was also documented.

7.2 Conclusion

The simulated MOSFET waveforms matched that of the measured waveforms which validates the design. It was also proven that synchronous rectification can improve the efficiency of the power converter by enabling soft switching on both the primary and secondary side of the power converter. Two different MPPT algorithms were tested on the LLC resonant converter and the result proved that variable stepping improves the MPP tracking speed when the power converter is coupled to a renewable energy source. This improves the energy efficiency because the algorithm allows a quicker and more precise output response to the varying input conditions caused by a renewable energy source such as a PV array. The converter also proved to be reliable and was able to extract more than 12 kWh in two days without failing. Implementing short circuit protection proved to be necessary when developing a power converter because it will eliminate the possibility of component failure and therefore eliminate unnecessary delays due to power converter failure or repair time. It was also observed when powering on the power converter with the electrolyser stack already connected will cause a large current spike. This is because the electrolyser stack represents a large capacitor which is initially discharged before the power converter is switched on for the first time. This can cause a power converter failure if no short circuit protection is implemented, however it is also not preferred to shut down the converter immediately when a current spike is detected. It is instead recommended to allow a few high current pulses (with a cycle by cycle duty cycle limit to limit the magnitude of the current) which can be specified by the developer, in conjunction with a time limit for the maximum number of pulses. The time limit is used when the overcurrent pulses (which may not be consecutive) are caused by the adjustments of the MPPT algorithm and the capacitive behaviour of the electrolyser stack. This allows the converter to distinguish between a real short circuit and the capacitive behaviour of the electrolyser stack that may mimic a short circuit behaviour for a short moment. If a short circuit does occur, then the system will allow a few pulses (while limiting the current pulses experienced by the MOSFETs, thus protecting them) and if the pulses reaches the timeout limit, the converter will shut down safely.

7.3 Recommendations

The LLC resonant converter's gain can be reduced by increasing the switching frequency, but this alone is not enough to allow the converter to achieve any voltage below the designed voltage. Therefore it is recommended to implement pulse skipping in conjunction with frequency control to enable the converter to have a wider output voltage and current range. It is also recommended to design the converter for a higher switching frequency because this will reduce the size of the transformer and will require less copper windings. This will reduce manufacturing cost while improving efficiency.

APPENDIX A – SHORT CIRCUIT PROTECTION

Figure A-1 shows the circuit that was designed and used (for reference purposes only) for short circuit protection. It makes use of a high frequency Current Transformer (CT), indicated as V4 in the figure, and a LM393 voltage comparator. If the voltage generated by the CT exceeds the reference voltage created by the resistor divider R1 and R2, then the comparator will generate a digital output corresponding to a 1. This output pin is then connected to the microcontroller's timer break interrupt pin and was used to implement the advanced short circuit protection features. The resistors R1 and R2 can also be replaced by a digital potentiometer which will allow the adjustment of the current threshold while the system is running.

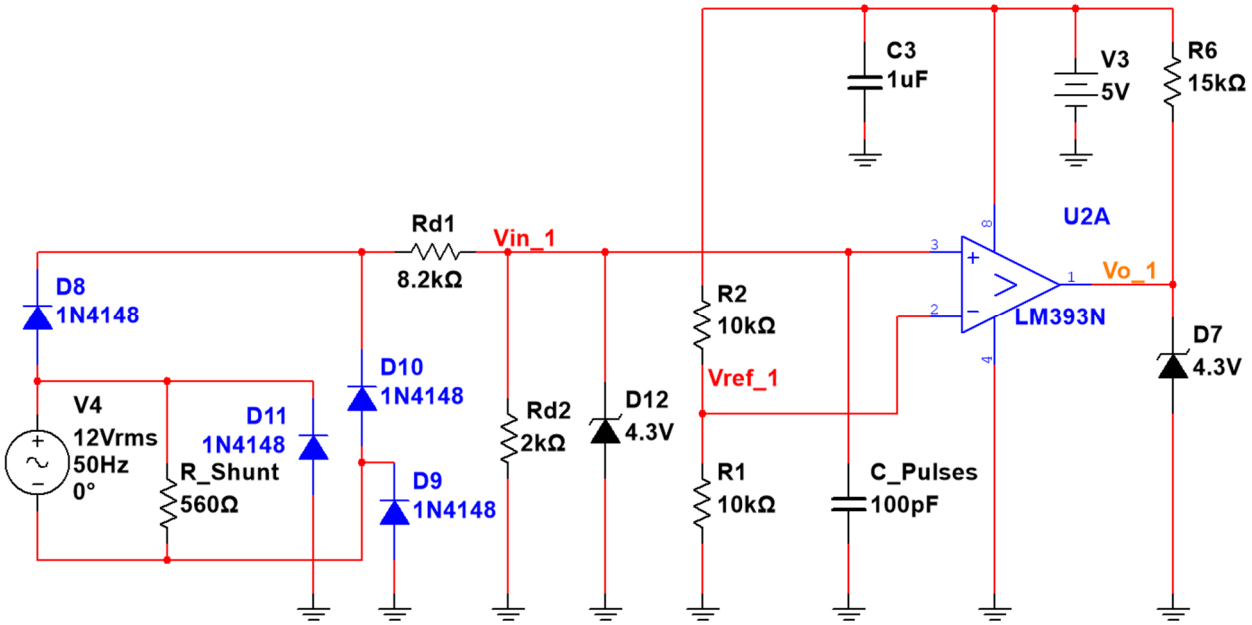


Figure A-1: Overcurrent protection circuit

Figure A-2 shows the menu (not targeted towards the end user, but the developer) where adjustments can be made while the system is running. It allows the calibration of the voltage and current sensors and also allows for DC offset correction. System variable states and a terminal window are also displayed to ease debugging of the firmware. The system frequency and dead time can be adjusted manually (open loop control) and also allows for the selection between different MPPT algorithms for research purposes.

The instant-off SCP will shut down the power converter if a single current pulse is detected in the high voltage LLC resonant tank circuit that exceeds the defined peak current value. This value is adjustable from 0.1 to 25 A in 0.1 A increments. Advanced cycle by cycle current limiting was also implemented which will limit the duty cycle (and consequently the current) of the high voltage MOSFETs instead of shutting down the power supply completely. The maximum number of OCP pulses can also be specified and the maximum OCP pulse count per time base can also be specified under “TIM2 Control”. This provides full short circuit protection of the high voltage MOSFETs while preventing the developer from accidently causing a MOSFET failure in the event of a programming error. It also allows the safe start-up of the power converter if the electrolyser stack is already connected to the power converter and it is switched on for the first time.

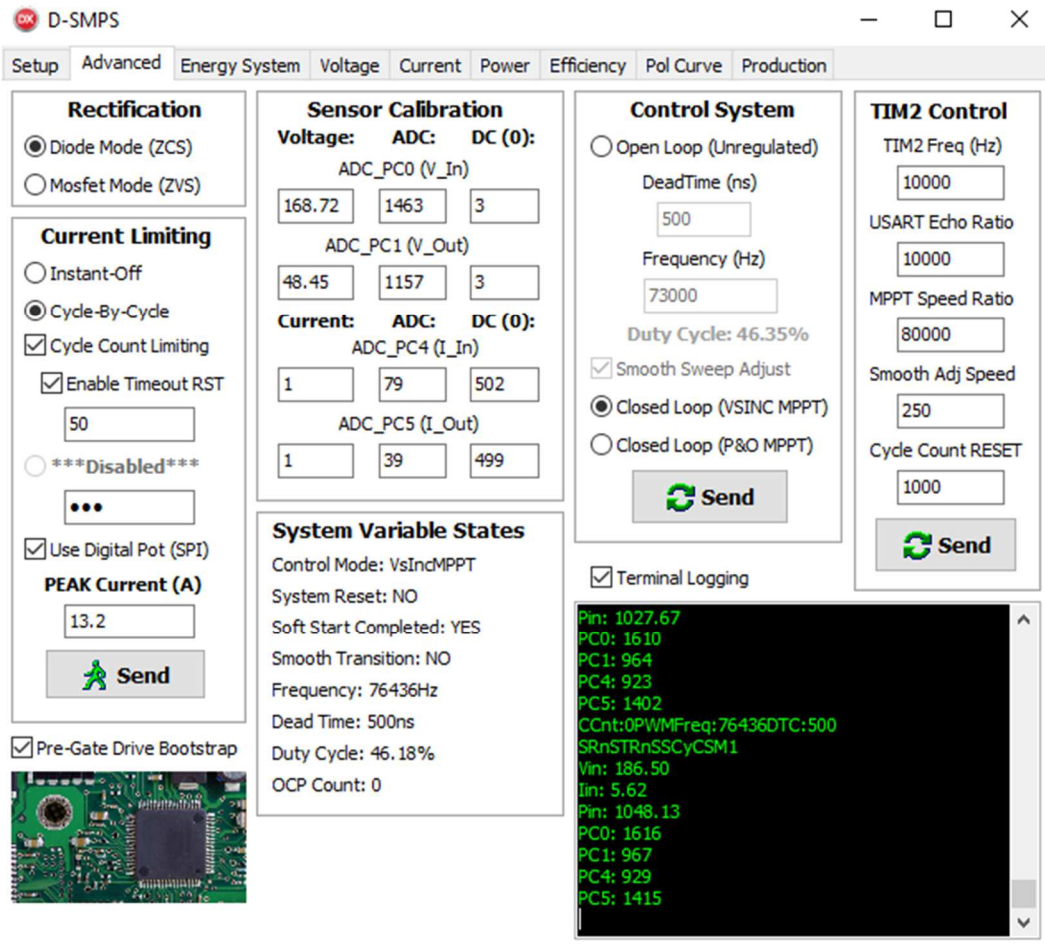


Figure A-2: Advanced control system menu

APPENDIX B – ISOLATED VOLTAGE SENSOR

Figure B-1 shows the circuit diagram of the isolated voltage sensor. V1 is the voltage to be measured and V3 is an isolated 5 V source that can be made using a single B0505S-1W converter. V2 does not need isolation and can be provided from a USB port. The microcontroller ADC is connected to R2_ADC0. This circuit provides a safe method of measuring high voltages where the ground of the microcontroller is not at the same voltage level as the ground of the voltage being measured. This eliminates the risk of damage to the computer's USB port. A full design procedure for this circuit can be found in the HCNR200-300E or IL300 dual optocoupler datasheet.

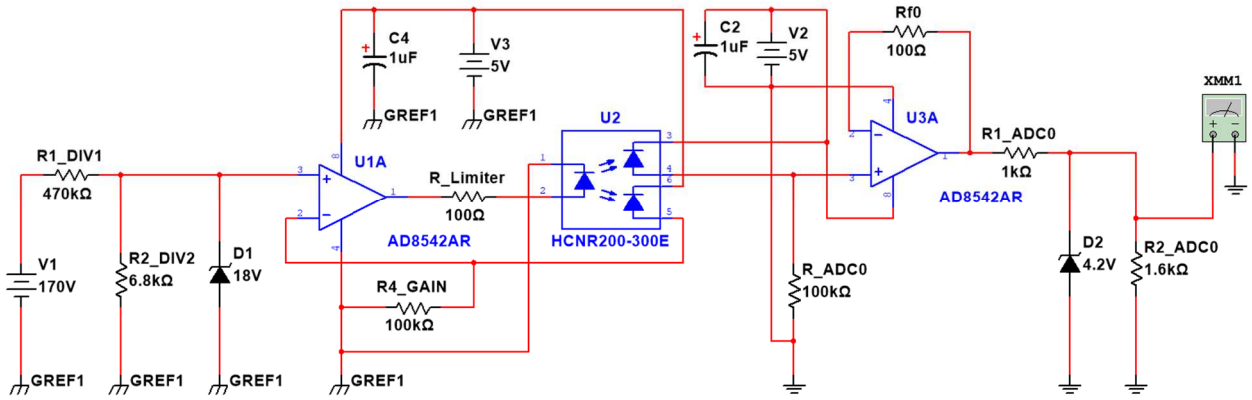


Figure B-1: Isolated voltage sensor

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