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Ruan van den Heever
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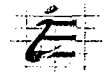


NORTH-WEST UNIVERSITY
YUNIBESITI YA BOKONE-BOPHIRIMA
NOORDWES-UNIVERSITEIT
POTCHEFSTROOM CAMPUS

Real Time Remote Heart Rate & ECG Monitoring for the Modern Sport Scientist - a front end design -

Ruan van den Heever

A dissertation submitted in partial fulfilment of the requirements for the degree Magister Ingeneriae in Computer Engineering

Supervisor: Prof. Willie C. Venter (PhD)

2007

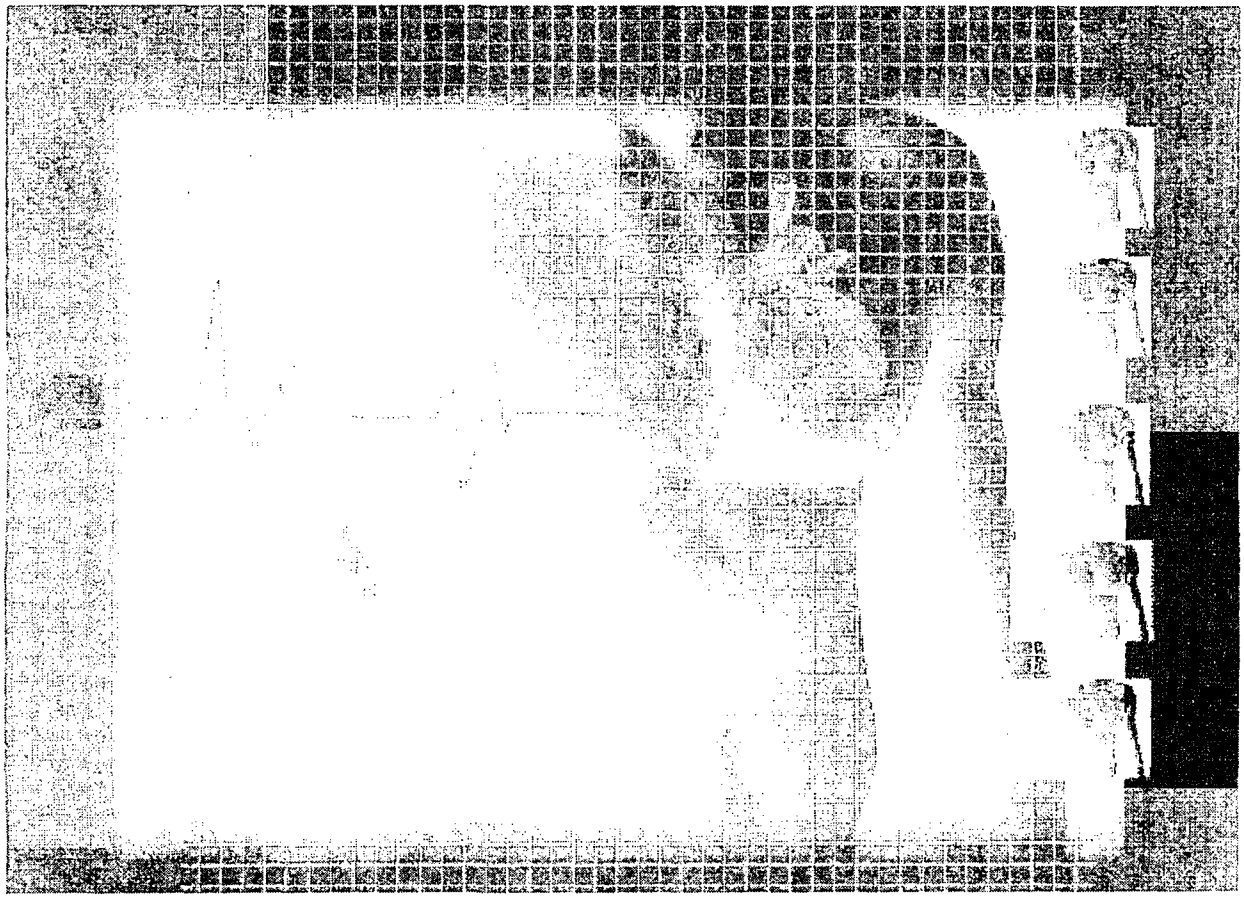
Potchefstroom

The scientific curiosities of today are the catalysts and social dynamos of tomorrow. This requires no elaboration in an epoch which has witnessed the explosive emergence of nuclear physics from academic study and the laboratory into the fields of public utility and international controversy. The development and application of a particular scientific technique depends in part on need and in part on the elaboration of its theoretical significance and of robust experimental methods.

G.K.T Conn
Department of Physics; University of Exeter,Exeter, England

Dedicated to my sister,

Zelna



International Accreditation

Patent Application

The work presented in this dissertation has been handed in and awarded a preliminary international patent depending on final submission to the PCT commission in Geneva Switzerland in September 2007.

Patent: SUID-AFRIKAANSE PATENT AANSOEKNOMMER 2006/07480 GETITELD: "REAL TIME MONITORING SYSTEM AND METHOD OF ELECTRICAL SIGNALS RELATING TO AN ATHLETE'S HEART ACTING" IN DIE NAAM VAN NOORDWES-UNIVERSITEIT

Refer to Appendix E for the full text concerning the international PCT application.

International Conference Exposure

The research and developed product presented in this dissertation have also been presented at two international conferences during 2006.

1. "The international Conference on Sport Technology and development toward sport performance"
   21-23 September 2006, Faculty of Sport Science, UiTM (Universiti Technologi MARA), Shah Alam, Malaysia

2. "The international Conference on Sport Science"
   21-26 December 2006, Faculty of Sport Science and Faculty of Engineering, UPM (Universiti Putra Malaya), Selangor, Malaysia

Preface

The development of digital systems, parallel and dual processing has improved to such an extend in the past decade, that ideas thought to be impossible even five years back, are now considered to be old technology.

The development of the hardware needed for this project makes great use of this idea. Whereas previously simple analogue filtering was insufficient to retrieve wanted signals from within extensive white noise levels, modern digital signal processing techniques in conjunction with simple analogue filtering are implemented to retrieve signals for the purpose of this project.

Taking into account that the objective of this project is the real time remote monitoring of the heart rate and electro cardio graph of an athlete during active sport participation, the utilization of wires between the athlete and the monitoring system is not possible. The only feasible solution to the problem is the use of RF (radio frequency) communication. Monitoring an electro-cardio-graph of any one person requires high accuracy of data as well as high speed data transfer between the subject being monitored and the observer. It also places a large amount of stress on the transmission protocol.

The further capabilities of the system to allow different athletes to be monitored at the same time is realised through the implementation of different RF frequency channels in the communications link as well as dual processing of data to ensure constant and reliable real time information to the observer.

Executive summary

A need exists to optimise the efficiency of the way athletes are trained in the professional sports environment. Since it is a multiple variable problem with constraints, it provokes the need for sophisticated research, control and design.

A control and monitoring system will be developed for the scenario where the operating range is between 0 and 50 degrees Celsius, the accuracy of the system is at least within a margin of plus or minus 10% and will be within the financial reach of the average and above average athlete and trainer. The system will be implemented in the sport science department of the North-West University.

The system behaviour under working conditions will be investigated on the athletics track indoors and out. A simplified model will then be created in software packages such as Orcad and Labview (referencing the technical design). Techniques such as '*Fuzzy Logic Control*' and '*Model Predictive Control*' will then be implemented in the final version of the control software, especially where it concerns the heart rate and electro-cardio-graph monitoring equipment.

A literature study as well as extensive research (based on statistical outcomes) and experimentation should give an indication of the level of sophistication needed for the finalization of the project as well as the feasibility of the outcome.

With the newly available heart rate and electro-cardio-graph information in real time at the hands of the athlete trainer, a study will be made of the advantages and possibilities of such a system in the modern athletes training and sporting program.

Acknowledgements

I would like to express my gratitude to the following people in no particular order;

Prof. Willie Venter, for all the financial support, for accepting my stubbornness and for asking all the leading questions.

Prof. Dawie Malan, for the opportunities created by you and for advising on the requirements of such a system.

Dr. Rudi van der Walt, for your anticipation and constant interest in the system. For all the opportunities created, identified and reacted upon by you and for your financial support.

Janny Whitelock, for doing all the work you have done on such short notice, for excellent work delivered and for your patience with all my mistakes.

Yolandi, for understanding; Your quiet support is of inexpressible value.

My mother, Ina van den Heever, for receiving all the "nanos", and all the phone calls to me.

My father, Kennedy van den Heever, for all your support, help, time and leadership.

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Literature & Background Study

PART II... . Front-end Design

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PART III.....ECG Acquisition Circuitry Design

Design Documentation

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*Please refer to appendix G for some full colour illustrative pictures representing the different components as designed in this project.

*Please refer to the DVD in appendix G for a full length video illustrating the outcome of this research.

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ABREVIATIONS

IR	-	Infra Red
RF	-	Radio Frequency
ECG	-	Electrocardiogram
GPS	-	Global Positioning System
IC	-	Integrated Circuit
FM	-	Frequency Modulation
AM	-	Amplitude Modulation
OP AMP	-	Operational Amplifier
ADC	-	Analogue to Digital Converter
mW	-	Milli-Watt
ISM	-	Industrial Scientific and Medical (Radio bands)
IA	-	Instrumentation Amplifier
IF	-	Intermediate Frequency
AI	-	Artificial Intelligence
PC	-	Personal Computer
SDS	-	Sudden Death Syndrome
CMR	-	Common Mode Rejection
CMRR	-	Common Mode Rejection Ratio
FIR	-	Finite Impulse Response
IIR	-	Infinite Impulse Response
TTL	-	Transistor-Transistor Logic
LPF	-	Low Pass Filter
HP / HPF	-	High Pass / High Pass Filter
DSP	-	Digital Signal Processing
SOIC	-	Small Outline Integrated Circuit
PPM	-	Parts per Million
RTI	-	Return from Interrupt
DRL	-	Driven Right Leg

Literature & Background Study

- Note: Although this document is written with patient safety in mind, any ideas and design proposals as well as thoughts expressed are not by themselves necessarily compatible with all *system* safety requirements; anyone using any ideas in this document must ensure that, in a particular design and application that design and application as a whole meets required safety criteria.

1. Purpose of this Research

Purpose of the Research

s an athlete is becoming more of a professional sports-practitioner, training hours get longer, athletes and coaches keep pushing longer and harder and fitness and stress levels on the body keep extending just a little further. Monitoring the heart rate and ECG of an athlete can provide the athlete but more specific the professional coach with much more than just fitness-level information. Monitoring the heart rate and ECG of an athlete can provide the coach with critical medical information regarding the health of the athlete.

It is too often that one reads an article about an athlete or sports-personality who has suffered from medical conditions whilst competing, more than two out of ten with fatal consequences. For this reason and many more, important to the sport science world, optimally controlling, monitoring and measuring the heart rate and ECG of an athlete makes up the purpose of this project. Since it is a multiple variable problem with constraints it provokes the need for sophisticated research, control and design.

The objective of this project is to develop a full scale, real time remote ECG and heart rate monitor to be used on athletes over a large distance. The monitor must be small enough and light enough so that it can be fitted on an athlete while training or competing. The means by which the monitor will be fitted to the athlete is not defined, but must comply to all sports regulations. Further more all sub-systems surrounding the ECG and heart rate monitor including the hand-held controlling unit, the data relay units the computer software and all firmware running on and controlling the heart rate monitor, hand-held controlling unit and relay units must also be developed so that the final output of the system can be tested and evaluated.

With the latter as the secondary objective of this research the primary objective of this research is filter design. An optimal filtering process for obtaining a true and accurate ECG signal from a *moving athlete* has to be researched. The final outcome will most probably consist of a mixture of analogue and digital processes. The final objective is to integrate the analogue and digital filtering worlds to such an extent that a clean true and accurate ECG signal will be available for further processing and data extraction within the rest of the control system.

The information given by a system like this will aid in the growth and progression of professional level training programs, as athletics and sports in the wider context is not a social event any more but is becoming a means of income and world class competition more and more every day.

2. Research Methodology

Research Methodology

Basically this dissertation constitutes four different stages. The first stage will focus on a literature and background study. The second stage focuses on deriving mathematical models for the control and design mechanisms, this stage also focuses the attention on the development of tested designs and possible updates during development. Next the implementation process followed by testing, evaluation and a conclusion.

2.1 Literature Study

Literature Study

Although the project is about designing and implementing a real time remote ECG and heart rate monitoring system for athletes, understanding the bio medical aspects of the human heart and body will be of great help from an engineering point of view when the system needs to be designed and implemented.

Time will be spent on researching the human heart rate and ECG signal provided by it. The help of experts in this field as well as sport scientists will be attained to complete this part of the literature survey.

A literature study as well as extensive research (based on statistical outcomes) and experimentation should give an indication of the level of sophistication needed for the finalization of the project as well as the feasibility of the outcome.

2.2 Design and Development

Design & Development

Because the system to be considered in this research is complex, it might become difficult to determine optimal rules for final designs. The reasons for the complexity of the system are forthcoming. Data transfer between different units must meet certain speed criteria to enable the system to work in real time. Aside from being able to transfer data between different units, the system must also be able to keep data on different units up to date to ensure redundancy. Communication issues are sure to play a key role in the system design. As wireless communication must be used in order to supply the system portability, transfer rates, error checking and encoding will all be playing a key role in the success of the outcome. Also, the human body is not predictable in the sense of electrical potentials generated, movement and noise generated by muscles. Ridding the ECG signal from any or all of these types of noise and imperfections will most certainly proof to be a complex task. Most design schemes are *rule based* and this in specific might present various issues to be dealt with whilst designing the heart rate monitor. This will lead to the study of generic algorithms in order to extract a rule scheme that will control the heart rate monitor optimally.

2.2.1 Modelling Dynamics

Modelling Dynamics

The modelling of a remote ECG and heart rate monitor for athletes is a

difficult task to accomplish in the laboratory, although certain aspects of the analogue circuits may be modelled on software packages like ORCAD and MATLAB. Basic modelling will have to be done with the aid of statistics gathered during the development and testing phase and further extensive testing will have to be done in the field in order to attain true and accurate feedback.

2.2.2 Controller Development

Controller Development

Because of the complexity of a remote ECG and heart rate monitor for athletes it will be necessary to develop a certain amount of *support equipment* in order to make the heart rate system functional and credible for testing, evaluation and implementation. A multi-input and multi-output hand-held controller unit will be designed along with the ECG and heart rate monitor based on the dynamics of the models derived and the functionalities found necessary. This hand-held controller unit will be able to communicate with the remote heart rate monitor via RF communication and will be able to send and retrieve any data found necessary during development of the system to and from the heart rate monitor. In order to grasp the idea of a remote ECG and heart rate monitor and to understand the idea of a hand-held controller unit better, refer to the graphical representation of the idea in figure .

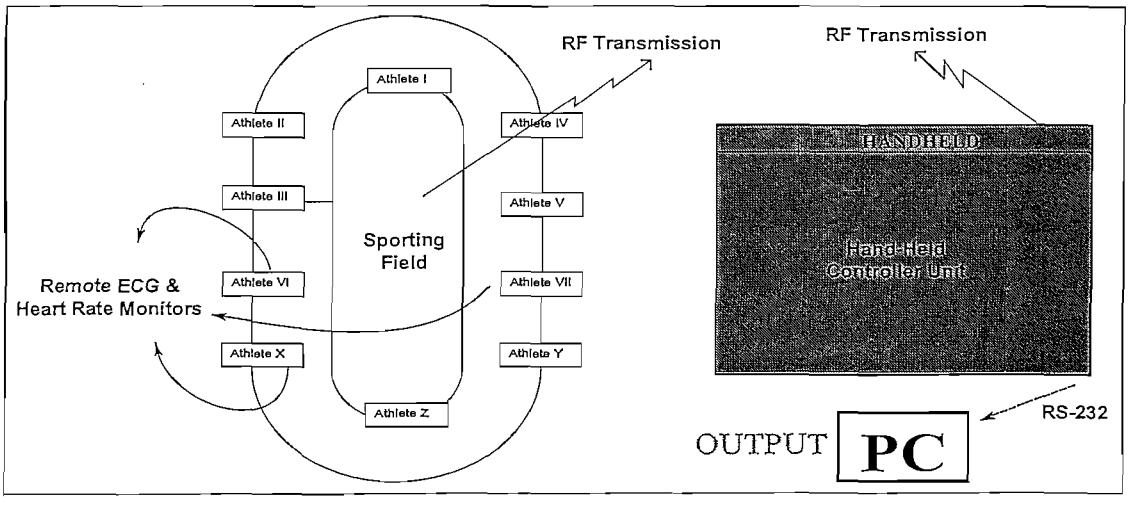


Figure 1: Initial Graphical Representation of Overall System

It was originally thought that direct communication between the remote heart rate monitors and the hand-held controller unit will not be sufficient for operation of this system due to one major issue presented with the implementation of RF as the primary communication technique between the remote heart rate monitors and the hand-held controller unit. As will be discussed later, this was the case. The issue at hand is communication (data packet) loss. This is one of the largest shortcomings of similar systems on the market. As will be discussed and graphically represented in figure 4, it was found necessary to add data relay units between the remote heart rate monitors and the hand-held controller unit in order to ensure continuous and reliable communication between the heart rate monitors on the athletes and the hand-held controller unit on the side of the field in the hands of a third person.

Further more, self adjusting software has to be designed to control the ECG and heart rate monitor in order to ensure that heart beats (pulses) will be detected correctly. This software might be seen as artificially intelligent although it will not be developed with this in mind. The software controlling the ECG and heart rate monitor will be able to predict when a new heart pulse will be present in the analogue signal picked up from the human body, and by means of this type of AI, noise and false pulses will be eliminated. The self adjusting aspect of the software will prove to be important when the heart rate of an athlete starts increasing and decreasing. It will be necessary for the software to be able to predict when a heart pulse will be present in the signal and this will only be possible if the software is able to adjust according to increasing or decreasing heart rate.

Research also has to be done on different RF communication techniques. RF communication is a field to be studied on its' own and falls well outside the scope of this dissertation. Because of the complexity of this communication method as well as the complexity of implementing RF communication into any electronic system, only the practical issues surrounding this part of the project will be discussed. For example, reasons for choosing FM, in stead of AM as a modulation scheme for the RF communication, and in depth discussions about how to design wide band FM

receivers will be left out. This text will only include design issues surrounding the practicality and placement of RF transmitters and receivers to ensure communication at all times and reduce interference to and from the remote ECG and heart rate monitor.

2.3 Implementation

Implementation

Firstly the models for the control mechanisms will be constructed with the aid of a system identification toolbox in Matlab and ORCAD. The control mechanisms include the electronic circuitry, communication aids, software and memory devices on both the heart rate monitor as well as the hand-held controller unit. The RF antennas, ground planes and their placement on both the hand-held controller unit and the heart rate monitor will be developed with the aid of RF design experts. Modelling the hand held unit will be a difficult task as the output of the hand-held controller unit depends on a continuous stream of input from one or more ECG monitors. Simulating this stream of input data is not easy as the data as it will be received in the real world will proof to be inconsistent and randomly different as subjects will vary. This unit will be tested after careful design, development and consideration of all constraints.

For testing purposes the entire system will be implemented in Potchefstroom at the sport science department of the North-West University. Athletes training and students studying at this department will use and evaluate the system.

2.4 Testing and Evaluation

Testing & Evaluation

It is very important to evaluate all work done. The hand-held controller unit to be implemented will contain non volatile memory which will be used to save any data transferred from the remote heart rate monitor during operation. This will be but one redundancy technique to be designed into the system in order to validate the results expected. The hand-held controller unit will also be able to continuously

download all data received from the remote heart rate monitor to a laptop or desktop computer via serial communication, where a higher level software package which will be developed in a language of later choice will receive and analyse the data. This software package will be able to send requests to the hand-held controller unit which in turn will transmit the request to the remote heart rate monitor and then wait for a response. This type of architecture will allow for real time as well as delayed validation and evaluation of the system.

Testing is one of the most important events in any project. Testing of this project and the sub-parts of the system will be done as development continues. This has to be done in order to make sure that the assumptions and designs for the next phases will be correct. In any project that needs the accuracy levels of this one, continuing to some later designs are dependant on the success of the previous designs.

3. Background and System Subcategory Overview

Background

Technology is the heartbeat of development in the present day. Whether only improving on a previous design or defining a brand new idea. Smaller is better and faster is cheaper.

Who would have thought about a cellular phone even twenty years ago!? The bare naked idea of talking to someone in a remote location on an instrument with no wires attached to it, the size of a small pocket calculator, was a technological idea still to be discovered.

As time went by and continues development progressed, the idea of wireless communication and data transfer grew stronger. Today this is a global issue and communicating with someone or transferring data between continents by means of wireless methods can be done in more ways than one.

Infrared (IR, as will be referred to in the rest of this text) or Radio frequency (RF, as will be referred to in the rest of this text) communication methods can be seen in almost every household. Remote control switches (for car alarms, house alarms and many other applications), cellular phones, IR remote controls (for television sets, video recorders, etc.), digital satellite television to mention only the most common applications. Missile guidance and communication systems, GPS (Global Positioning Systems) and space technology are somewhat more complicated applications.

The fact is, wireless communication systems, electronic components and integrated circuits (IC's) have improved to such unimaginable extent over the last ten to fifteen years that this type of communication methods are becoming even cheaper than the now old fashioned wired systems.

Control, monitoring and measurement are the main components to successfully justify the purpose of this project. Because sport in the broader sense of the word is becoming more of a professional career than just a means of relaxation, new and more advanced training facilities and programmes need to be developed. Together with the more elaborated training and fitness programmes more advanced and better means of control over the limitations of the human body is needed.

3.1 Heart Rate & ECG Monitoring Equipment

The Monitoring Equipment

Heart rate is becoming more than just the means by which a human is declared dead or alive, to stretch the definition a little.

thletics coaches and trainees themselves are becoming all the more interested in the heart rate of an athlete and other related information based on the heart rate. For example, blood oxygen levels, heart pulse width, strength and heart muscle stress etc. This data can be extracted from the heart rate of a person by means of different mathematical manipulations of the *tempo of change* of the heart rate. This type of information is important to the coaches and trainees in order to

construct a useful and potential driven training program. A well defined example of this implementation will be rugby coaches who need this information to know when to replace a certain player on the field with a reserve player. The application of such a system as will be developed in this research though, stretches far beyond rugby and can be applied on a much broader base with benefits to virtually the total sports environment as we know it today.

Bio kinetics and sport science are but two other fields where the heart rate and ECG information of an athlete is of utmost importance. Based on the heart rate of an athlete the coach for instance, is capable of adjusting the training program to suite any individual. The trainer is put into a position to be able to tell if an athlete is strained too much or can be driven harder.

The health of an athlete, overall, is one of the most important aspects in the trainer-trainee relationship, especially taking into account the level of professionalism in the sports environment today.

For even more justifiable reasons which lead to the research and design of a real time remote ECG and heart rate monitor, refer to Appendix B for a short description and elaboration on the topic of *SUDDEN DEATH SYNDROME,* one of the most debated topics in the sports environment today.

3.2 ECG Background

ECG Background

3.2.1 ECG Acquisition Requirements

ECG Acquisition Requirements

An ECG is a recording of the electrical activity on the body surface generated

by the heart. ECG measurement information is collected by skin electrodes placed at designated locations on the body. The ECG signal is characterized by six peaks and valleys labelled with successive letters of the alphabet P, Q, R, S, T and U.
(see figure 2)

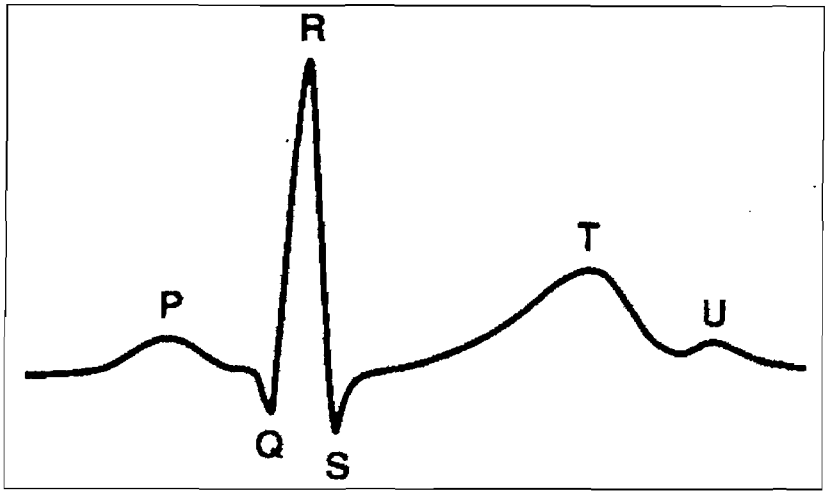


Figure 2: Typical ECG-Monitor Output.

Figure 2 with acknowledgement to Enrique Company-Bosch and Eckart Hartmann, Analog Devices.

3.2.2 Electrical Changes in the Heart

Electrical Changes in the Heart

As the body fluids and tissues are good conductors of electricity, the electrical activity within the heart can be detected by attaching electrodes to the surface of the body. The pattern of electrical activity may be displayed on an oscilloscope screen or traced on paper. The apparatus used is an electro cardio graph and the tracing is an electrocardiogram (ECG).

The *normal ECG* tracing shows five waves which, by convention, have been named P, Q, R, S and T as described above. (Differences exist between normal, stress-related and intensive care ECG tracings. All of the peaks and valleys as described on page 9 do not apply to the different tracing methods. For the purpose of

this application and extracting the heart rate from the ECG signal, the normal tracing is enough.)

See Appendix A for a short description on SA nodes, AV nodes, AV bundles and Purkinje fibres which will describe the presence of the P wave.[3]

The T wave represents the relaxation of the ventricular muscle.

The ECG described above originates from the SA node and is known as a sinus rhythm. The rate of sinus rhythm is 60 to 100 beats per minute. A faster heart rate is called tachycardia and a slower heart rate, bradycardia. [3]

By examining the pattern of waves and the time interval between cycles and parts of cycles, information about the state of the myocardium (where the word myocardium is derived from the medical term *cardium* meaning **heart** and *myo* meaning **muscle**) and the cardiac conduction system is obtained. The cardiac conduction system is a complex electrical conductive system surrounding the heart. With cardiac conduction understood in the medical world as the electric potential transferred from one part in the heart muscle to another and so the different waves in the ECG are formed.[17]

The main objective of this project and study however is not to be able to trace a perfect ECG but to be able to predict the heart rate of a person to the extend of very high accuracy. In order to be able to control the accuracy level of prediction, a more precise ECG will be of great value. The section on technical background will shed more light on this.

As figure 3 demonstrates, the timing factors of the heart beat can be derived from an electro cardio graph signal. By examining this signal and making predictions based upon the heart beat period that can be derived from the signal, the heart rate can be extracted with the aid of some not too complex mathematics.

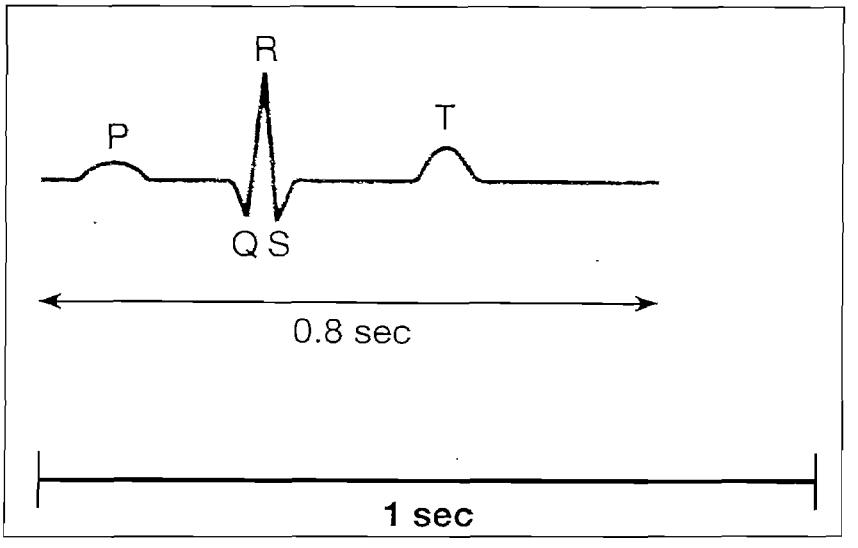


Figure 3: Typical Heart Rate Period

Figure 3 with acknowledgement to Ross and Wilson, Anatomy and Physiology In Health and Illness

As can be seen from figure 3, once the period of a heart beat cycle can be determined, the heart rate can be extracted.

3.3 System Outline

System Outline

3.3.1 Current Systems

Current Systems

Various other products are available on the market for obtaining heart rate during sporting event training sessions and for personal use. All of these products make use of the following concept. The ECG signal is picked up by means of some kind of sensors (usually IR related) placed on the body of the athlete. Two electrodes placed inside a plastic strap, strapped around the upper torso of the athlete makes contact with the skin and ensures conduction of the electrical signals. The units also contain some kind of microcontroller which, from the density of oxygen in the blood of the athlete (if the IR technique is used), or small electrical differences in skin contact

(if the ECG and electric potential difference method is used), determines the heart rate and stores the data on some kind of memory device. Three of the top brands on the market today also implement some kind of RF transmission device on their heart rate monitors, which can unfortunately only transmit the data over a very short distance to a watch worn on the athletes arm. Thus, a lack of real time data is intrinsically built into the heart rate monitors. One of the well known brands originating from Finland tries to transmit the data in real time, but, unfortunately still experiences some (every time the athlete wearing the device turns his/her back on the RF receiver data is lost) data loss during real time transmission due to several RF issues of which the biggest one is the loss of the so called *line-of-sight* concept. Two demonstrations of this particular system was attended but unfortunately no personal testing was allowed. Line-of-sight is a common problem in RF applications where low power transmissions are used. *Refer back to the bottom of page 4 as well as the bottom of page 14 for elaboration on this concept.*

Because the purpose of most of the available heart rate monitors is simply to determine the heart rate of an athlete, no other commercial product making use of the actual ECG signal to determine the heart rate could be found. It is relatively easy to construct a monitor making use of IR to determine the oxygen level in a humans' blood. When blood is oxygen rich, the colour of blood is lighter and when it is oxygen poor, the colour of blood is darker. Thus, more or less of the transmitted IR light will be reflected depending of the density of oxygen in the blood. When the heart beats, blood is pumped through vanes. With each pump the blood density becomes higher and when the pump action is over, the density decreases. The heart rate is then determined based upon the amount of reflected IR light. This is also the most common technique implemented in heart rate monitors used in hospitals. A small IR transceiver in clipped over the thumb of the patient and heart rate is detected by means of the above described procedure. More complex ECG and heart rate tracing equipment is used in intensive care units as well as in operating rooms. This type of equipment is developed for use on patients lying in beds and not inducing any unnecessary movement that causes noise (noise is also known as *common mode* in the electronic world and the meaning behind this term will become more clear as this dissertation

progresses) which will destroy the ECG signal and thus rendering its use for determining heart rate useless. It might be a good time to stress the fact that the research done for this dissertation will be based on facts but, the actual implementation of different techniques might be a result of practical consideration. Very complex ECG and heart rate monitors exist, but none of them have been designed with the idea of using it on a moving subject inducing unwanted and unpredictable common mode.

3.3.2 Forthcoming Development

Forthcoming Thesis Development

Where most available systems to the sport environment fail to comply with the modern sport scientists' needs, is the lack of continuous, accurate, *real time* availability of the extracted data over a large (further then 50m) distance, typically across an athletics field, rugby field or soccer field. Heart rate is determined and stored only to be available for download after a training session or sporting event. For the modern sport scientist it is crucial to have this information at hand during a sporting event.

When a rugby game is played and heart rate is monitored by any one of these available market products the sport scientist can download the data after the game has been played. It then takes about two to three days to work through all the data, extract necessary information draw up graphs and come to certain conclusions. If the team has been playing and practising in different manners three precious training sessions (one each day) have already been misused before the information gets from sport scientist to coach and team.

As discussed before in section 1.2.2 on page 3, developing and designing a real time ECG and heart rate monitoring system implies the development of a few sub-systems supporting and justifying the remote ECG and heart rate monitor and its output.

Included in these subsystems are a hand-held controller unit for requesting the heart rate of a specific athlete on the sports field, receiving back the heart rate and displaying the result on a graphical display.

Further more, practical issues surrounding RF communication does not allow for direct communication from the hand-held controlling unit to the athlete. The main reason for this is the human body itself. If the remote heart rate monitor is placed on the chest of an athlete it means that the antennas for transmitting data is shielded by the body of the athlete from the hand-held controller units antenna. If the remote heart rate monitor is placed on the back of the athlete the same situation will present itself if the athlete turns around.

Rather it will be necessary to design and implement *data relay units* which will be placed next to the sporting field. From the hand-held unit, communication to these data relay units will be implemented at a *specific radio frequency*. Thus, a request for heart rate or ECG signal will be transmitted from the hand-held unit to the data relay units. From the data relay units the request for heart rate or ECG signal will be relayed to the athlete on a *second* radio frequency. For returning the result the process is simply reversed.

This type of sub-system design makes way for dedicated communication to and from all units and athletes around and on the field. By making use of this concept it will now not matter in which direction the athlete faces, or if the remote heart rate monitor is placed on the chest or the back of the athlete, the antennas mounted on the remote heart rate monitor will always be in direct contact (*line-of-sight)* with any two of the data relay units placed on the four corners of the sporting field.

To get a better understanding of the proposed system as an entity refer to the following two depictions. Here the remote heart rate monitors, data relay units and hand-held controlling unit are placed into perspective.

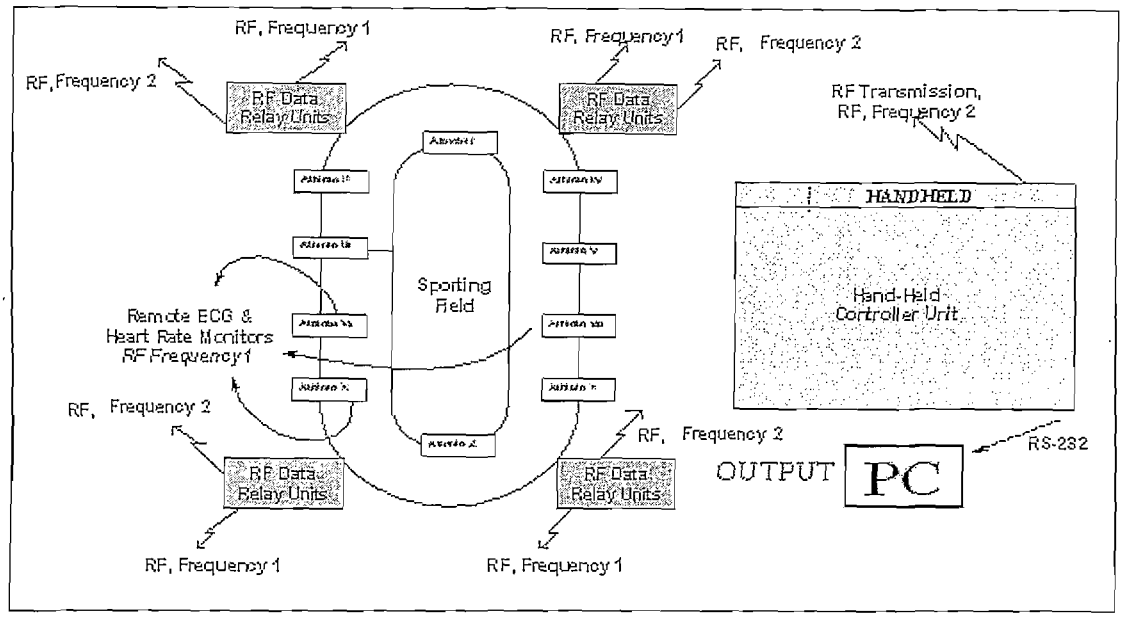


Figure 4: Proposed Overall System Layout

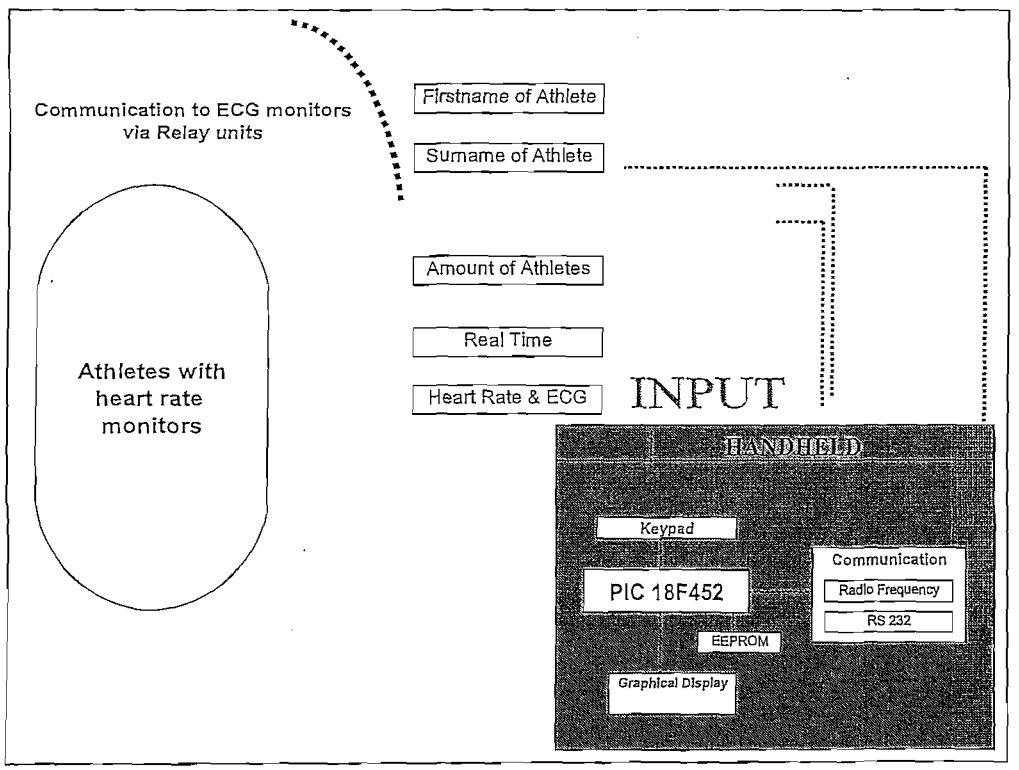


Figure 5: Hand-Held Controlling unit Block Representation

From figures 4 and 5 it is possible to see that the overall system will consist of several real time remote ECG and heart rate monitors on a sporting field. Four data relay units will be placed around the field in order to ensure constant communication to and from the heart rate monitors. These data relay units will communicate to and from the heart rate monitors on one RF frequency as discussed earlier and to and from the hand-held controlling device on a different RF frequency. This will ensure constant communication to and from the heart rate monitors not only because they will always be in line-of-sight with any two of the data relay units around the field but also because a channel for communication will always be open for transmitting data. To explain this concept briefly; it will always be possible for the hand-held controlling unit to communicate to the data relay units and at the same time it will always be possible for the heart rate monitors to communicate to and from the data relay units at the same time. This is purely a result of implementing two different RF frequencies. In short, no cross-talk can occur between the heart rate monitors and the hand-held controlling unit. The data relay units will be responsible for relaying data to and from the heart rate monitors and to and from the hand-held controlling device. The *frequency swap* will happen in the data relay units as depicted in figure 4.

The hand-held unit will be used to set up the entire system before operation.

The user will be able to select *to only see* the heart rate of an athlete, in which case the heart rate will be calculated on the ECG monitor and transmitted to the hand-held unit where it will be displayed. This heart rate data can also be downloaded in real time to the higher level software package running on a PC or laptop next to the sporting field. Here it will be possible to manipulate the data, represent the data graphically and make print-outs of the data. The software will also be able to warn the coach or sport scientists if heart rate becomes too high or too low or if the rate of change is unpredicted.

The user will also be able to set up the system to transmit the entire ECG signal in which case all of the sampled data points on the remote ECG and heart rate

monitor which is on the athlete will be relayed back to the hand-held controller unit via the data relay units next to the field from where it will be downloaded in real time to the higher level software package on a PC or laptop. This software package on the PC will be able to reconstruct the ECG signal from the sampled data points and graphically display the ECG signal. All sampled ECG data points received by the PC will also be stored in a database for later examination.

For the purpose of this project it will be possible to, in real time, continuously track the heart rate of 64000 athletes all at once but only one ECG signal from any two athletes will be displayed and updated regularly at any one time on a PC screen. The limitation of 64000 athletes is purely a result of the usage of 16-bit integers in the software controlling the remote ECG and heart rate monitor. The limitation of one real time ECG signal is a limitation placed on the system by national law, prohibiting the usage of more bandwidth which will allow for the transmission of more ECG signals. Displaying an ECG signal correctly in real time means sampling the heart signal at least once every 10ms and constructing a graphical view of the sampled data. Doing this and transmitting all the data for more than one athlete requires much more bandwidth than is available by law and quite frankly, way more than is made available by ECASA, the telecommunications governing body of South Africa. (Determining the amount of bandwidth necessary for transmitting high volumes of data over an RF channel is a discussion that falls outside the scope of this dissertation and the reader is referred to the following book for more information: Wireless Communication Systems Second Edition, Thomsons, Roy Blake, 1997)

With successful implementation of this newly designed system a sport scientist will have all the information at hand to give advise to the coach and team manager during a sporting event as how to change players, play the team or take action upon crucial health-concerning information made available by the real time extraction of the ECG or heart rate information of a specific athlete.

3.4 Constraints Subjected to the Control and Design of the System

The control of the system will be subjected to various constraints, some of which are listed in the following table:

Parameter	Constraint boundary
Temperature	Reliably operational between 0 and 50 degrees Celsius (based on component values)
Battery Power	12V, 9V, 5V and 3.3V all controlled voltage levels (Duration Factors based on temperature and frequent usage)
Handling	Equipment drops or severe shaking
Contact	Heart rate equipment needs to be checked and serviced regularly and electrodes must be replaced at least once per new athlete.
RF Communication	Selectable and allowable frequencies, transmission power, and reliable protocols. Restrictions on the ranges of RF communication will be placed on both communication between athletes and the relay units and between the relay units and the hand-held controller unit. Reaching distances will be accepted as adequate if communication between athletes and the data relay units can reach 100m and if communication between the relay units and the hand-held controller unit can reach 200m.

Table 1: Constraints of the control system

If necessary the hand-held controlling unit will be able to receive additional inputs from PC's or laptops depending on testing and evaluation. It might be necessary to build in super user software routines only available to the designer of the system in order to validate or evaluate communication, mathematical manipulation or even system redundancy. A simple example might be to implement counters on the remote heart rate monitor, the data relay units next to the field and the hand-held controlling unit to ensure that all data points transmitted from the remote heart rate monitors are relayed correctly by the data relay units and received correctly and in order by the hand-held controlling device. These counters can then be accessed by the designer through some controlled method to validate the transmission of data points.

Another major constraint to the control of the system is reliable communication. Understanding the basic procedures of RF communication is an important part of this project, although it falls outside the scope of this dissertation a very thorough study of this communication technique and its restraints will be done.

Design Documentation

1. OVERVIEW

Overview

Part I of this dissertation gave a brief explanation of the problems encountered when making use of currently, off the shelf available heart rate monitors. The advantages of having a heart rate monitoring system with the added functionality of transmitting the heart rate to a hand-held controller unit in real time, was also discussed.

It was then said that, the purpose of this research is to design a fully functional ECG monitor capable of tracing an ECG, determining the heart rate from the ECG signal, and transmitting the data to a hand held computer unit in real time. A brief elaboration on the design of the broader system surrounding the real time ECG monitor (data relay units, RF communication methods, the hand held computer unit etc.) was also given, as all of these subsystems are a necessary part of the outcome of the research. Although not the main focus of the research, justification of the ECG monitor requires the design and development of such sophisticated subsystems. Without the mentioned subsystems, the end result of the research would not be visible and thus can not be tested and evaluated.

With the latter mentioned, it is safe to say that the main focus of the rest of this dissertation will be on a sophisticated front end design (a filter design). With the front end of an ECG monitor designed to be highly sensitive, accurate and functioning properly, making any calculations from the acquired signal will be much more of a software issue than will it be a design issue.

First, an overview of the practical issues to be considered when designing an ECG monitor will be provided. All of the different subsystems (and components included in each of them) of the heart rate and ECG monitor will be discussed, which will be followed by an investigation of the problem areas surrounding each. Detail

explanations as to different decisions taken in the design process will also be provided.

The document will then go on to discuss considerations in the choice of components and possible programming of the relevant software.

The document will also provide the reader with design templates as well as a suggested solution for the unique problem of tracing an ECG signal, calculating the heart rate from the ECG signal and transmitting the data to a hand held computer unit in real time.

1.1 Control Overview

Control Overview

- Because control during the design phase of a project is one of the most critical phases of a project, controlling a project like this in the wider sense of the context depends on the accuracy during design and development.

If all of the different types of electronic components available today is taken under consideration, it becomes all the more difficult to choose the correct components for different applications.

In an application like heart rate monitoring and ECG monitoring equipment, some of the most difficult decisions will have to be made when deciding on components for the application. Noise levels, package sizes, packaging and battery power will be some of the most critical issues, to mention but a few.

Controlling the output (which includes the financial management of the project) will be difficult due to the fact that specialised designs, precision equipment and imported components may become very expensive.

1.2 Technical Electronic Background & Overview

Technical Background

Before venturing off into part II, the technical design of an ECG monitor, a few basic electronic concepts need to be understood. As a highly sensitive heart rate and ECG monitor will be designed, an urgent need to investigate and understand a few fundamental electronic concepts exists. Comparators, operational and precision instrumentation amplifiers will be the main analogue components used in the process, knowing exactly what the differences between and uses for each of them are, is extremely important in order to prevent an underperforming electronic design.

1.3 Important Electronic Fundamentals

Important Electronic Fundamentals

Retrieving in real time, a heart rate and ECG signal from an athlete will require certain advanced electronic designs in the analogue and digital domains. Transmitting the data from the athlete also requires careful design of a communications protocol. For these reasons and possible others some electronic fundamentals which will later be necessary for a good system design will first be explored. As progress is made through the design part of the heart rate and ECG monitoring system in part II of this dissertation, references back to, and elaboration on some of these fundamental issues will be given.

1.3.1 Analogue Domain

The Analogue Domain

a) Comparators and Operational Amplifiers

The approach that will be followed is a simple question and answer method:

Q: What is a comparator and how does it differ from operational amplifiers?

A: A comparator has but one basic function; to determine if an input voltage is higher or lower than a reference voltage.[8] The outcome of the test is presented as one of two answers, yes or no, and is expressed as one of two voltage levels, established by the limiting values of the output. A few different applications are found for comparators in the practical world:

1. *Switch driving,*
2. *Polarity identification,*
3. *Pulse generation and*
4. *Square or triangular wave generation.*

"The devil is in the details", because in principle any high gain operational amplifier can be used to make this decision. But, there are some basic differences between the design of op amps and comparators. The one with the most impact on this project is the fact that all comparators are designed to have output levels, compatible with digital voltage-level specifications. Also, for use with digital circuitry, many comparators have latched outputs.[6] Refer to design techniques with comparators and op amp for an explanation of latch outputs and digital voltage specifications.

Q: So, how *do* comparators and op amps differ?

A: Overall, the op amp is designed to provide accuracy and stability, both on dc levels as well as dynamic, for a specified linear range of output values in

precision feedback (closed-loop) circuits.[6] When an open-loop op amp is used as a comparator and its outputs swinging between their limits, the internal capacitors used for dynamic stability causes the output to be slow. The op amp is lazy to come out of saturation and slew through its output range.

On the other hand, comparators are generally designed to operate open loop. Thus, output levels slew between specified upper and lower limits. This is in response to the sign of the net difference between the two voltage inputs. They are quite fast since they do not require the op amp's compensating capacitors.

Imagine the input voltage to a comparator to be more positive than the reference (0V) or the reference plus the offset voltage (V_{os}) plus the required overdrive *(due to limited gain). A voltage corresponding to logic "1" will appear at the output. The output will be "0" when the input is less than V_{os} and the required overdrive. So, a comparator can be thought of as a one bit ADC.*

Comparators and op amps are also specified in different ways. One example is the offset voltage. On an op amp the offset voltage is the voltage applied to the input to drive the output to a specified voltage corresponding to an ideal zero input. On a comparator this definition is modified to centre in the specified voltage range between 0 and 1 on the output. A typical low or "0" output from a TTL comparator is less than 0.5V. For a low voltage op amp, the low *output is close to its negative rail. Thus in a single supply application the* low *output of the op amp will be almost 0V.*

Figure 3 depicts the typical low voltage differences between an op amp and a comparator. A 1mV differential input voltage is applied to both.

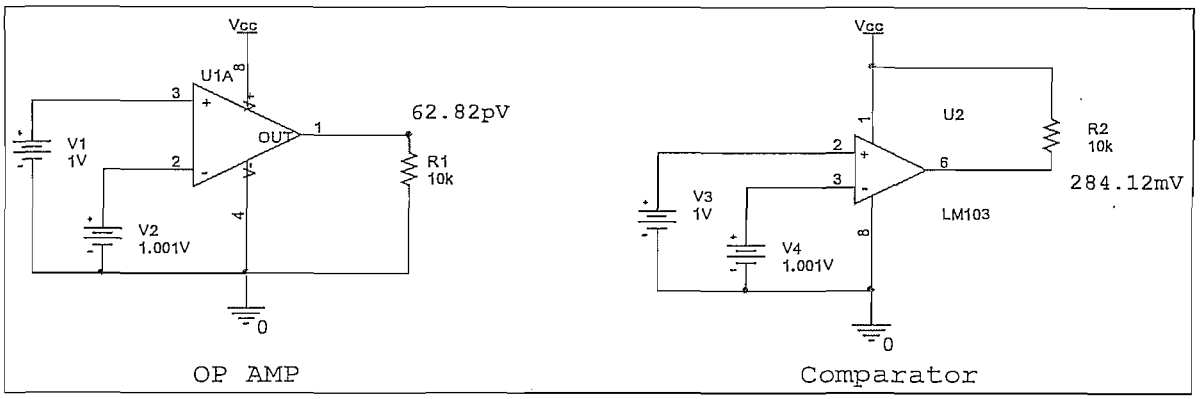


Figure 6: Responses of a Single supply op amp compared to a comparator for a 1mV differential input.

*All simulations done in ORCAD ver. 9.0, PSPiCE.

Built to compare two levels as quickly as possible, comparators do not have the internal "Miller" capacitors [18] used for compensation as do op amps. Also, their output circuits are capable of more flexible excitation than that of op amps.

The absence of compensation makes way for very wide bandwidth in comparators. While op amps usually use a push-pull technique (almost the same as for Class B amplifiers) for symmetrical swings between supply voltages at their outputs, comparators usually have open collectors with grounded emitters. For this reason the output of a comparator can be returned through a low value collector load resistor to a voltage different from the main positive supply.

Q: OK, now it is clear that there are fundamental differences between op amps and comparators. How *does* the designer choose to replace a comparator with an op amp?

A: Pay attention to the following six major factors:

1. *Transition time.[18]*
2. *Consider saturation recovery.[18]*
3. *Watch out for input protection diodes.*
4. *Consider the way they interface with different logic families. [16]*

5. *Watch out for input voltage range specifications and phase reversal tendencies*
6. *Consider V_{os} (output voltage) and I_B (base current) non-linearity vs. input common mode voltage of the different components.*

As the design progresses, some of these factors will be discussed in more detail.

The bottom line is....

An op amp may be used as a comparator with excellent added precision at low frequencies. In fact, for comparing signals in the milli- and micro-volt ranges, op amps are the only practical choice. It can also be an economical advantage as free amplifier channels can be implemented in further designs. It is possible to save time and money and produce a more accurate design if a little time is spent on really understanding the fundamental differences between comparators and op amps. Major trade offs include recovery time, speed and power consumption. [18]

b) Operational Amplifiers and Instrumentation Amplifiers

Again, the exploration of the differences and similarities will be done with a question and answer method.

It might be considered tradition to start a discussion on instrumentation amplifiers (I.A) and operational amplifiers by saying that an I.A is not an op amp.[6] To the informed user this might seem obvious, and as awkward as a description by exclusion may be, such an approach is inevitable and perhaps necessary to give insight into the delicacy of a real time remote heart rate and ECG monitor's design. The ultimate flexibility provided by currently available op amp IC's, is the first thought that springs to mind when an engineer needs a signal conditioning gain block.

The purpose of this background discussion is to inform the reader when and where an instrumentation amplifier may best be employed, as well as to explain where its unique specifications give it an advantage, over the more flexible op amp.

Q: What is an instrumentation amplifier?

A: In an environment hostile to precision measurement, an instrumentation amplifier is a precision differential voltage gain device.[14] The device is usually optimized for operation under these conditions. Real transducers rarely exhibit zero output impedance and even zero-to-ten volt ranges. Induced, leakage or coupled electrical interference (noise) is always present to some extend. In brief, even the best "cookbook" must be taken with a grain of salt.

Knowing this, I.A's are intended to be used whenever acquisition of a useful signal is difficult. Because source impedances may be high and/or unbalanced, I.A's must have extremely high input impedances.[6]

One of the most important aspects of an I.A is balanced differential inputs, so that the signal source may be referenced to any reasonable level independent of the I.A output load reference.

Probably the most important aspect of an I.A is common mode rejection (measure of input balance), which is very high so that noise pickup and ground drops are minimized.[18] Further more all critical components to an I.A are usually internal to the package where in the I.A is found.

Of course all is not easy. The precision of an I.A is provided at the expense of flexibility. An I.A is not intended for integration, differentiation, rectification or any other non voltage gain functions. Although possible, these tasks are best done by the more flexible op amps.

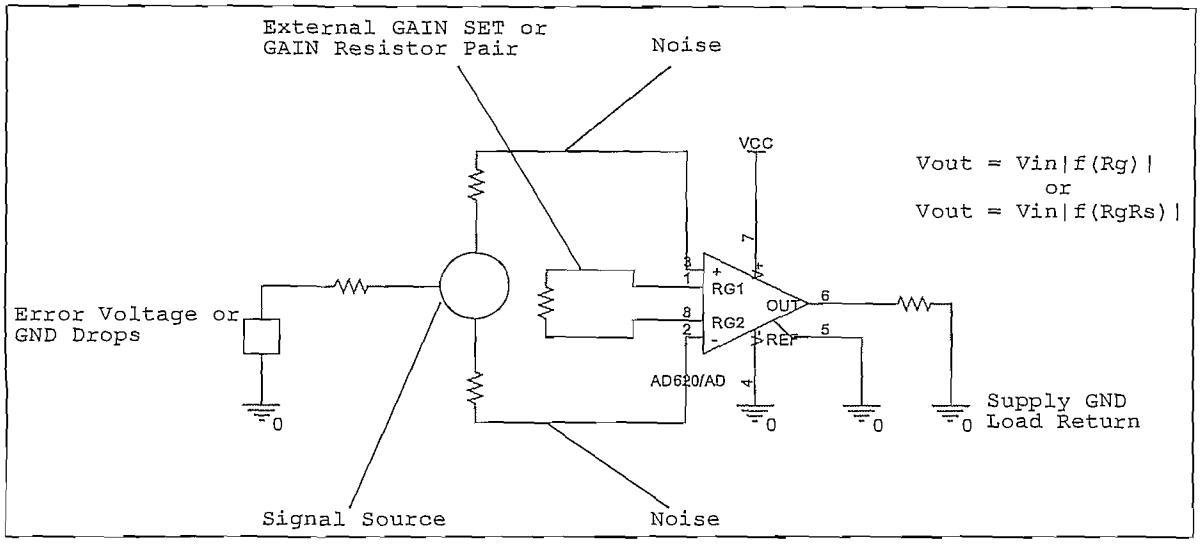


Figure 7: A Functional Diagram of a basic I.A

Direct interfacing to floating signal sources is permitted. Being truly differential, the I.A detects only the difference in voltage between the two inputs.[14] Further more any common mode signals (these must be present on both inputs), such as noise and voltage drops in ground lines are subtracted and cancelled at the inputs before amplification.

The output of an I.A is single ended. Knowing this the user will be able to drive ground referenced loads as normally found in measurement equipment. Load references are usually common to the power supply return path.[18] More attention will be given to the overall grounding aspect in the design documentation.

1.3.2 Communication

Communication

A variety of communication methods and protocols exist. Deciding on which to use is a difficult task. Implementing them is even more difficult due to the simple nature and complexity of high speed communication protocols. A good understanding of each and the differences is necessary to implement the correct and most useful design for the application.

Seeing that the objective of the project is to retrieve heart rate and an ECG signal from an athlete in real time while the athlete is training or competing, it is necessary to have constant communication to and from the monitor on the body of the athlete. Further more, because the athlete is running or practising some other kind of sport, it is not possible to have any wires attached to the athlete leading to some kind of controller placed next to the field.

For this reason and many more, RF communication is the leading choice. Knowing this, a solid understanding of this communication method, the ways of implementation and electronic background of it is necessary. As said previously because of the difficult nature of RF itself this dissertation will not discuss the RF design in depth. Only pointers for implementation and practical issues will be discussed. Further more, because of the sensitive nature of interfacing analogue, digital, RF and other high frequency electronic components such as voltage inverters all onto one design it is thought appropriate to give a short background on basic RF design as well. This background knowledge, however little, will play a crucial role in the later design of the ECG monitor. *Refer to appendix B for this background.*

Q: What are important issues to keep in mind when designing with RF?

A: *Have a good understanding of the following:*

1. Bandwidth of the receiver
2. Transmission rate of data from the transmitter
2. Transmission power. Usually about 10mW maximum in the ISM band
3. Frequencies available for use without licences.

B: *Keep the following in mind when implementing RF:*

1. Range of transmission with a set power output.
2. Ground planes for the antenna. [18]
3. Coding of data before transmission for transmission stability. (For example Manchester coding.)
4. Which antennas to use for different applications. [18]
5. Do the communicating units have line of sight or are there obstacles in their path of communication.

Now that the *most basic* electronic background necessary to understand, before constructing an ECG monitor have been discussed, it is time to take a closer look at the practical issues surrounding the design of an ECG monitor.

2. PRACTICAL ISSUES WHEN WORKING WITH ECG SIGNALS

Practical ECG Issues

- ECG signals may be corrupted by various kinds of noise. The main source of noise is: power-line interference, 50-60Hz pickup and harmonics. [17]
- Electrode contact noise: variable contact between the electrode and the skin, causing baseline drift. [17]
- Motion artefacts: shifts in the baseline caused by changes in the electrode-skin impedance.
- Muscle contraction: electro-myogram-type signals (EMG) are generated and mixed with the ECG signals.

- Respiration, causing drift in the baseline.

- Electromagnetic interference from other electronic devices, with the electrode wires serving as antennas, and

- Noise coupled from other electronic devices, usually at high frequencies.

Different ECG monitors are constructed to operate under different circumstances. All of the above mentioned sources of noise have been taken from a variety of different designers' ideas and brought together, for a single solution and the implementation thereof.

For meaningful and accurate ECG detection, steps have to be taken to filter out or discard all these noise sources.

As this research extends the margins of the normal ECG monitoring system in, that it is to be used outside on the sports field in real time, the equipment must be made small, so as not to add a considerable amount of weight to an athlete. Equipment should also be made durable as it will be used outdoors.

At this stage it is clear that many decisions need to be made between many different components, all suitable for the product, many different design approaches and many different implementation methods of these solutions.

It should also be clear by now that an ECG signal is an analogue signal. Thus, the design of an ECG monitor will include an analogue front-end, in order to pick up the ECG signal from the human body. Next, certain filters will have to be implemented to rid the signal from common mode and other noise. These filtering techniques might be analogue or digital, and lastly the digitization of the signal will be discussed. At the end of the design of the ECG monitor, a short discussion surrounding the subsystems (hand-held computing unit and data relay units) will be given in order explain and evaluate the system as a whole.

The development and final design of the heart rate and ECG monitor will be discussed in the following manner:

1. First, an in depth discussion on different I.A's will be given and, a few different methods of implementing them will be explored.
2. Next the analogue filtering techniques following the front-end of the ECG monitor will be discussed.
3. Finally the digitization and digital filtering techniques will be discussed.

In short, the heart rate and ECG monitor can be depicted, very much by an over-simplified block diagram as seen in figure 8. The discussion of the design will follow the order as depicted from left to right as depicted.

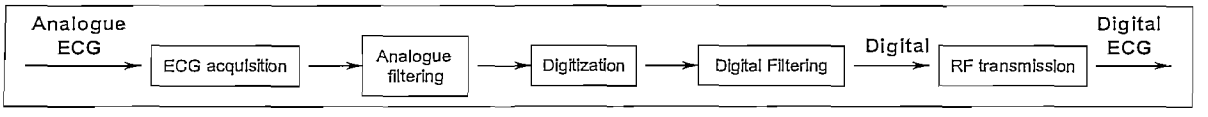


Figure 8: Simplified Block Diagram of the ECG Monitor

2.1 Analogue Topology

Analogue Topology

Figure 9 shows a block diagram of a typical single-channel electro cardio graph. In the chain, it is apparent that all filtering is done in the analogue domain, while the microprocessor is used principally for communication and other downstream purposes.

Thus the powerful computational properties of the digital core are not readily available to deal with the signal in its essentially, raw state.[13] In addition, sophisticated analogue filters can be costly to the overall design due to their inflexibility and the space, cost and power they require.

In another sense it has become all the more difficult choosing the correct analogue device for a certain application. This is due to the fact that so many different I.A's and op amps exist, that the application for each, has become obscured.

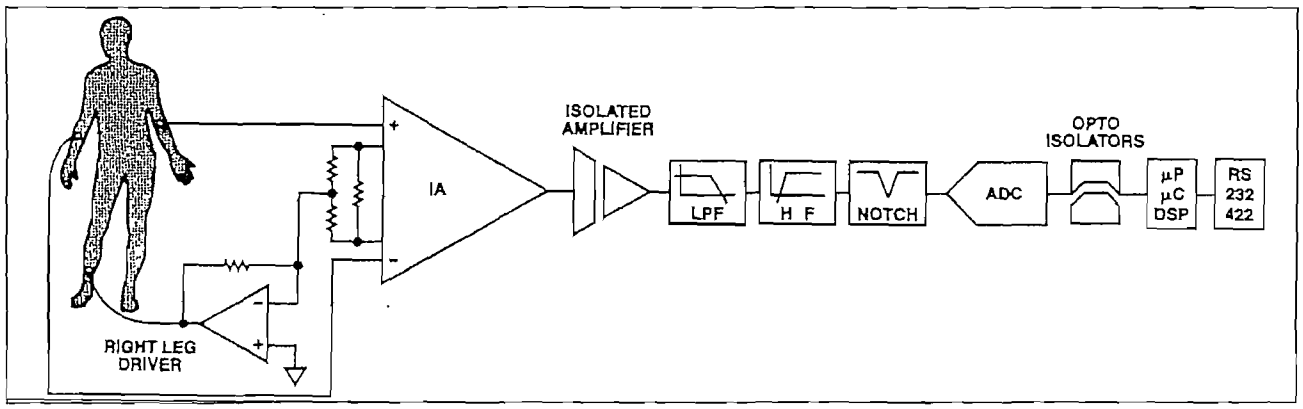


Figure 9: Typical single channel Electrocardiograph procedure

Figure 10 with acknowledgement to Enrique Company-Bosch and Eckart Hartmann, Analog Devices.

It is by no means possible to design an ECG monitor without any front end, or filtering components in the analogue domain.[6][12][18] Designing any analogue acquisition system without a front end means not designing the system at all. A front end in the analogue domain is necessary to capture the signal of interest. It is merely stated that, making use of the powerful computational capabilities of microprocessors will aid in the design of a sophisticated and sensitive enough ECG monitor, to be used during sporting events and transmitting the data in real time. Having a mixture of analogue, digital and RF components integrated into one application, especially one as sensitive as this drags along its own issues but, they will be dealt with as the design progresses.

The front end of an ECG must be able to deal with extremely weak signals, ranging from 0.1mV to 5.0mV peak-to-peak, combined with a DC component of up to ±300mV – the latter resulting from the electrode-skin contact.[13][14][17][18] In short, the so called electrode skin contact acts as a typical voltage divider, where the electrode and the skin can be seen as two resistors respectively, each with a different resistive value. Added to this still is the common mode component of up to 1.5V resulting from the potential between the electrodes and ground. [6][8][13][14][17][18]

Again, it is extremely important to consider, and re-consider the analogue design from every possible design-view as a faulty or inferior analogue design will result in a faulty output signal. Because the analogue processing is the first step towards obtaining an ECG signal and heart rate, inferiority at this point of the design will result in more complex filtering designs, more complex anti-aliasing filtering techniques before digitization and possibly even, irreparable damage to the acquired analogue signal.

If a system like this one is to be accurate, and moreover specifically focused on the human heart rate, the next analogue issue would be bandwidth.

The bandwidth of common ECG equipment available for medical use, varies from 0.5Hz through 1kHz, depending on the application.

For monitoring equipment used in intensive care units, up to 1kHz bandwidth is used. This is to be able to rid the ECG signal of possible pacemaker voltage potentials and to distinguish between the pulses generated by a pacemaker and the electric signal originating from the heart itself. [17]

In order to make this product useful on the athletics track and in the sporting environment over all, the bandwidth needs to be reduced to within a range of 0.5Hz to 120Hz. This is sufficient to detect the heart rate of a racing athlete, and at the same time, filter out the noise spikes resulting from muscle contraction and feet bumping on the ground whilst running. Respiration noise spikes are also limited.[6][17][18]

3. ANALOGUE INPUT PROCESSING

Analogue Processing

The idea for constructing the heart rate and ECG monitor, is to construct the analogue front-end, making use of a typical instrumentation amplifier (I.A) and the right leg common mode feedback approach. *Refer to appendix F and section 3 of Part*

III of this dissertation for an explanation of the right leg common mode feedback approach used in most common ECG monitors.

This common approach, however, needs somewhat of a change to implement the idea of a real time heart rate monitoring system. Rules regarding jewellery and any other objects on the athletes' body need to be taken into account. Thus, the right leg common-mode feedback approach will have to be changed somewhat. In any event, it should be obvious that, having a wire running down the leg of an athlete will not be feasible. Furthermore, taking into account that an athlete has to carry around the ECG monitor with him/her whilst competing or training, weight becomes another factor.

Having mentioned this, we immediately need to take a look at the basic operation of an I.A, and the circuitry needed to make it operate at its optimum functionality. Most I.A's needs to be supplied by a positive and negative voltage supply. To supply a positive and a negative voltage, normally, at least two batteries are needed. It is possible to generate a positive and negative voltage by making use of a single battery but, this design calls for the use of two Zener-diodes. Implementing Zener-diodes in a circuit intrinsically means adding a noise factor to the circuit, and the bandwidth of this noise factor stretches over and beyond the bandwidth of interest for obtaining the ECG signal. Also, implementing this design to generate a positive and negative voltage supply means adding two resistors in the voltage network to protect the Zener-diodes from damage as a result of too much current flowing through them. This places a current consumption margin on the circuit as a whole. For a reference as to how this type of circuit produces a positive and negative voltage from a single battery, refer to any basic electronic design theory. Further more, practical considerations such as space, weight and the possibility of an athlete getting hurt during a sporting event because of the extra equipment (a second battery) does not justify this solution, albeit theoretically correct. Thus, another design change is necessary.

Before continuing to explore further possible problem areas in the analogue domain let us take a look at possible different I.A configurations and then discuss a

proposed precision instrumentation amplifier circuit and the setup of the circuit, which will be implemented as the front-end of the ECG monitor.

3.1 I.A Configuration and Designs

I.A Configurations

While there are many ways of designing an I.A, most designs can be classified into one of two categories.

A set of interconnected op amps and a precision resistor network is probably the most commonly found configuration. The reason for implementing such a configuration is minimizing component count and is commonly found in hybrid I.A's. [6][13]

The other category uses fundamental active circuit elements such as differential circuits and controlled current sources rather than op amps. Unnecessary features are eliminated and active device count tends to be minimized. Probably the most important feature of these kinds of designs are the fact that dependence upon accurate resistor matching is decreased.[13]

As readily available I.A IC's tend to differ from package to package the latter technique tends to be the most useful. Also because non-linearity tends to be lower at higher gains this technique is used in modern I.A packages although some sacrifice of linearity may exist at lower gains.[13]

3.1.1 Op Amp based I.A's

Op Amp I.A's

Three different types of I.A design will de discussed along with their advantages as well as disadvantages. Implementation strategies and operation will

also be explored. Each type of I.A will, theoretically be explored and the operation of each will be discussed. At the end, in section 3.1.2, a discussion on the choice, best fit for *this* ECG application will be given.

a) A Single Op Amp Solution

Single op amp I.A Design

All things considered , figure 10 demonstrates the most simple method of *implementing a differential gain block with an op amp.*

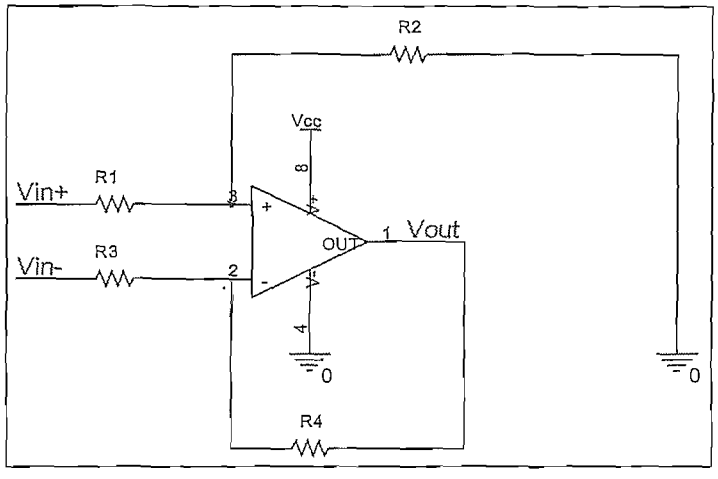


Figure 10: Differential Input Gain Block (Simple Subtractor)

Output for V_{IN}^+ (V_{IN}^- grounded) is:

$$V_{O1} = V_{IN}^+(R_2 / (R_1+R_2)*((R_3+R_4)/R_3) \quad (1.1)$$

Output for V_{IN}^- (V_{IN}^+ grounded) is:

$$V_{O2} = -V_{IN}^-(R_4/R_3) \quad (1.2)$$

By Superposition:

$$V_O = V_{O1} + V_{O2}$$

$$= V_{IN}^+(R_2/(R_1+R_2))((R_3+R_4)/R_3) - V_{IN}^-(R_4/R_3) \quad (1.3)$$

if $R_2 = R_4$ & $R_1 = R_3$

$$VO = (V_{IN}^+ - V_{IN}^-)(R_4/R_3) \quad (1.5)$$

By doing this a simple differential voltage amplifier has been created, meaning that the difference between two input signals can be obtained at the output of the op amp. But the input impedances are low and unequal, as the two input resistors, R36 and R37 may or may not have the same value, depending on the gain required. To make things worse, all the resistors have to be ratio-matched to maintain a good common mode rejection.

$$V_{OUT\,CM} = V_{OUT} \text{ for } V_{IN}^+ = V_{IN}^-$$

$$= V_{IN}[(R_2/(R_1+R_2)((R_3+R_4)/R_3) - (R_4/R_3)] \quad (1.6)$$

To explain equation 1.6 and demonstrate the impracticality of this type of design let us take a look at a scenario where we need to obtain an output signal from

this type of I.A with a gain of 1. Thus all resistors are equal. For a 0.1% mismatch in just one of the resistors we obtain the following:

$$R_1 = R_3 = R_4 = R$$

$$R_2 = 0.999R$$

$$V_{O\,CM} = V_{IN}\,[(0.999R/1.999R)(2R/R) - (R/R)]$$

$$= 0.0005V_{IN}$$

$$CMR = -20\log(0.0005) \qquad (1.7)$$

$$= 66.02dB$$

In the case of this study and for the objective of designing an ECG monitor, source resistances are not low and definitely not balanced. To elaborate on this issue as it might seem unclear, it is not a given that the impedance of the human skin with respect to another point (which stays the same) will be exactly the same from every single point on the body. Furthermore, even though the values from human to human tend to differ, measuring the resistance of the human skin or body results in very large values. Gain and CMR will be degraded even further if these issues are taken into account and a single op amp based I.A is implemented.

Further more, considering that reasonably priced and readily available resistors are not perfected during manufacturing one can hardly expect to improve on this type of performance when using a design like this. For an application where a precise outcome is expected this type of design is inferior by means of intrinsic factors.

b) A Dual Op Amp Solution

Dual op amp I.A Design

Some of the weaknesses of the single op amp design are eliminated by the more elaborated, two op amp design as shown in figure 11.

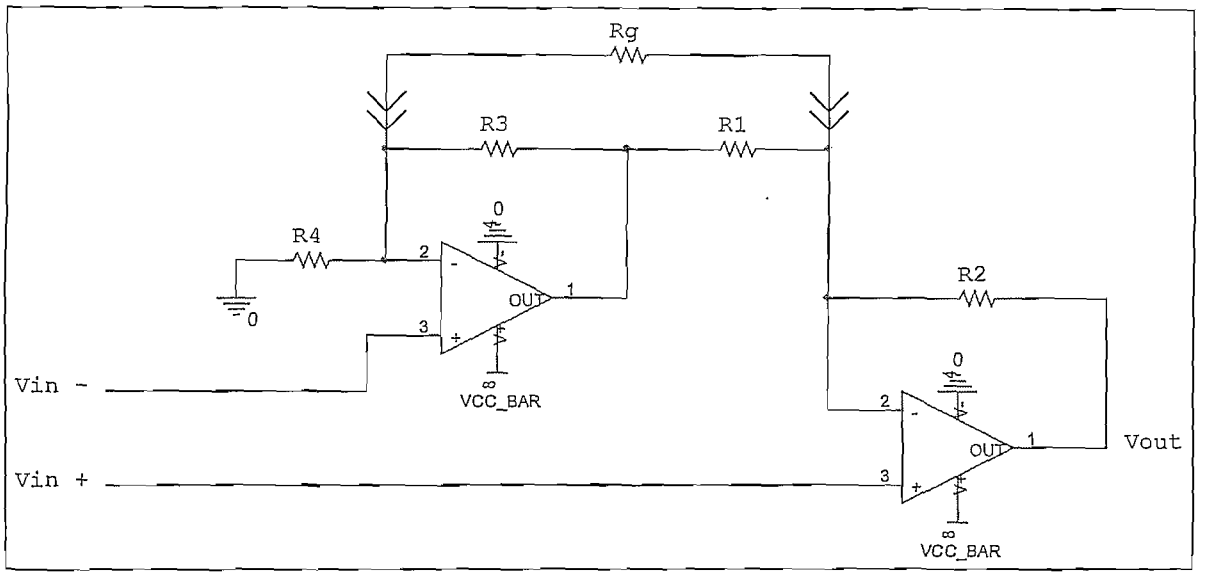


Figure 11: Instrumentation Amplifier designed with two op amps

Figure 11 with acknowledgement to Enrique Company-Bosch and Eckart Hartmann, Analog Devices.

The first noticeable design change is that input impedances are high. Thus permitting the output impedances of the source, to be non-zero and even unbalanced.

The gain of this type of design is set by changing only one resistor, R_g. By doing this the CMR is allowed to remain constant once initial trimming is accomplished. Albeit, CMR is still dependant on resistor matching.[7][8][14]

When studying the circuit design very carefully, it is worth mentioning that a disadvantage of a design like this one can be that the common mode, voltage-input-range is a function of gain and may be poor.

The left hand side amplifier is called upon to amplify a common mode signal by the ratio $\frac{R_3+R_4}{R_4}$ and this could lead to the saturation of this amplifier and by doing so leaving no room for amplifying the differential signal of interest. Saturation of this amplifier may be a result of amplifying an already "*large amplitude*" signal to the extent that the op amp simply saturates or amplifying frequency content (as part of the common mode that enters the system) outside the bandwidth capability of the specific op amp to the extent that the component simply becomes unstable.[1][2][6][13]

Again for a precise instrumentation amplification application specifically where the differential signals of interest vary between 0.1mV through 5mV and common mode might extend this amplitude by mentionable factors, this type of design, intrinsically proves not to be adequate.

c) A Classical Three Op Amp I.A Design

Classical I.A Design

By far the most common configuration of most I.A's is a three op amp solution as is depicted in figure 12.

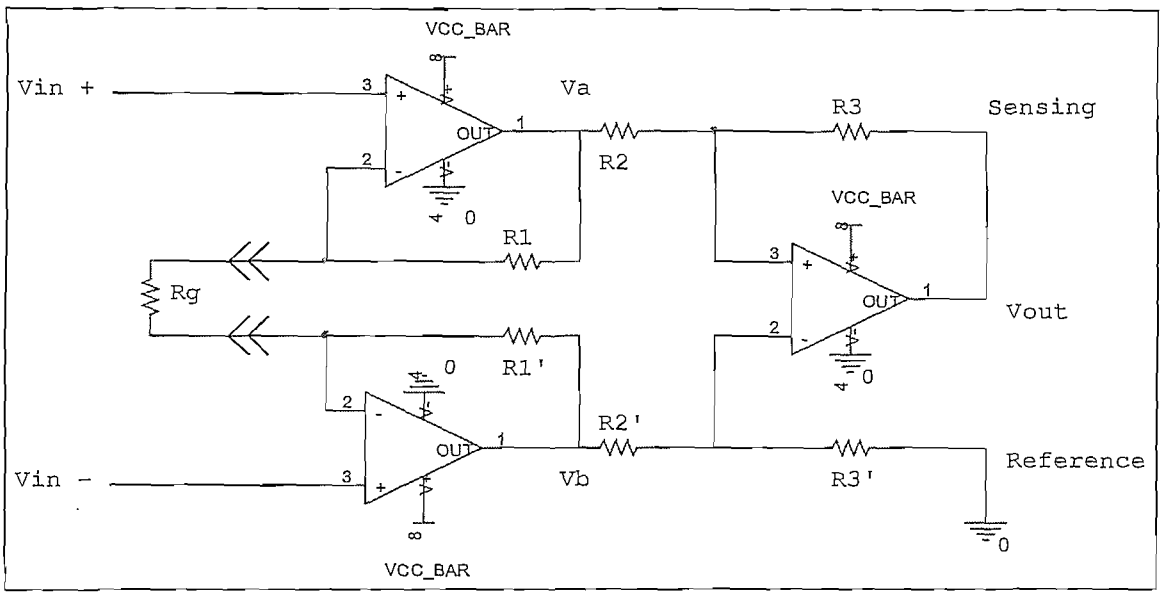


Figure 12: A typical 3 op amp Instrumentation Amplifier

Figure 12 is a commonly used three op-amp design found in any basic electronic course textbook teaching the principles surrounding operational amplifier design.

A transfer function for this type of design, as for the single op amp design can easily be written down by making use of the superposition theorem:

FOR V_{IN}^{+} = 0

$$V_a = V_{IN}^{-}\left[\frac{(R_1 + R_G)}{R_G}\right] \qquad (1.8)$$

$$V_b = V_{IN}^{-}\left[\frac{R_1}{R_G}\right] \qquad (1.9)$$

FOR V_{IN}^{-} = 0

$$V_a = V_{IN}^{+}\left[\frac{R_1}{R_G}\right]$$

$$V_b = V_{IN}^{+}\left[\frac{(R_1' + R_G)}{R_G}\right]$$

THUS:

$$V_a = V_{IN}^{-}\left[\frac{(R_1 + R_G)}{R_G}\right] - V_{IN}^{+}\left[\frac{R_1}{R_G}\right]$$

&

$$V_b = V_{IN}^{+}\left[\frac{R_1' + R_G}{R_G}\right] - V_{IN}^{-}\left[\frac{R_1'}{R_G}\right]$$

LEAVING:

$$V_{OUT} = -V_a\left[\frac{R_3}{R_2}\right] + V_b\left[\left(\frac{R_3'}{R_2' + R_3'}\right)\left(\frac{R_3 + R_2}{R_2}\right)\right] \qquad (1.10)$$

if $R_3 = R_3'$ & $R_2 = R_2'$ & $R_1 = R_1'$

$$V_{OUT} = (V_b - V_a)\left[\frac{R_3}{R_2}\right] \qquad (1.11)$$

SUBSTITUTING for V_a and V_b

$$V_{OUT} = (V_{IN}^{+} - V_{IN}^{-})\left[\left(\frac{2R_1}{R_G}+1\right)\left(\frac{R_3}{R_2}\right)\right] \qquad (1.12)$$

Using this configuration we can clearly see that gain and CMR still depends on the ratio matching of R_2, R_2', R_3 and R_3', as was the result in both the single op amp as well as the dual op amp designs.

With a little mathematical manipulation, however, it can be shown that CMR does not depend on R_1 or R_1' for the three op amp design at all. With the understanding that a more complex resistive network is present in this three op amp design, bear with the design explanation for just a while so as to understand the reason for the latter statement to be *so* important.

$$V_{CMout} = (V_a - V_b)$$

$$= V_{IN}^{+}\left[\frac{R_1' + R_G}{R_G}\right] - V_{IN}^{-}\left[\frac{R_1'}{R_G}\right] - V_{IN}^{-}\left[\frac{R_1 + R_G}{R_G}\right] + V_{IN}^{+}\left[\frac{R_1}{R_G}\right]$$

BUT

$$V_{CMin} = V_{IN}^{+} = V_{IN}^{-}$$

SO THAT

$$V_{CMout} = V_{CMin}\left[\left(\frac{R_1' + R_G}{R_G}\right) - \left(\frac{R_1'}{R_G}\right) - \left(\frac{R_1 + R_G}{R_G}\right) + \left(\frac{R_1}{R_G}\right)\right]$$

$$= V_{CMin}\left[\left(\frac{R_1'}{R_G}\right) - \left(\frac{R_1'}{R_G}\right) + 1 - \left(\frac{R_1}{R_G}\right) + \left(\frac{R_1}{R_G}\right) - 1\right]$$

$$= V_{CMin}[0]$$

$$= 0$$

A useful conclusion from this mathematical manipulation, in theory at least, is that any amount of gain as determined by R_g, can be taken at the front-end of the I.A design, without compromising common mode signal error. Common mode rejection ratio, CMRR, will increase in direct proportion to gain, which might prove a very useful property.[4][5][1]

Common mode signals in the three op amp design are amplified by a factor 1, regardless of gain. This is because no common mode voltage will appear across R_g, so no common mode current will flow through it. (Remember that the input terminals of an op amp operating normally will have no significant potential difference between them.[4])

The latter proves to be a big advantage because large common mode signals can be handled independent of gain. Also because of the symmetry of this type of configuration, first order common mode error sources at the input amplifiers, if they track, tend to be cancelled out by subtraction in the output stage. [1][6][13]

3.1.2 A Dedicated I.A Design

Dedicated I.A Design

esistor matching still tends to be a problem if one looks at the readily available products on the market. Another trade-off to consider is the one between performance with ease of manufacturing and lower cost with the difficulty of finding the right components.

These reasons and the sensitivity and accuracy needed to trace an ECG signal justify understanding and choosing an I.A based upon minimum active components and creating a dedicated design for the application.

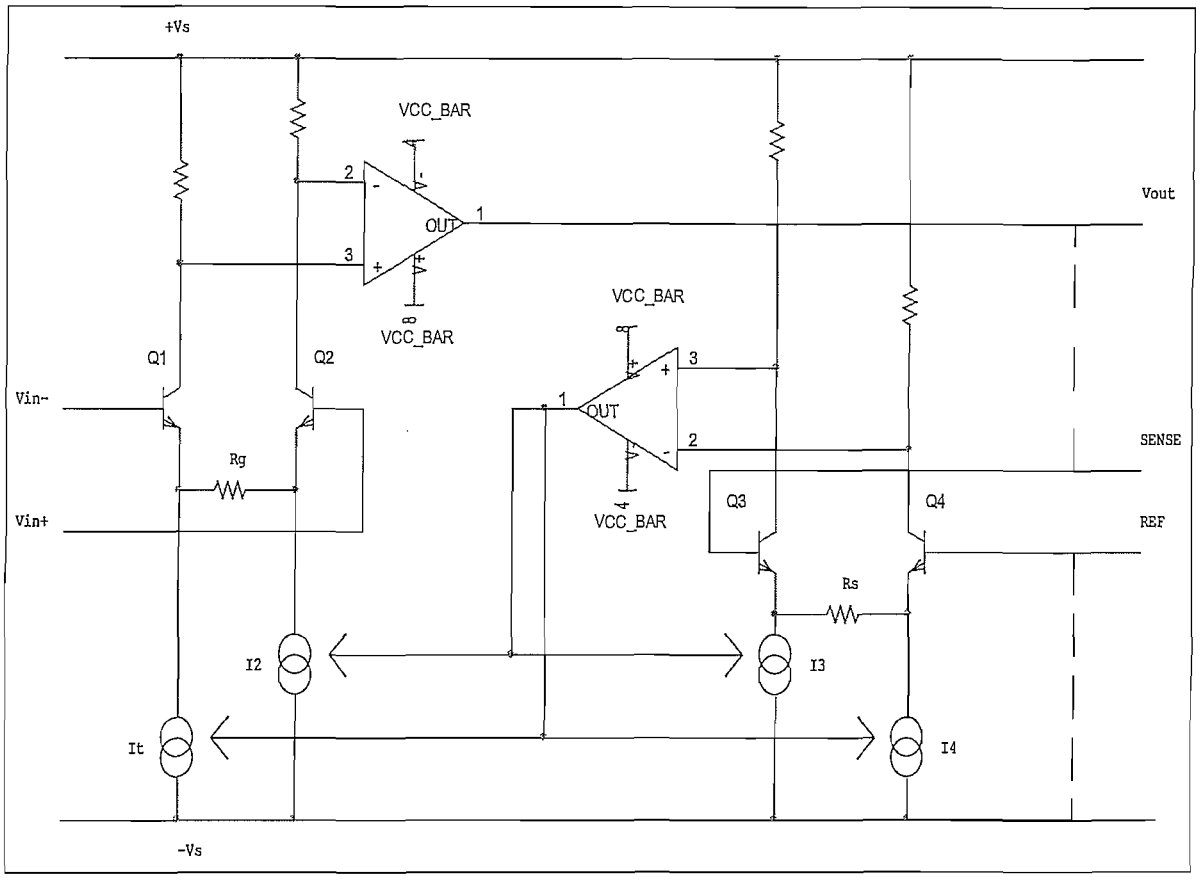


Figure 13: A Dedicated I.A Design

Figure 13 with acknowledgement to Texas Instruments.

Forward gain, in this design, is provided by two transistors, Q_1 & Q_2 as well as the main signal amplifier which is referred to as the input differential stage. (The op amp visible in the top left hand corner of figure 13.) The gain associated with the transistors is $\left[\frac{1}{Rg}\right]$. The main task of the signal amplifier is to sense the difference in input stage collector currents present in Q_1 & Q_2.

With the output connected back to the sensing input differential stage, Q_3 & Q_4 acts as a feedback error sensing amplifier. Trans-conductance is $\left[\frac{1}{R_s}\right]$. The second op amp then senses the collector current imbalance in that stage. [13][14]

With a differential input applied at $V_{IN}^{+} and V_{IN}^{-}$ the collector currents in Q_1 & Q_2 will become unbalanced by a ratio of $\left[\frac{V_{IN}^{+} - V_{IN}^{-}}{R_G}\right]$. This imbalance is sensed by the first op amp. An error voltage is developed between the sensing and reference points.

This in turn tries to unbalance the collector currents in Q_3 & Q_4. The ratio by which the unbalance is measured is $\left[\frac{V_{SENSE} - V_{REF}}{R_S}\right]$.

Sensed by the second op amp, this unbalance is accounted for by adjusting I_3 & I_4 to equalize the collector currents in Q_3 & Q_4. In Theory $I_4 - I_3 = \left(\frac{V_S - V_R}{R_S}\right)$. Also $I_1 and I_2$ is adjusted so that $I_1 - I_2 = I_4 - I_3$.[14]

Thus balance is reached when:

$$\left[\frac{V_S - V_R}{V_1 - V_2}\right] = \frac{V_{OUT}}{V_{IN}} = Gain \qquad \textbf{(1.13)}[13][14]$$

and

$$I_4 - I_3 = I_1 - I_2$$

SO THAT

$$Gain = \left[\frac{R_{SCALE}}{R_{GAIN}}\right] \qquad \textbf{(1.14)}\ [13][14]$$

It should , from this analysis, be apparent enough that the previous requirement of carefully matching resistors has changed to a requirement of carefully matched active devices.

With currently available IC technology this is possible by utilizing the art of precision photographic techniques. Careful layout and well controlled processing is a must as well.[14]

The result, from practical and empirical experimentation by a great deal of professionals, is said to be a good trade off between high precision and low cost.[13]

However, for the application of tracing a true ECG signal and designing a very sensitive front end that will deliver an accurate output to the next stages of the ECG monitor one further design adjustment needs to be made before implementation in *this* circuit.

4. A Quick Review

Design Review before Continuing

efore continuing with the discussion of the proposed front end for this specific application, it seems like a good idea to review what have been done so far.

It is clear by now from Part I that the goal of this research is the understanding and design of an ECG monitor and more specific *a front end and filter that will best suite a real time application in the sports world.*

Up to now discussions have been provided, elaborating on the differences between a variety of analogue components possibly needed in, and suitable for an ECG tracing application. Technical differences between comparators, op amps and instrumentation amplifiers have been discussed.

Further more, thus far in Part II the differences in design and layout of different I.A topologies have also been discussed and compared. A conclusion was reached that the use of a dedicated design will best suite the needs of this application.

Reasons for this decision were given in the previous section (section 3.1.2) based on comparison with other design topologies.

In the next few sections an in detail elaboration on the specific instrumentation amplifier design layouts, best suited for this application will be given. Discussions on other analogue components, needed to be constructed around the I.A to make it function correctly as part of an ECG application, will also be given.

Remember that, in the beginning of Part II of this dissertation it was said that, although certain decisions might, theoretically, seem to be the better choices to make, many design choices are made based upon the practical considerations surrounding the complexity of the system.

When reading through the next few sections keep the following in mind:

1) The ECG monitor needs to be as small as possible.
2) From the latter, using as few batteries as possible.
3) The ECG monitor output needs to be as accurate as possible because in a real time sports environment type of application a lot of unwanted external noise sources not usually present in an ECG signal, are interfering with the signal of interest. (E.g. Bumping feet, heavy respiration, excessive muscle contraction and excessive body-electrode movement artefact.)
4) An open mind needs to be kept when interfacing the analogue circuit to the rest of the ECG and heart rate monitor because there will still be an additional digital and RF part to the monitor.

5. Proposed Front End Solution

Proposed Solution

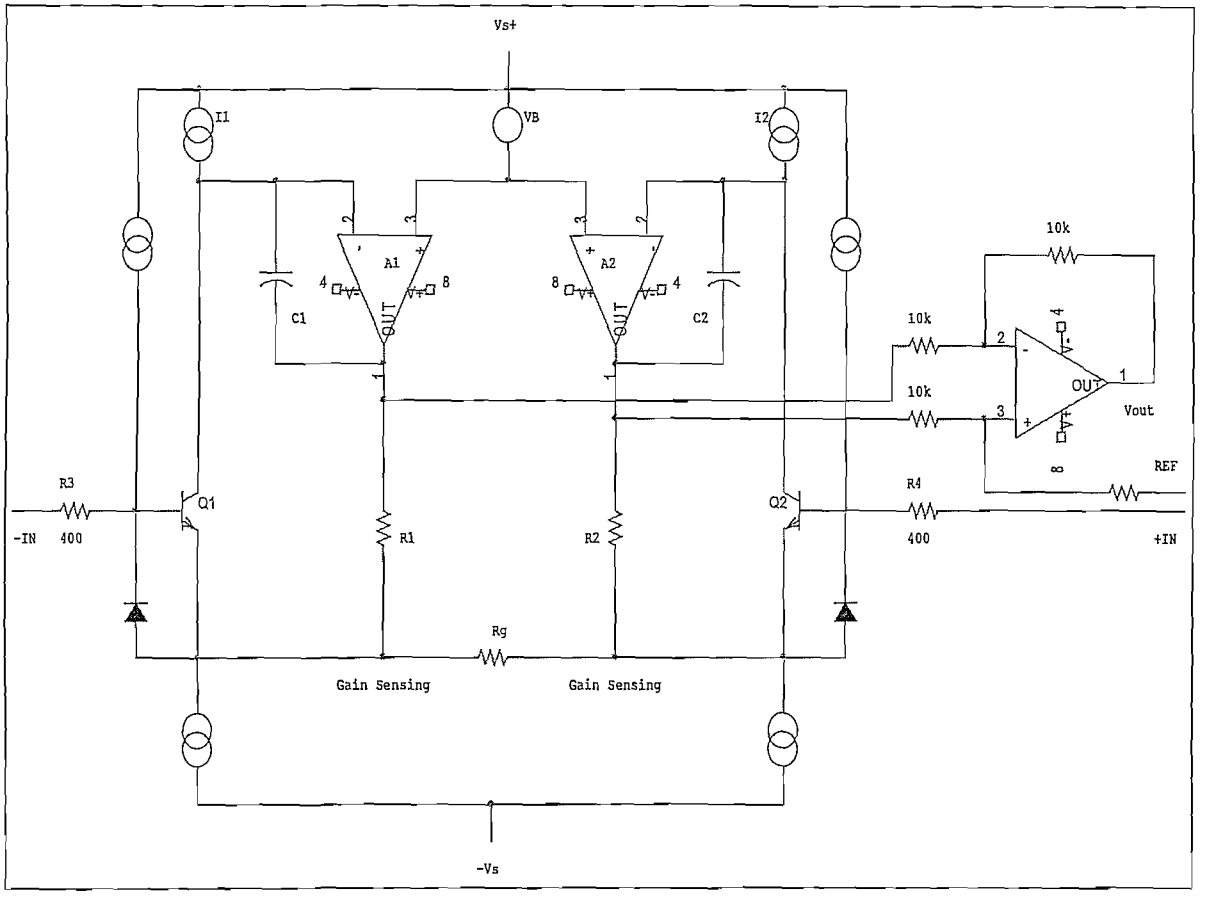


Figure 14: Proposed Front End to ECG Monitor

Figure 14 depicts the custom front end solution intended for use in *this* application.

As described previously this type of I.A is a deviation of the classical three op amp design. Gain achieved from this circuit is user programmable by changing only one resistor, R_g.

A single differential-pair bipolar input for great precision is provided by transistors Q_1 & Q_2.

The Q_1 to A_1 to R_1 and Q_2 to A_2 to R_2 feedback loop assures constant collector current in the input transistors Q_1 & Q_2. The input voltage is hereby impressed across the external gain resistor R_g. [2][1][14]

One of the main ideas of an I.A operating in this manner is just this, giving the user the freedom of choice as to how much gain is taken at the front end of the design.

Inherently to the circuit then is the differential gain developed at the outputs of the two op amps from the inputs. The gain can be calculated as $G=\left[\frac{R_1+R_2}{R_G}\right]+1$. It should be relatively easy to see that this equation can be derived from figure 14 by making use of the basic laws of ohm and op amp theory. Refer to appendix F for a detail description of the amplification calculation.

Finally there is a unity gain subtraction. This happens at the third op amp. A single ended output is created and referred (to) as the Reference pin potential.

In the last place R_g determined the gain of the circuit, or in other words, the trans-conductance of the pre-amp stage.

The two main circuit gain resistors R_1 & R_2 are selected to be 24.7kΩ.[14] These two resistor values can in fact be chosen as other values. The only important factor is that they have the same value in order to keep the system balanced. Care should also be taken not to select the values to be too high. This will result in additional unwanted noise in the I.A stage. Gain can now be programmed quite accurately by changing R_G. Refer to the previous paragraph for the equation. The

mathematical function for determining the gain can be expressed as $G = \left[\frac{49.4k\Omega}{R_G}\right] + 1$.

Again, refer to appendix F for a detailed description on this calculation.

From this the gain for a certain value of R_g may be determined and also the value of R_g for a wanted gain can be determined.

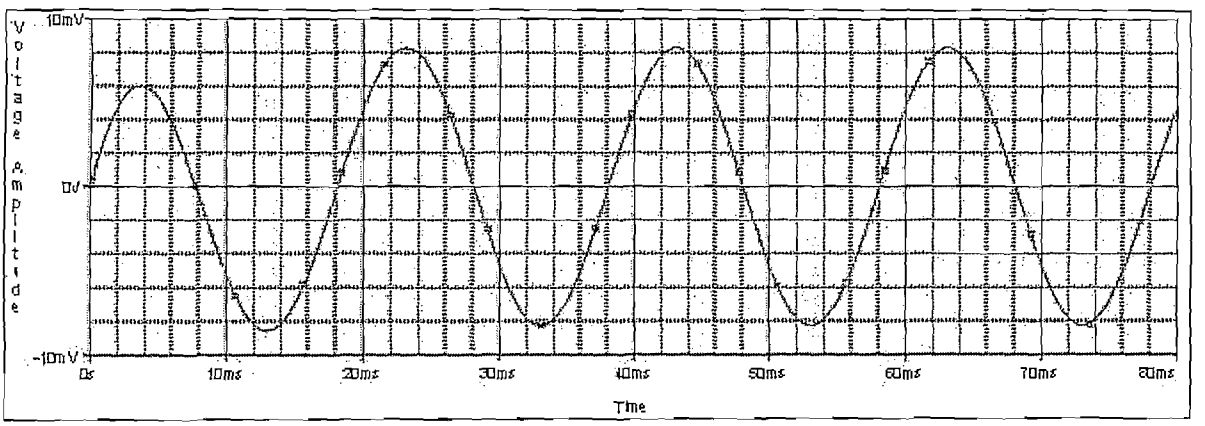


Figure 15: Typical signal across R_G for a 50Hz input signal

Figure 11 depicts a typical signal generated across R_g for a 50Hz input signal of 3mV.

Typically as R_g reduces to produce a larger gain, trans-conductance will increases asymptotically to that of the input transistors. Theoretically this has an advantage; Open loop gain is high so that programmed gain can be increased. This means that gain related errors are reduced.[6][8]

Also, gain-bandwidth product increases with programmed gain. By this frequency response of the amplifier is optimized. Remember that the gain bandwidth product is determined by C_1 & C_2 as well as the pre-amp trans-conductance.

5.1 Overcoming the Battery Problem

Dedicated Design Supply Issue

Previously a discussion on the issue of size, space and weight was given. Usually when an I.A is implemented a dual power supply is needed because the I.A is fed with a positive and negative supply.

In principle this is not a problem in the design of an ECG monitor. However, for this specific application using two or more batteries creates a space, packaging and weight issue.

Take a look at figure 14 again. The circuit was designed in such a manner that unity gain is subtracted in the last stage of the amplifier. A single ended output is created and this potential is referred to an accessible pin for external usage. It becomes clear by studying the circuit of figure 14, that any applied voltage to this reference pin will become the so called "ideal ground" or wanted reference for the output signal. Figures 16 and 17 demonstrate this.

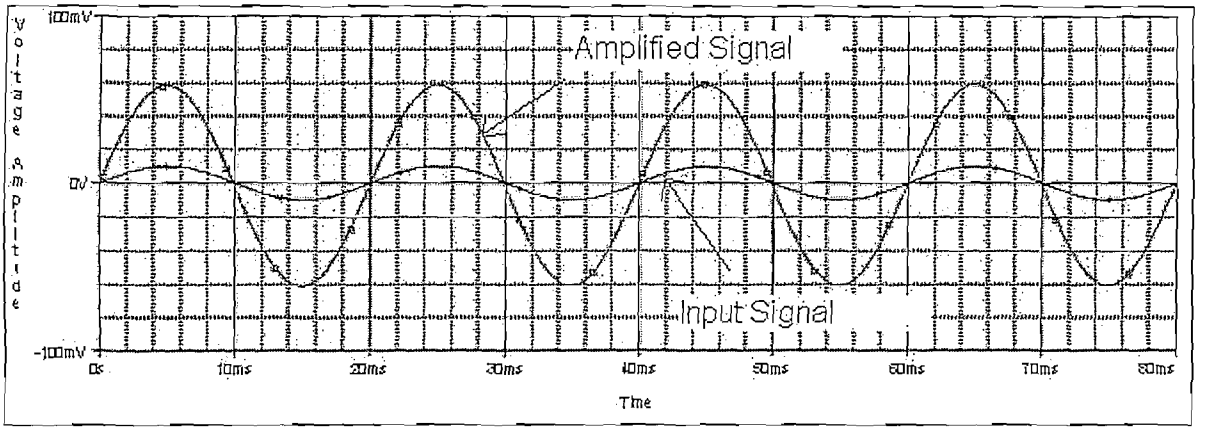


Figure 16: Typical Input/Output of an I.A with a dual voltage supply

It can be seen from figure 16 that the I.A was supplied by a positive and negative voltage supply. The input signal has no offset and is a typical 50Hz sinus

wave. The red graph is the input to the I.A. The green graph is the typical expected output after a little amplification.

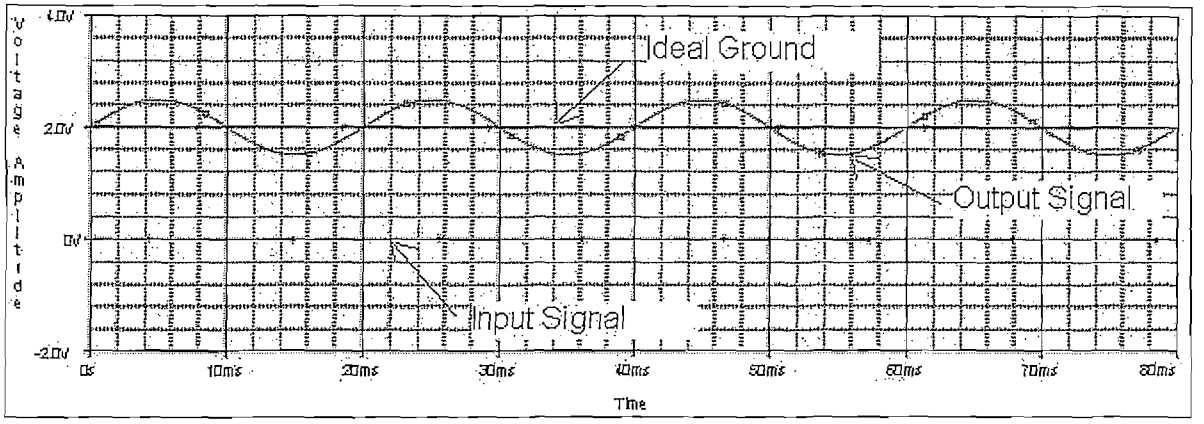


Figure 17: Typical Input/Output of an I.A with a modified power supply

Figure 17 depicts an output from an I.A with a slightly modified power supply. In this case a voltage of 1.6V has been supplied to the reference pin. The input signal however still swings around 0V. The outcome of such an adjustment is clear from figure 17. The input signal is taken, amplified and the output swings around the referenced voltage or "ideal ground".

This flexibility allows the user to make use of a single power supply or battery for the application of the ECG and heart rate monitor. However, again all is not as simple as it seems.

5.2 Obtaining Precision from a Single Supply Instrumentation Amplifier

Dedicated Design, Precision Issues

From previous discussions it is known that for *this* application of an ECG and heart rate monitor, practical considerations call for a single voltage supply.

It is also known that single supply I.A's are available for use below the 5V margin. Though it seems easy to make use of any one of these products, it is also a fact that great attention to detail is required to achieve a high level of accuracy and precision from such an I.A.[1][13][14] Although single supply I.A IC's are available, these products trade off DC and AC performance for low supply voltage and current. [13] Trading off DC performance in this application is not an option due to the already, very low DC values present in an ECG signal. Remember that one of the most critical issues to be dealt with when acquiring an ECG signal is just this, ridding the signal from unwanted DC components. If AC performance is traded off, ridding the signal from the unwanted external noise forms as discussed in the beginning of Part II will simply become more difficult as all of the noises are of an AC nature.

Because the majority of sensing applications provide an output signal swinging around a 0V or ideal ground (reference signal), achieving high precision performance in a single supply application is a practical issue. [1][8]

Maximum dynamic range at the output of such circuits is always important. Thus, the output voltage range of the circuit should be as large as possible and the conditioning circuitry should not operate at the extremes of the input voltage range. [14]

The following circuitry proposes a solution to the desired accurate and precise front end while only operating on a single voltage supply.

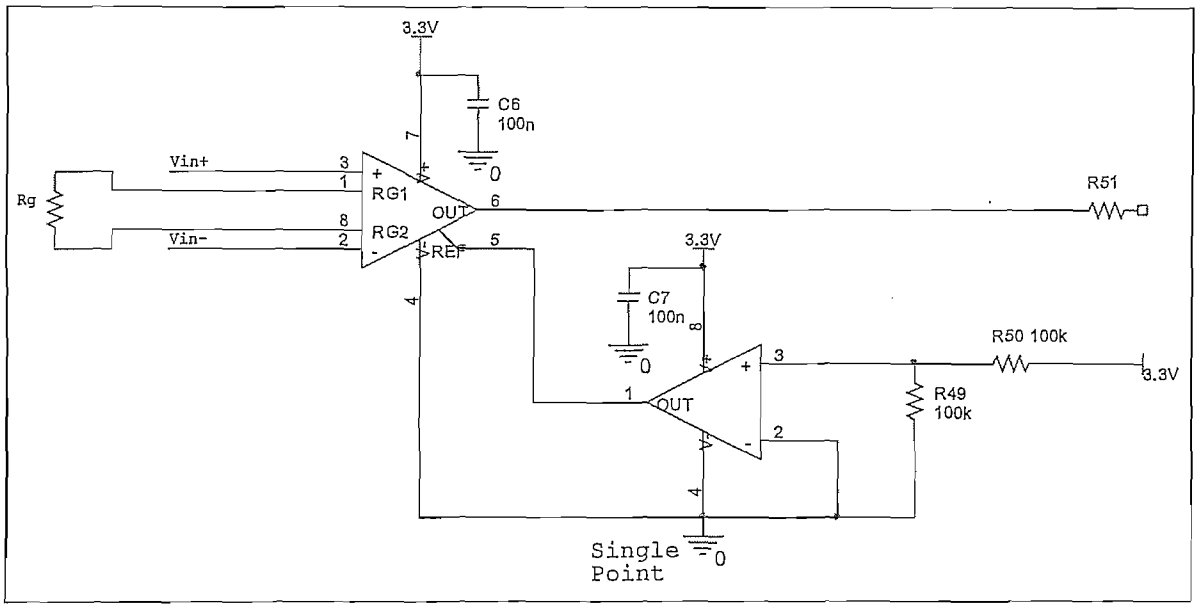


Figure 18: Stable Referencing of an I.A

Figure 18 is a custom design for this ECG monitoring application and forms part of the patent application.

The following example discussion is simply included and based upon simple electronic fundamentals in order to explain the reason for the design topology as depicted in Figure 18.

The challenge is to reference the I.A with a stable "ideal 0V" supply.

In this example an I.C was used as a composite I.A. The second I.C (an operational amplifier) shown is configured to be a voltage follower. R_{49} and R_{50} are configured to be a common voltage divider. The output of the op amp is a stable $\left[\frac{3.3}{2}\right]V$. This output provides a low impedance source for the I.A reference pin.

A low impedance source is required to maintain high common mode rejection with the I.A. It is also worth noting that the output of the op amp can drive load currents of up to 20mA under normal conditions which makes way for additional

external circuitry without affecting any later amplification circuitry as will be discussed shortly.

The I.A maintains its high linearity performance with a single voltage supply because its front end is actually configured to operate from a dual voltage supply. The circuit however relaxes its output drive level.[4] Because the voltage divider shifts the entire signal above ground level the final output is measured with respect to $\left[\frac{3.3}{2}\right]V$ and not 0V.

However, even though this design is feasible and makes for a very attractive solution the overall DC and AC tradeoffs to voltage level and current consumption is of major concern and a better solution need to be found. Due to the background and constraints put on the design by the essence of the project the battery must be as small, light weight and durable as possible. It simply is not acceptable to design for a battery that will operate for less than at least two hours under continuous RF transmission and reception conditions. This is to have the system working for at least half an hour longer than the duration of a long rugby, soccer or other sports event.

The best solution for this scenario was found on a standard, now almost obsolete technology, coaxial network cards used for communications between computers. A DC voltage inverter was implemented on the design to supply the I.A with a negative voltage equal to the positive voltage applied to it and the other supply pin of the I.A itself. The reference pin of the I.A can now be connected to the ground plane (0V level) of the design. This makes for the best solution of the problem simply because the design is very small. Again, a decision taken based on practical considerations after the theoretical impacts have been studied as discussed in the previous few paragraphs.

By making use of a voltage inverter running at a very high frequency (48kHz) it was easy to filter out any noise generated by the inverter itself as this noise lies far outside the bandwidth of the ECG itself. (0.5 – 120Hz) The frequency of the voltage

inverter was also chosen with the communications design-*part* of the ECG monitor in mind. The frequency of the inverter should not interfere with the transmitter and receivers on the ECG monitor as this will cause communication losses. Considering that the transmitter and receiver make use of a carrier frequency of 433MHz any interference in this regard is kept to a minimum by choosing the inverter frequency at 48kHz. It also overcomes the trade off issues concerning DC and AC performance encountered when feeding an I.A designed to operate from a dual voltage supply, with a single supply, and referencing the output with an offset. The package of the voltage inverter is no larger than a 8-pin mini SOIC IC and can easily be incorporated into the design of the ECG monitor. Figure 20 depicts the final setup of the I.A used in the ECG front end design.

It can be seen by studying figure 20 that a dual supply I.A has been implemented and supplied by a positive and negative voltage supply. The negative supply is being generated by the onboard voltage inverter running at a relatively high frequency and the positive supply of the I.A comes from the same point which supplies the voltage inverter of a positive voltage to invert. The reference pin of the I.A is now connected to ground (0V) and thus all of the above mentioned and pre-discussed issues have been overcome.

Another important design issue that is overcome by this design is supply differences. Because the inverter is supplied by the same supply that feeds the positive supply of the I.A, any drop, increase or difference in the supply line will also be deflected to the negative supply of the I.A. This means that the dual supply of the I.A will always be balanced.

This type of implementation delivers excellent DC as well as AC performance under very low current consumption conditions, typically around $575\mu A$. (Empirically tested.) After careful consideration including availability and numerous comparison tests the I.A chosen for the job was the AD623 from *Analog Devices*. The gain of the AD623 can be set externally by the replacement of a single resistor to anything

between 1 and 1000. Furthermore, the AD623 exhibits the ability to have a *rail-to-rail* output swing.

The DC performance of the AD623 displays excellent performance; A gain accuracy of 0.1% was found with a gain equal to 1 (G=1) and 0.35% with a gain bigger than 1. (G>1). The AD623 has a 25ppm gain drift with a gain equal to 1 (G=1) and a $200\mu V$ max input offset voltage.[14]

The AD623 is available in a variety of different versions concerning temperature performance. The one chosen for this application was the AD623B which exhibits a maximum input voltage drift of $1\mu V/°C$. [14] The AD623 also exhibits excellent noise and CMR (Common Mode Rejection) specifications. $35nV/\sqrt{Hz}$ RTI noise at 1kHz with a gain setting of 1 (G = 1). [14]

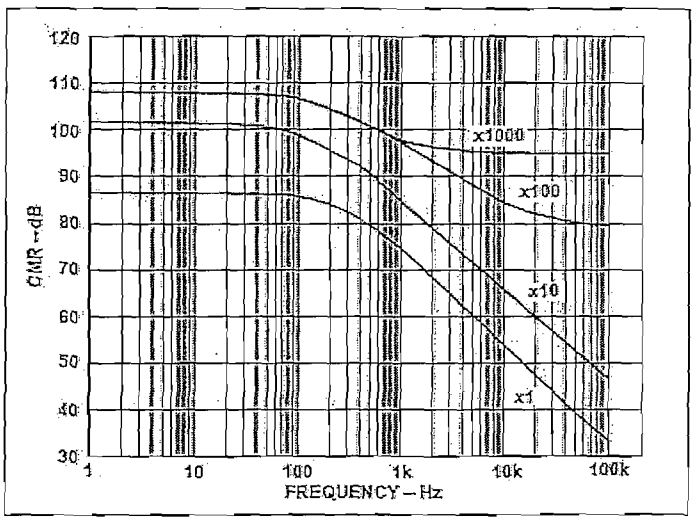


Figure 19: CMR vs. Frequency @ +5 Vs, 0 Vs

Figure 19 with acknowledgement to Analog Devices.

The AD623 holds errors to the minimum through excellent AC performance which increases as the gain setting increases. It can be seen from figure 19, that the

CMRR remain constant up to about 180Hz, which means that line noise and line harmonics are rejected with high accuracy. It can also be seen that since the bandwidth of an ECG signal falls between 0.5Hz and 120Hz and the CMR of the AD623 remains constant up to almost 180Hz the CMR within the data area of the ECG will be handled without any complications.

Lastly the AD623 also exhibits excellent AC characteristics. The I.A holds good performance up to almost 800kHz with a gain setting of 1 (G=1) and shows a $20\mu s$ settling time.[14] For comparison and to show that CMRR increases with gain, it can also be seen from figure 19 that the AD623 exhibits a 90bB minimum CMRR with a gain setting of 10 (G=10) and a 84dB minimum CMRR with a gain setting of 5 (G=5). These results were achieved with an input frequency of 60Hz and a $1k\Omega$ source imbalance to ensure imperfect test conditions as are usually encountered in real world applications.

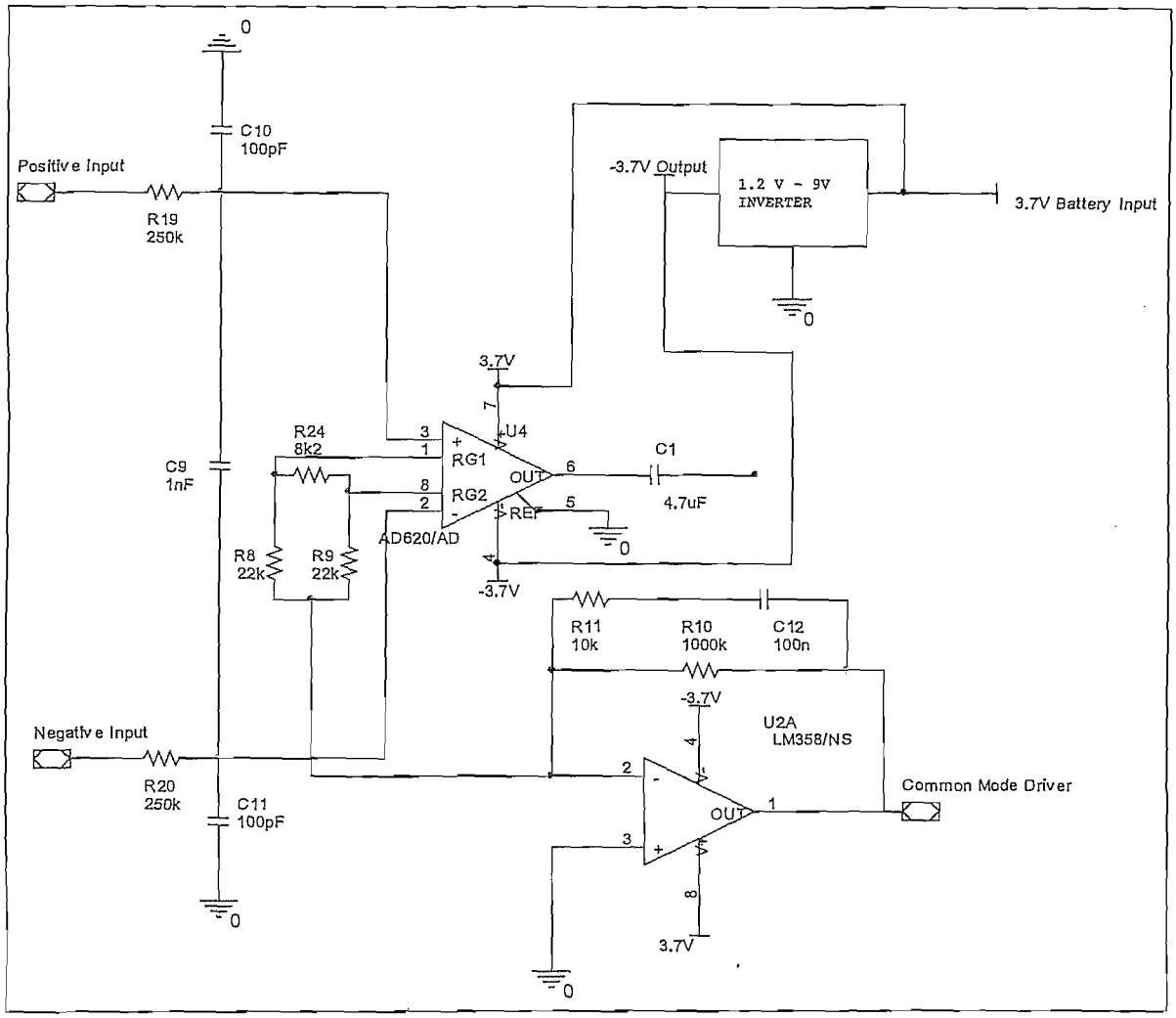


Figure 20: Final I.A front-end design

6. A Quick Review

Design Review before Continuing

So far a conclusion has been reached that using a dedicated I.A design will be in the best fit the theoretical and practical needs of this application. It can also be concluded that it is possible to manipulate the design of this circuit to such an extend

that accurate and precise front end amplification will still be possible even if an I.A in need of a dual voltage supply is used but only a single supply is available.

Thus, issue of not losing accuracy or giving up any precision have been overcome. The common problem of not being able to sample an analogue signal swinging around 0V as a midpoint and referenced against a single voltage supply has also been dealt with.

There is however still one more issue to be overcome in terms of total freedom of manipulation of the analogue signal (or any analogue signal swinging around $0V$ for that matter). A microcontroller is implemented on the ECG monitor, not only to allow for communication manipulation, filtering assistance and monitor control but also to handle the analogue-to-digital conversion of the ECG signal. With a microcontroller operating from a single supply the problem is that only the top half of the ECG signal will digitally be converted correctly. The latter is a result of the output signal from the I.A being swung around $0V$ after being referenced against this point and handled in this matter throughout the rest of the analogue filtering stages implemented on the ECG monitor. The solution to this issue however, will be discussed later, after a complete discussion of the analogue and digital filtering techniques following the I.A and implemented on the ECG monitor.

A point has now been reached where enough information have been gathered about actually acquiring the ECG signal and thus, it is now possible to start discussing the actual analogue and digital filtering techniques as they will be implemented on the ECG and heart rate monitor. It is in these techniques where the heart of the success of the system lies. But the devil is in the works again. Filtering techniques which allow for accurate, fast and reliable results in the environment where *this* ECG monitor will be implemented calls for a design of a totally different scope.

7. Filtering the Raw ECG Signal

Analogue Filtering

From the previous discussions it is now known that the environment wherein this ECG monitor will have to operate places enormous constraints and design specifications on the system. To rid an ECG signal of unwanted noise by means of filtering processes, while the subject of whom the ECG is monitored is not moving and thereby not producing even more inherent noise to the signal is relatively easy. But doing so for a signal where continuous random, non-predictable noise is added to the raw signal calls for a combination of analogue and digital filtering techniques, interlocked in such a fashion so as to let the result of the one compliment the result of the other.

7.1 Interlocking Different Filtering Techniques

Interlocking Filters

As the use of a microcontroller was mentioned a few times up to now, the next issues to be dealt with are the constraints placed on the system by the microcontroller.

Making use of a microcontroller seems the way to go. This will allow for easy access to the outside world by intercommunication to and from the RF transmitter and receiver onboard the ECG monitor. It also allows for good and relatively easy manipulation of the analogue signal by converting it to a digital representation and having the ease to evaluate, amplify and transmit this representation of the original analogue signal at hand. But, inherently when the word *microcontroller* is used, the term, *timing,* becomes an issue. It is no hidden fact that converting an analogue signal to its digital representation, reading this value, manipulating this data, possibly

encoding this data for RF transmission, communicating with the RF transmitter, transmitting and receiving a reply, takes up time. And time it does take up, a lot of it. Even though a microcontroller driven by a 20MHz crystal which results in a clock cycle of $50ns$, is intended for use in this application, a few of these cycles together quickly becomes a few milliseconds and the microcontroller runs out of processing power. The system starts lagging and important data is lost.

The constraints of weight and packaging placed upon the final design in order to keep the ECG monitor as small as possible and as little irritable to the athlete as possible have also been discussed.

Although an all analogue design will result in an *always in time* design, should one should decide to implement only analogue filtering techniques to rid the raw ECG signal of noise the design quickly results in a bulky electronic system with no other option than letting your physical design size grow until all components fit onto the final layout. Also, one of the most basic concepts taught in basic electronic design theory is this; More electronic components (operational amplifiers, resistors and capacitors) result in more noise in a circuit, and also result in energy usage and finally battery-life is shortened. Athlete comfort, size and weight will be contemplated.

In the same way doing all the filtering in the digital domain will result in the ECG monitor, or more precisely the microcontroller onboard the ECG monitor, running out of processing power and not being able to sample enough points on the ECG signal to reproduce a good accurate and clean ECG signal representation. Simply put, the resulting signal will be seriously damaged by the effects of aliasing.

For these reasons and possibly others not even considered in such detail the final design needs to be one where analogue and digital filtering techniques are interlocked, working together and complimenting each other. All of this in order to produce a final, clean ECG signal in such time which will allow for sampling the signal, reading the sampled value, manipulating the data, encoding the data, transmitting the

data, receiving a reply upon transmission of a data point, resending lost data, and be back and ready in time to sample the next value of the ECG signal and still comply with the digital sampling theorem. (The sampling theorem is to be discussed later when the digital filtering techniques are discussed.)

7.2 The Filtering Processes

Filtering Processes

As has been mentioned earlier, the result of measuring the electrical activity of the heart muscles is called an ECG. Measuring this activity under continuous strain and inside a real-time environment while athletes are competing or training realizes a much more careful approach to the design process of the ECG monitor, but more important, it places much more strain on the approach of the filtering processes. For starters, an immense amount of noise, (bumping feet, excessive respiration and swinging arms), not usually present in an ECG system now also need to be filtered.

The various noise types that were considered are:[9][11][13]

1. Electromyographic interference;
2. Network interference;
3. Base-line-wander, due to respiration;
4. Abrupt base-line-wander, as a result of excessive movement;
5. Instrumentation noise as a result of electromagnetic interference;
6. Composite noise constructed from all of the other noise types and
7. Electrode-body artefact.

It seems like the appropriate time to give visual representations of the destruction of the ECG signal caused by the different kinds of noise as described above to shed more light on the seriousness of corruption these noise sources induce.

For the purpose of pictorial explanation, the x and y scales on the following graphs can be neglected as they only represent a quantised value of the DC value of the captured ECG signals and the amount of sampled points in each representation respectively.

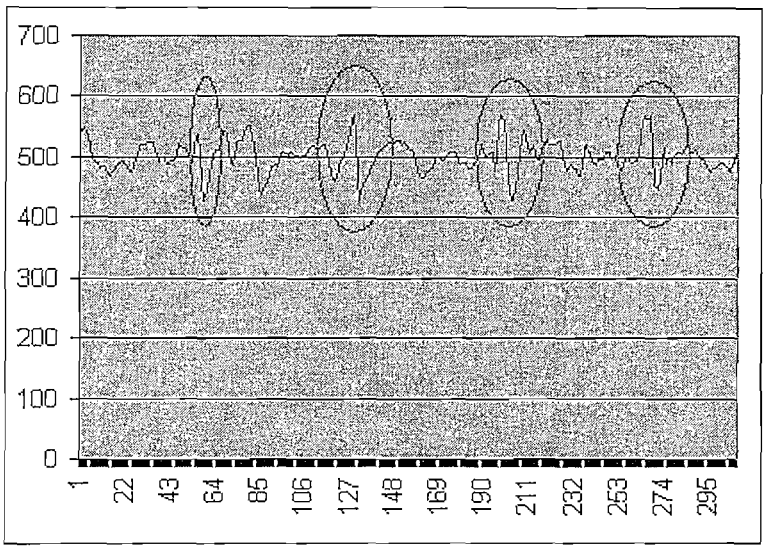


Figure 21: Network Interference destruction of an ECG Signal

Network interference consists of the ever so present 50Hz or 60Hz pickup and harmonics, which can be modelled as sinusoids. Characteristics, which might need to be varied in a model of power line noise, include the amplitude and frequency content of the signal. Figure 21 depicts how a power signal typically affects the ECG signal.

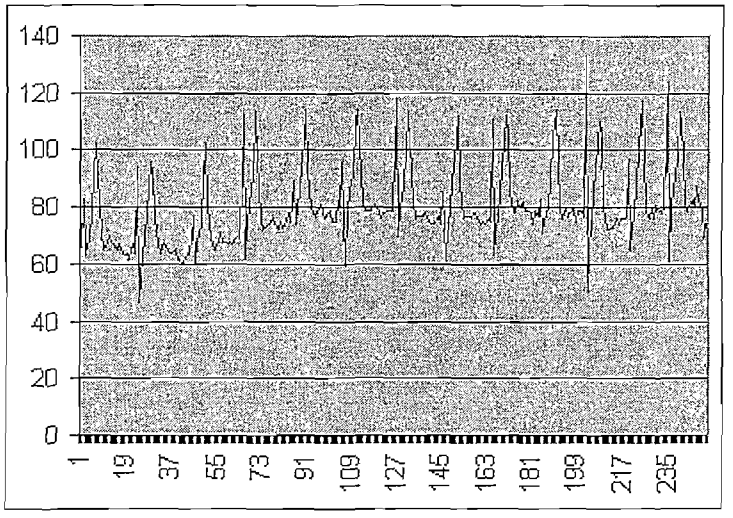


Figure 22: Motion Artefact Destruction of an ECG Signal

Motion artefacts are transient base line changes caused by changes in the electrode-skin impedance with electrode motion. As this impedance changes, the front-end of the ECG monitor (the I.A input) sees different source impedances (the human body), which forms a voltage divider with the amplifier (I.A) input impedance. The usual cause of motion artefact is movement of the subject's muscles with respect to the bones they are attached to which in turn causes movement of the skin.[17] Electronically translated the source impedance changes as the electrode-skin position changes. The peak amplitude and duration of the artefact is variable, as illustrated in *Figure 22*. This type of interference causes an abrupt shift in the base line of the signal.

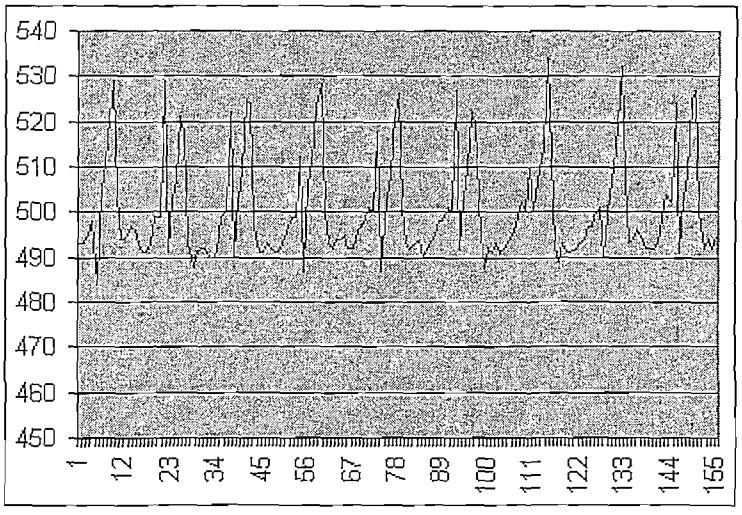


Figure 23: Muscle Contraction Destruction of an ECG Signal

Millivolt level potentials are generated by muscle contraction. Because the base line of muscle contraction is usually in the microvolt range[17] it usually is insignificant. It is difficult to capture an exact graph of muscle contraction noise interference on the ECG and therefore this type of noise is simulated and depicted in Figure 23. The maximum noise level is formed by adding random single precision numbers of 50 percent of the ECG maximum amplitude to the uncorrupted ECG signal. The following FFT is representative of the miss-formed T-wave of the ECG signal in figure 23 but in the frequency domain.

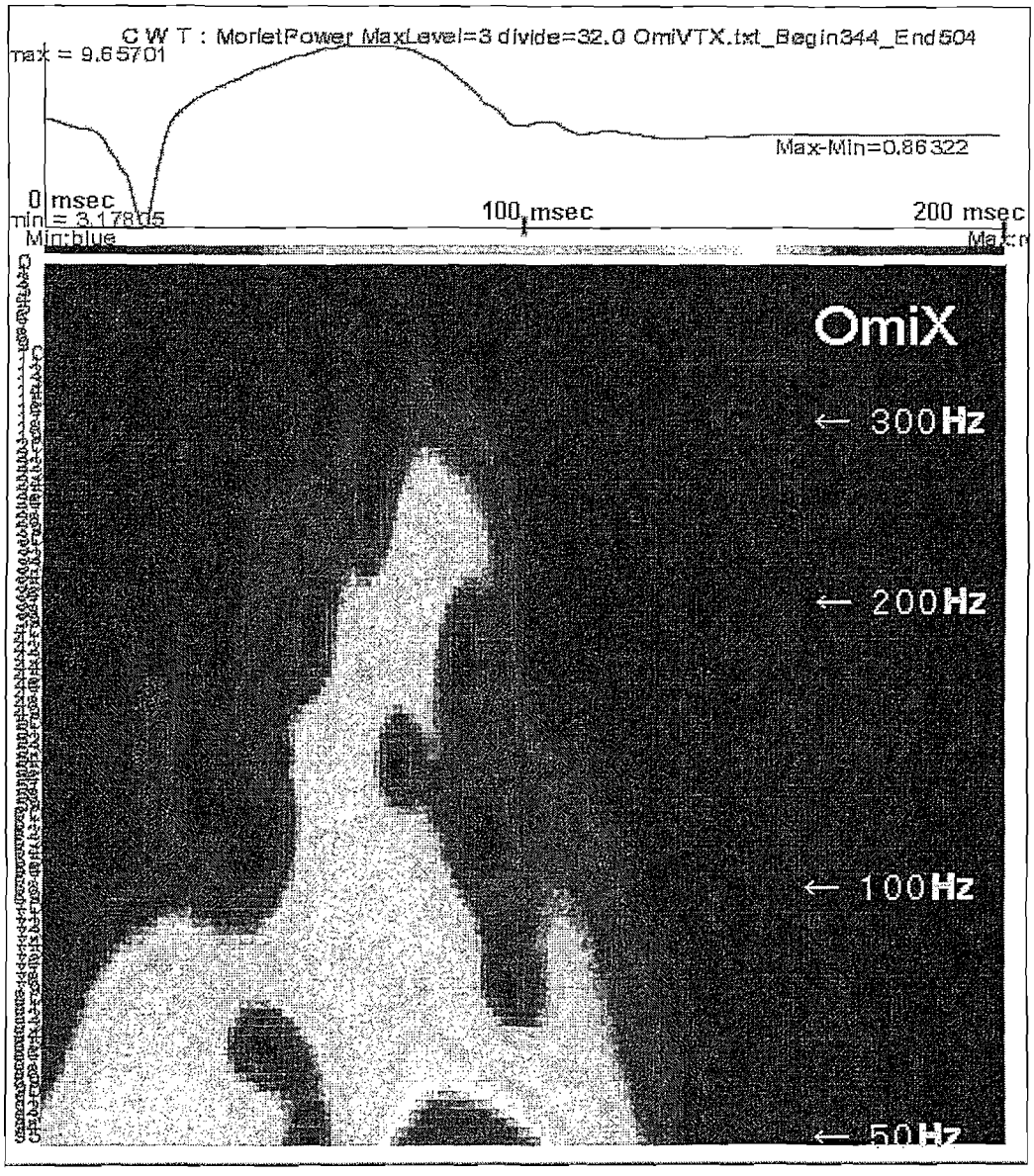


Figure 24: FFT of Contaminated T-wave

As can be seen in figure 24, a contaminated ECG signal may contain frequencies as high as 300Hz.

Figure 25: Base Line Wander Destruction of an ECG Signal

Excessive base line wander occurs with heavy respiration, especially when an athlete is running. The drift of the base line with respiration can be presented by a sinusoidal component at the frequency of respiration. The amplitude and the frequency are variable but can be found well below 0.05Hz.[13][17] Figure 25 depicts an ECG signal corrupted by base line wander due to heavy respiration.

Electro-Surgical interference completely corrupts the ECG signal. This interference usually occurs at frequencies approximately between 150Hz and 1MHz. Since the bandwidth of the ECG lies approximately between 0.5Hz and 120Hz it is relatively easy to filter out these interferences. Also, this type of interference only occurs inside an operation room where other types of electronic devices operate at interfering frequencies.[17] Thus, for the purpose of this research, this type of noise has been neglected.

Interference from any kind of electronic devices is hard to predict and a precise algorithm for filtering out these interferences cannot be designed. In this case manual preventive action needs to be taken and one need only be aware of this.

The above mentioned forms of noise can be sorted into four major categories resulting from the noise injection mechanisms or coupling methods. The four categories are:[9][17][18]

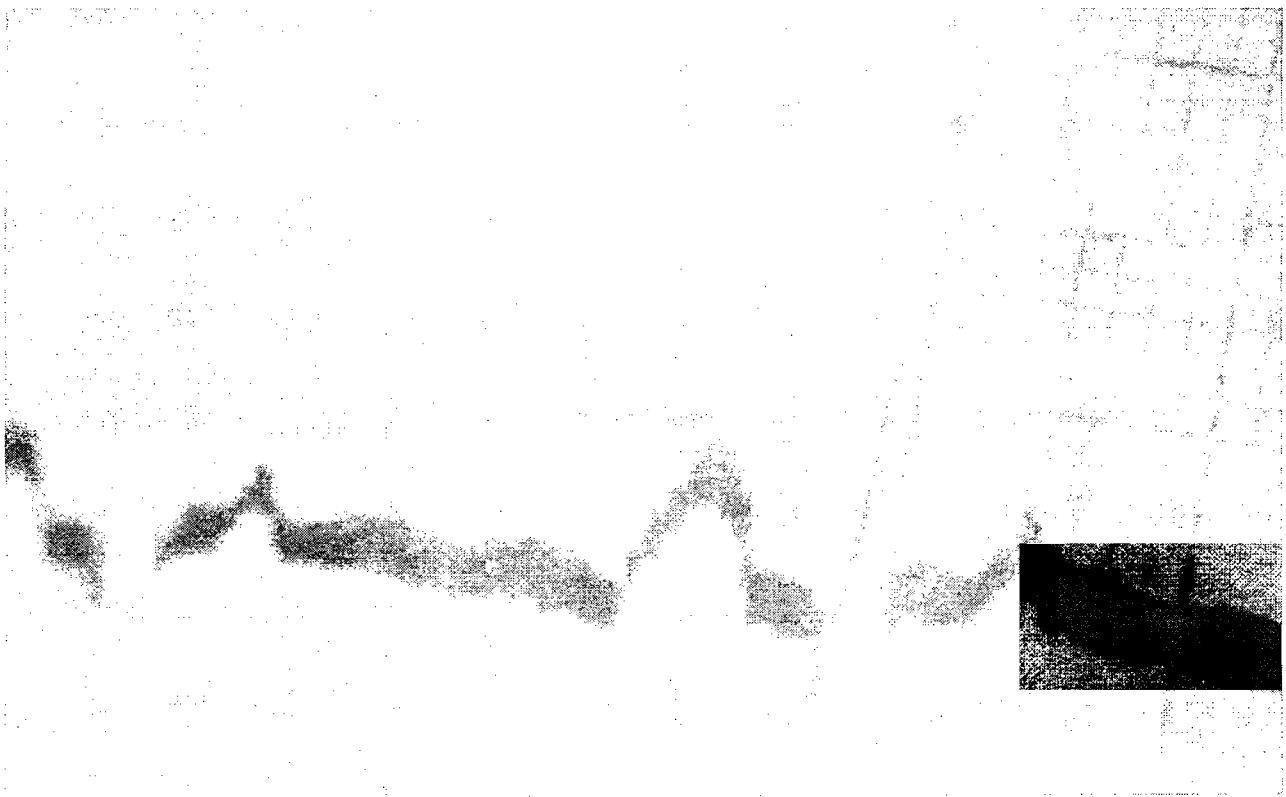
1. Inductive
2. Capacitive
3. Conductive
4. Radiation

Now that the different types of noise present in *this* system have been categorized, different filter structures can be presented to eliminate these diverse forms of noise. Their performance will be discussed with reference to efficiency, distortion of the signal and the effect of the filtering process on the RF transmission of the final manipulated data.

By now, a method for acquiring the basic raw ECG signal from the human body has been designed. Acquiring an accurate ECG signal calls for the implementation of a precision differential instrumentation amplifier as discussed in detail previously. Processing this raw signal into a useful, interference-free ECG signal will entail the following processes in the order they will be discussed throughout the next part of this dissertation:

1. Transferring the output signal of the I.A to the first filtering stage (Analogue domain) for the ECG bandwidth selection.
2. Amplifying the ECG signal to appropriate levels for digitization by the microcontroller (Analogue domain).
3. Applying the correct DC level shift to the signal before digitization (Analogue domain).
4. Digitizing the latter stages' output signal for network interference filtering (Digital domain).
5. Preparing the signal for RF transmission (Digital domain).

Design Documentation



1. Front-End *to* Filtering Processes

I.A output to Band-Select Filter Input

As discussed in the previous section, the front end of an ECG monitor must be able to sense extremely weak signals. Even a strong ECG signal almost falls below 5 to 8mV peak to peak.[17] The typical electrical considerations which have been taken into account while designing the front end were the following:

a) Signals to be sensed are between 0.1mV and 5mV *peak.*
b) Bandwidth of the ECG signal falls within 0.5Hz through 120Hz.[17]
c) Common mode rejection should be as high as possible.
d) Very high input impedances are experienced by the front end and,
e) Power supply considerations.

With reference to figure 16, the best idea would be to implement a capacitor between the I.A output and the input to the following filtering stages. This was done because a continuous DC shift of about $300mV$ was found to be present in the signal exiting the I.A. It was later found that this DC shift is a result of the "*electrode-skin contact effect*".

The "*electrode-skin contact effect*" acts as a voltage divider together with the input impedance of the I.A and it is this phenomenon together with the maximum input voltage offset of the I.A which allows for this $300mV$ output signal DC shift. Not ridding the signal of this DC shift might hold serious implications for the rest of the analogue circuit. Taking into account that the power supply to the circuit is $\pm 3.7V$ and that the raw ECG signal strength may vary from subject to subject and the fact that a good electronic design will never allow for a circuit or components to operate near or at its absolute maximum ratings, a very strong raw ECG input signal entering the filtering stages of the circuit may saturate the operational amplifiers on which the analogue filtering processes are based. The result may be the loss of data through the filtering

stages, a clipped signal, or even worse, a totally destroyed manipulated ECG signal entering the ADC (analogue-to-digital conversion) process.

2. Entering the First Filtering Process

- *Selecting the ECG Bandwidth* -

Decisions before Band-Selecting the ECG

For eliminating all frequencies outside the band of the ECG a few technical issues as well as different options to eliminate them had to be considered. Thus, frequencies above approximately 120Hz, causing instability of electronic components and frequencies below approximately 0.5Hz, where base line wander takes place, had to be eliminated.

Before continuing with the design of the actual filter processes a graphical representation of the ECG bandwidth will be presented to support previous statements claiming that the bandwidth of a normal ECG is between 0.5Hz and 120Hz. The following few graphs are representations of a normal ECG signal in the frequency domain.

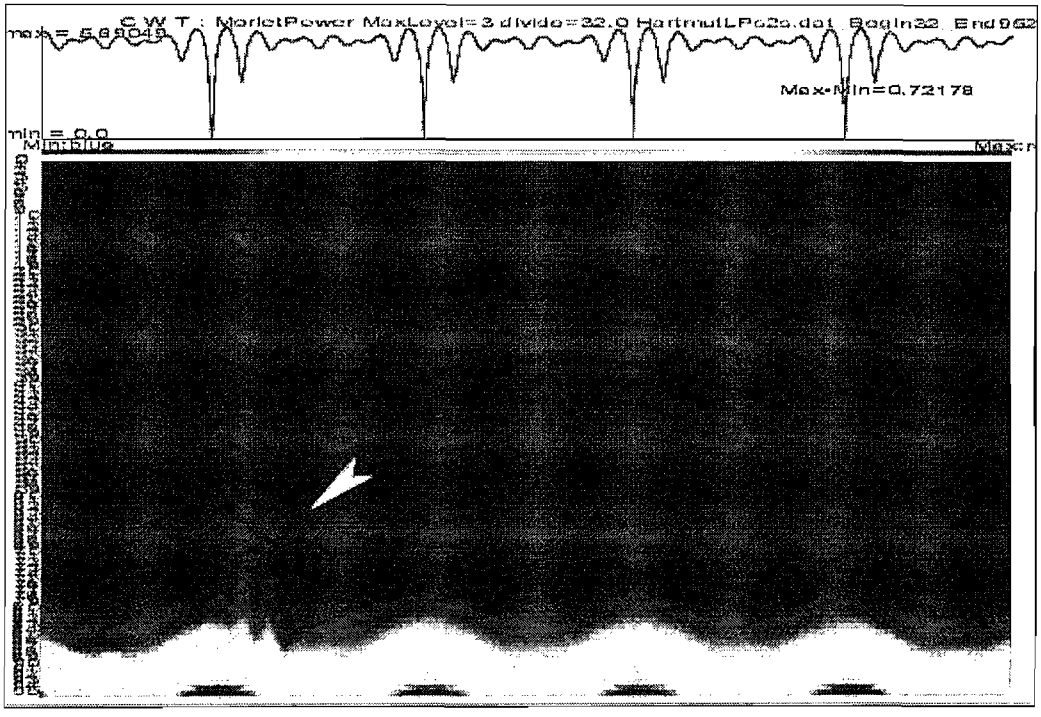


Figure 26: FFT of a Normal ECG Signal

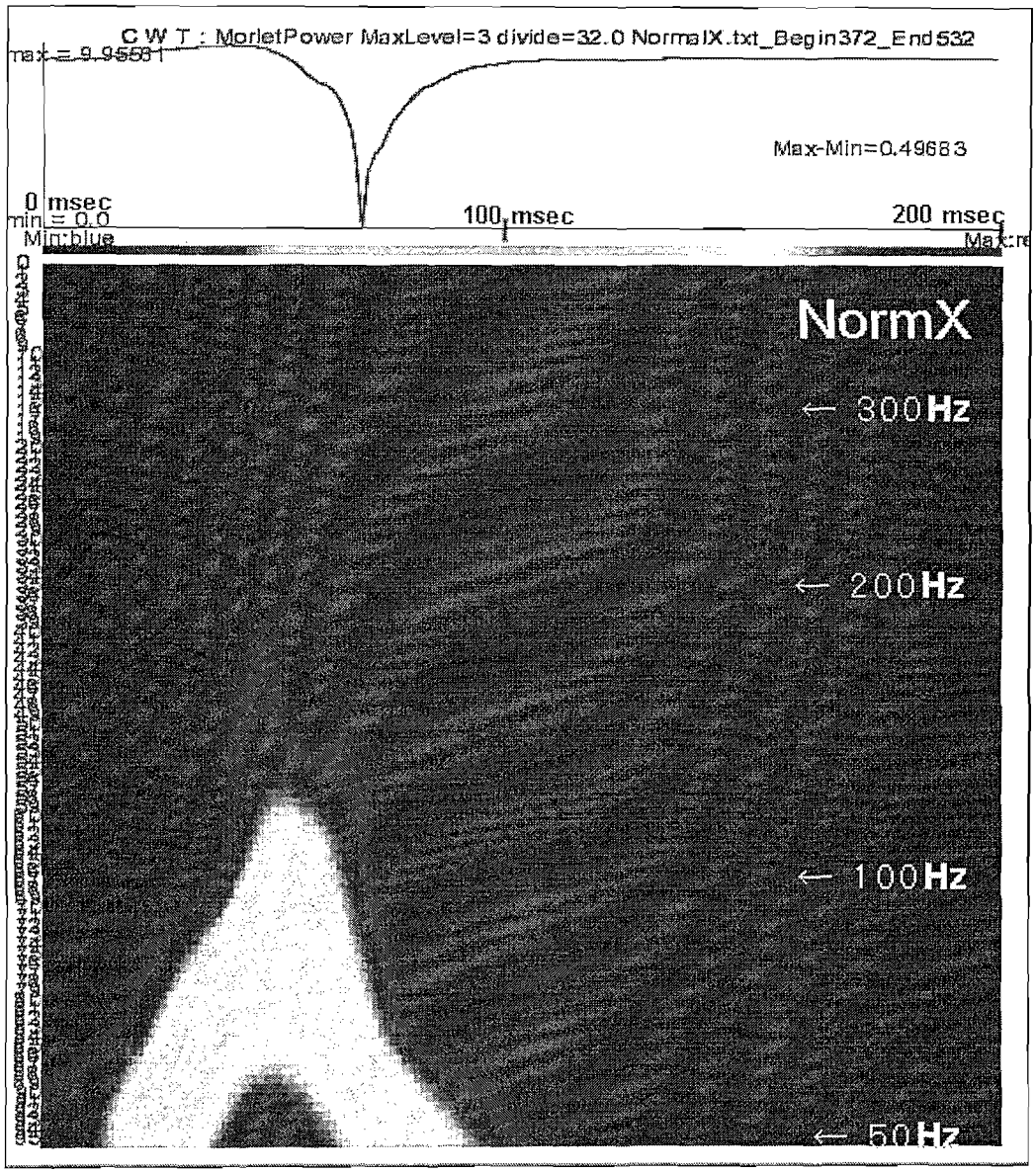


Figure 27: FFT of a normal QRS Complex

It can be seen from the previous two depictions that the bandwidth of a normal ECG lies well within 120Hz. A small amount of information lies outside this bandwidth as can be seen in figure 27 but this information is regarded as unnecessary information within the QRS complex which is the part of the ECG containing the highest frequencies.

Very high input frequencies to almost all operational amplifiers will disrupt the output of the following filtering stages. [1][6][8] For this reason a low pass filter is needed to cut out frequencies above the bandwidth of the ECG signal.

Very low frequency components severely influence the visual interpretation of an ECG signal [13][17] as well as the results obtained from computer based ECG analysis software. Removal of base-line-wander is therefore necessary to analyze the ECG and to minimize the changes in beat morphology. In other words, the information learned about the subject from the heart beat must stay consistent given consistent circumstances. Athletes participating or training generate a considerable larger amount of noise than do patients only taking an ECG stress test.[17] The bandwidth of such base-line-wander is then considerably larger than that caused by respiration and electrode impedance changes. Excessive base line wander occurs with heavy respiration, especially when an athlete is running. The drift of the base line with respiration can be presented by a sinusoidal component at the frequency of respiration. The amplitude and the frequency are variable but empirically, and can be found well below 0.5Hz.[17] This value has also, empirically been measured by fitting a sinusoid over the corrupted ECG signal. Figure 28 depicts an ECG signal corrupted by excessive base line wander due to heavy respiration.

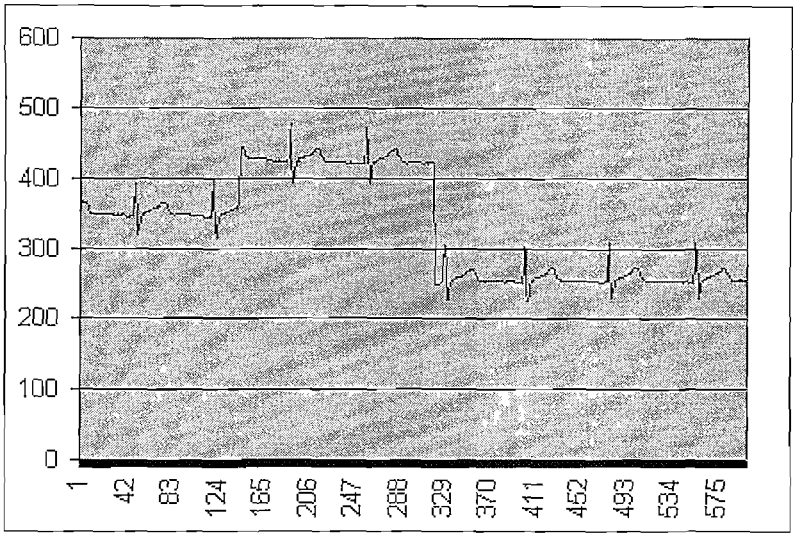


Figure 28: ECG Signal severely corrupted by Base-Line-Wander

Figure 28 depicts that it is possible to fit a sinusoid onto the respiration frequency of the human. It also depicts the 300mV offset referred to earlier. It can be seen that the respiration corruption of the ECG occurs about the 300mV offset.

Figure 28 shows that an abrupt DC shift (base line wander) is generated in the ECG signal. This is due to heavy respiration. Visual interpretation is heavily compromised and computer aided analysis will definitely also be defected.

2.1 Choosing the Correct Filter - *Selecting the ECG Bandwidth* -

Band-Selecting the ECG

Two main filtering approaches were considered for this filter design, *an analogue approach and a digital approach.*

-The Digital Approach-

Linear filtering can be used for base line wander removal or high frequency cut-off. This process holds the advantage of expressing the base line removal in spectral

terms. FIR filters is generally more acceptable than IIR filters due to the nonlinear phase response of the IIR filters. This nonlinear phase response can cause distortion in various important areas of the ECG signal. An IIR filter could, however, be used in a forward-backward filtering process which results in linear phase filtering. However, in this application using this type of filtering technique takes up a lot of the processing power of the micro controller on board of the ECG monitor. As the micro controller runs at 20MHz, taking into account that the micro controller needs to sample and convert the ECG signal to a digital representation and also process the data to be transmitted via RF, every clock cycle to spare is important. Data also need to be Manchester encoded by software before transmission, which takes up a considerable amount of time. (The reason for Manchester encoding the data before transmission thereof is a direct result coming from the understanding of basic telecommunication systems design. Encoding data both secures the data being transmitted from other channel users as well as stabilizes the data slicing components of the RF design on the receiving end of the system by means of the construction of the data in its encoded format. [19]) Albeit other encoding schemes may result in a better utilization of bandwidth to achieve the same bit rate, for instance 8B/10B, the scheme is more complex to implement and will result in even more processing time lost.

-The Analogue Approach-

The filtering technique chosen for removal of the base line wander is a non-adaptive technique. There are four widely used analogue filters namely, Butterworth, Chebyshev, Elliptic and Bessel filters. Many of which have advantages and disadvantages compared to each other. A Chebyshev filter was chosen for implementation in this design. The reason for choosing this type of filter will become clear soon. Two types are commonly found. Class I Chebyshev filters are all pole filters that exhibit equi-ripple behaviour in the pass-band and a monotonic characteristic in the stop-band. On the other hand, the family of class II Chebyshev filters contains both poles and zeros and exhibits a monotonic behaviour in the pass-band and an equi-ripple behaviour in the stop-band.[5][7][8] This means that the zeros

of this class of filters lie on the imaginary axis in the s-plane. It might, theoretically seem like a better idea to make use of an Elliptic (Cauer) approximation because of the known fact that Elliptic approximations in general, require lower order filters to achieve the same results as other filter approximations which again will result in lower component counts. No formal rigorous testing has been done but, a few iterations of Elliptic and Chebychev class II filters showed that the Chebychev class II filter tends to achieve a better delay performance when compared to an Elliptic filter of ver low order. In the following few graphs the Butterworth, Chebychev Class I, Chebychev Class II and Elliptic filters are compared to each other by means of their gain function, phase distortion, delay, step input, impulse reaction and pole-zero positions. The simulations were done for a low-pass filter with the following characteristics:

1. Filter Order : 2
2. Pass-band attenuation : 0.5dB
3. Stop-band attenuation : 30dB
4. Pass-band frequency : 100Hz
5. Stop-band frequency : 120Hz

Approximation:	Butter-worth	Cheby-shev	Inverse Cheby.	Elliptic	Bessel
Order	2	2	2	2	2
Circuit stages	1	1	1	1	1
Passband ripple	---	---	---	---	---
Pole pairs	1	1	1	1	1
Single poles	0	0	0	0	0
Zero pairs	0	0	1	1	0
Single zeros	0	0	0	0	0
Max. pole Qp	0.71	0.86	0.90	1.0	0.58

Table 2: Comparison Between 5 Different Filter Approaches

Table 2 compares the 5 different analogue filter approximations in terms of order, circuit stages, pass band ripple and poles. From the table it can be observed that the Elliptic filter approximation yields a maximum pole Q of 1. Further more is is

also visible that the inverse Chebychev and the Elliptic filters show the same amount of zero pairs, whereas the pole pairs are also of the same amount.

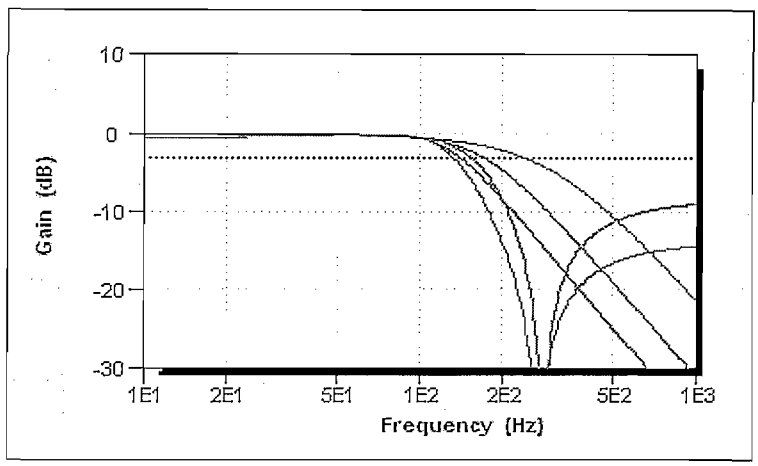


Figure 29: Comparison of Filter Gains

It can be seen from figure 29 that in terms of gain, the Chebychev Class II (red) and Elliptic filters yield almost the same gain functions. None of which complies to the stop band of 120Hz as was the intention. The latter is simply a result of a second order filter not being able to actually achieve 0.5dB attenuation from 0Hz through 100Hz and suppressing enough to achieve 30dB attenuation 20Hz later at 120Hz. (The 3dB line is plotted across the graph in the top for reference.)

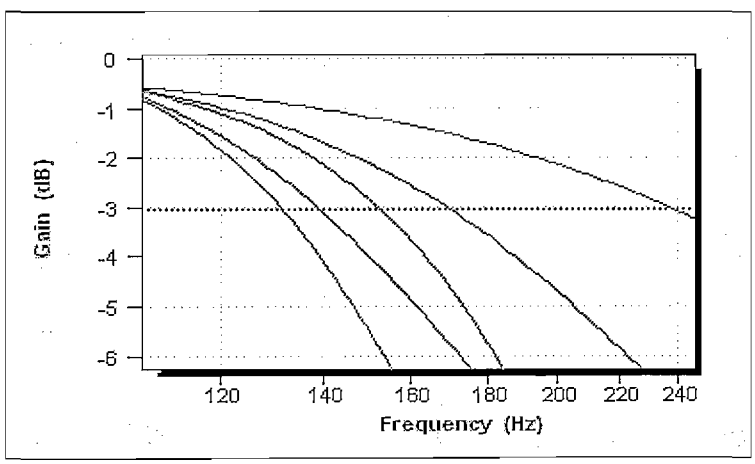


Figure 30: Enlarged graph of Figure 26.

Figure 30 is an enlarged graph of the portion of figure 29 where the 5 different filters cross the 3dB point. Although it can be seen that the Elliptic filter (purple) performs better than the Chebychev Filter (red) at the top of the curve, a mere 20Hz is not enough to eliminate an easier filter design. For this reason, as will also later be explained more analogue filtering techniques need to be implemented in order to restrict the bandwidth of the front-end to 120Hz.

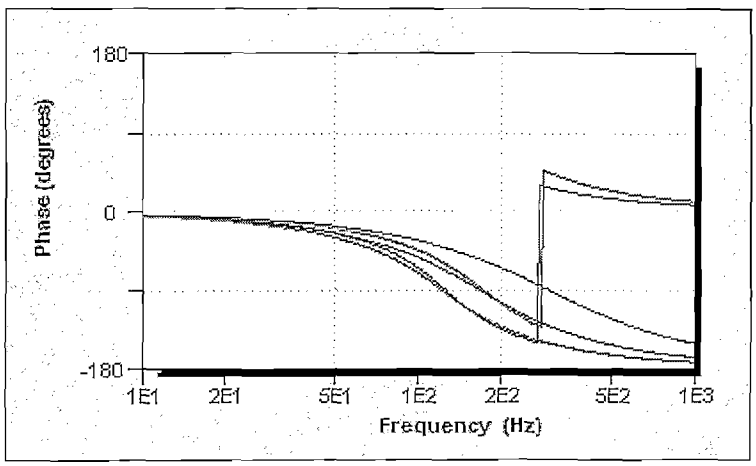


Figure 31: Phase Response Comparison of 5 Different Filters Approximations

It can be seen from figure 31 that the phase responses of the Elliptic (purple) and Chebychev (red) filters are not different enough to exclude either one.

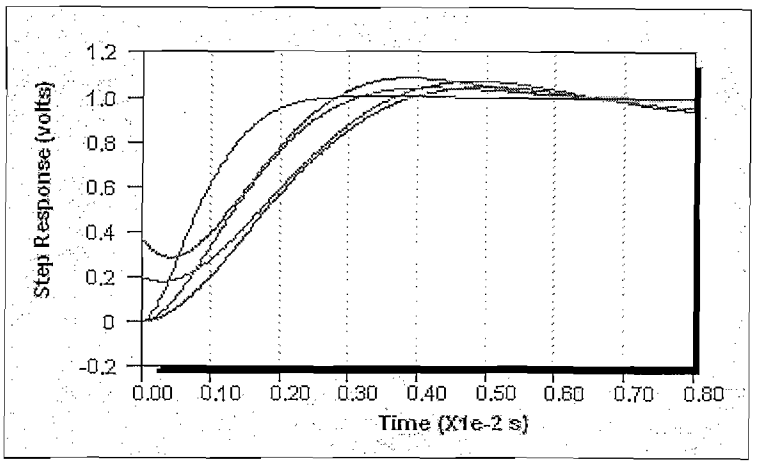


Figure 32: Step Input Response of 5 Different Filter Approximations

Figure 32 starts to give the first hint as to why a Chebychev filter was chosen rather than an Elliptic filter. As can be seen from the difference between the red (Chebychev) and purple (Elliptic) graphs, the Chebychev approximation yields a better step input reaction at lower frequencies.

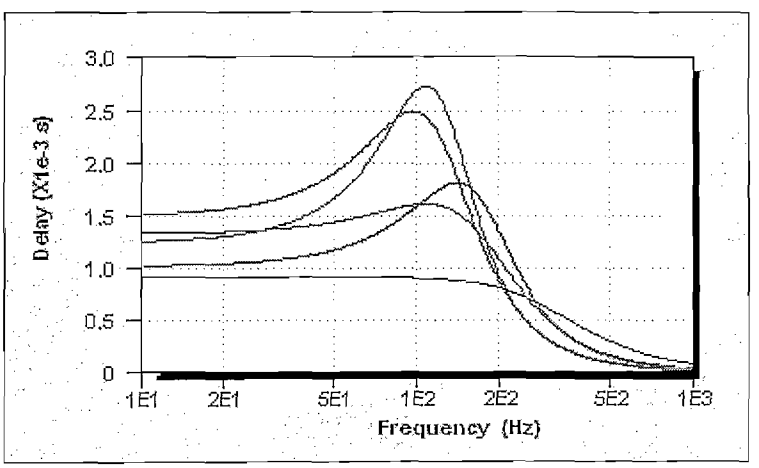


Figure 33: Delay Function Comparison of 5 Different Filter Approximations

The main reason for choosing the Chebychev approximation over the Elliptic approximation becomes clear from figure 33. At very low frequencies the Chebychev

(red) filter design tends to yield a better delay response than the Elliptic (purple) filter approach. For use in filtering a specific band in the process of acquiring an ECG signal, delays at low frequencies distorts the ECG signal. Remember that the entire bandwidth of the ECG signal is very narrow, and also lies at a very low frequency range, between 0.5Hz and 120Hz. Very little actual practical difference can be noted between the Chebychev (red) and Elliptic (purple) filter impulse responses as is depicted in figure 34. Also, as can be seen from figure 35, the pole-zero diagram shows that both the Chebychev and Elliptic filter approximations carry the same pole-zero construction.

As can also be seen from figures 36 and 37, the actual circuitry realizations (Twin-T network) of the two different filter realizations are exactly the same in terms of component count. Twin-T was chosen as an example because of its popularity. The same can be said for a KHN, Mikhael Bhattacharyya, Berka-Herpy, Akerberg-Mossberg and Fliege realization.

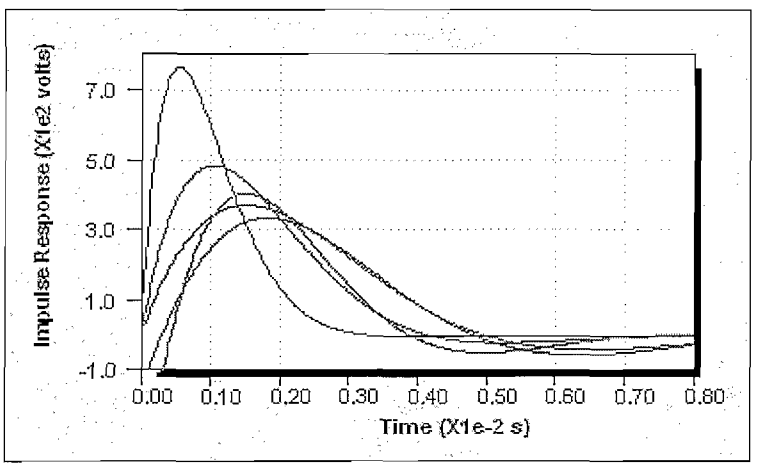


Figure 34: Impulse Response Comparison Between 5 Different Filter Approximations

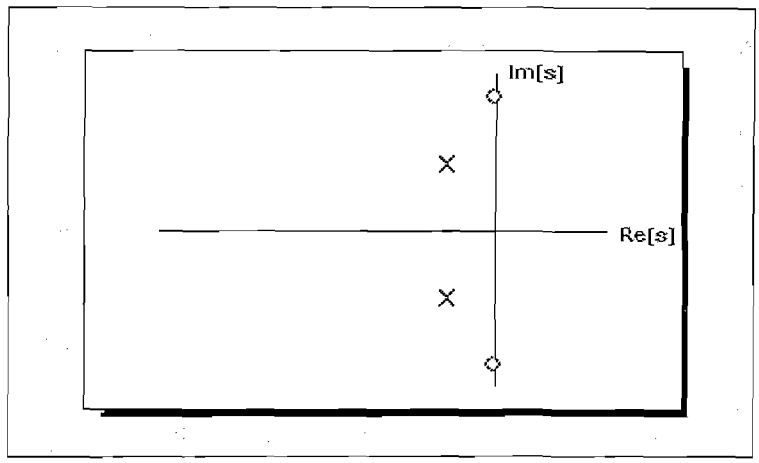


Figure 35: Pole-Zero Diagram of a Chebychev and Elliptic Filter Approximation

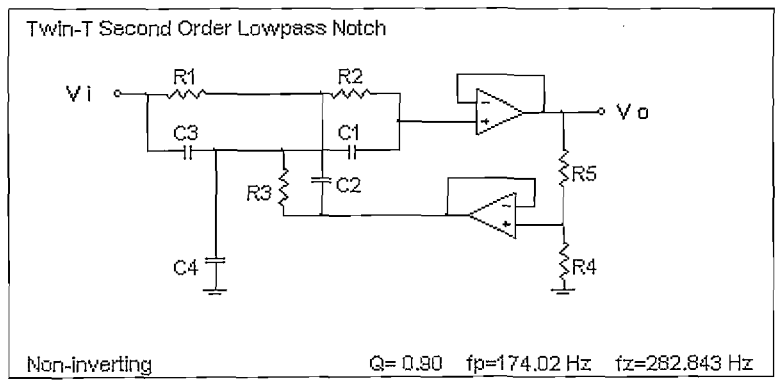


Figure 36: Twin-T Network Realization of the Specified Elliptic Filter

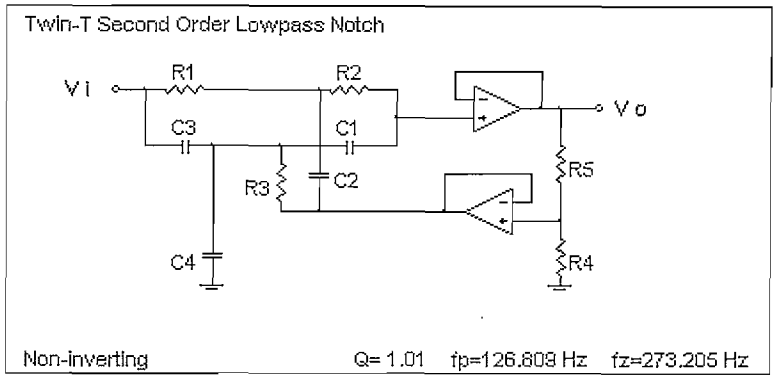


Figure 37: Twin-T Network Realization of the Specified Chebychev Filter

It may seem like an easier approach to implement a Butterworth filter because of the simplicity of its design. The main advantage of the Butterworth approach is that the loss of the filter is maximally flat at the origin. A flat pass-band is very good, however, although the Butterworth approximation shows a flat pass-band near the origin, it tends to get progressively poorer as ω approaches ω_p, where ω is the input frequency to the filter and ω_p is the pass-band frequency.[16] Moreover, the attenuation in the stop-band is worse than that of the Chebyshev approximation. The increased stop-band attenuation of the Chebyshev approach is achieved by actually changing the properties of the pass-band. As figure 26 depicts, this criteria is used to minimize the maximum deviation from the ideal flat characteristic.

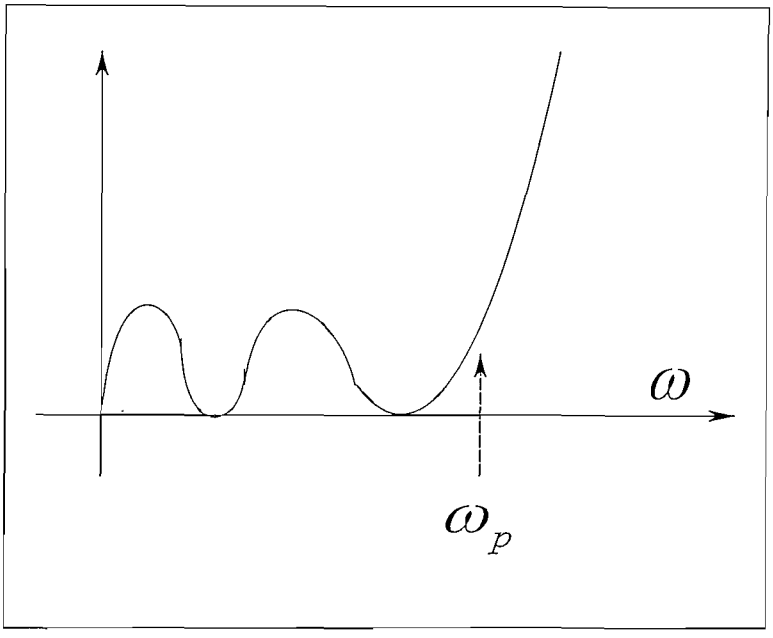


Figure 38: The Equiripple Pass-Band Characteristic of the Chebyshev Filter

The $n^{th} - order$ Chebyshev function $C_n(\Omega)$ can be defined as:[16]

$$C_n(\Omega) = \cos(n\cos^{-1}\Omega) \quad |\Omega| \leq 1$$
$$= \cosh(n\cosh^{-1}\Omega) \quad |\Omega| \succ 1$$

$$where\ \Omega\ is\ the\ normalized\ frequency$$

$$\Omega = \frac{\omega}{\omega_p}$$

The Chebyshev function can also be expressed as a polynomial in Ω as shown here:

$$C_{n+1}(\Omega)+C_{n-1}(\Omega)=\cos\left[(n+1)\cos^{-1}\Omega\right]+\cos\left[(n-1)\cos^{-1}\Omega\right] \quad \textbf{(1.15)}$$

using the identity:

$$\cos(A+B)+\cos(A-B)=2\cos A\cos B, \textit{yields}:$$

$$2\cos(\cos^{-1}\Omega)\cos(n\cos^{-1}\Omega)=2\Omega C_n(\Omega) \quad \textbf{(1.16)}$$

and this yields the recursive relationship:

$$C_{n+1}(\Omega)=2\Omega C_n(\Omega)-C_{n-1}(\Omega) \quad \textbf{(1.17)}$$

from the bottom of page 81,

$$C_0(\Omega)=1 \textit{ and } C_1(\Omega)=\Omega \quad \textbf{(1.18)}$$

is obtained.

As can be seen from the previous calculations it is now possible to obtain the higher order polynomials from the recursive relationships of these formulas. For example:[16]

$$C_2(\Omega)=2\Omega^2-1$$
$$C_3(\Omega)=4\Omega^3-3\Omega \textit{ etc.}$$

Let Σ be the pass-band ripple, Ωp be the pass-band cut-off frequency in rad/sec, A, be the stop-band attenuation parameter and Ωs be the stop-band cut-off frequency in rad/sec. The parameters Σ and A are related to parameters Rp and As

(the non-dB ripple and attenuation representations) respectively on the dB-scale and the relation is given by:[16]

$$\sum = (10^{\frac{Rp}{10}} - 1)^{\frac{1}{2}}, \qquad (1.19)$$

$$Also\ \Omega c = \Omega p \text{ and } \Omega r = \frac{\Omega s}{\Omega p}$$

The order N, of the Chebyshev filter is given by

$$g = \sqrt{\frac{A^2 - 1}{\sum^2}} \qquad (1.20)$$

$$N = \sqrt{\frac{\log\left(10\left(g + \sqrt{g^2 - 1}\right)\right)}{\log 10\left(\Omega r + \sqrt{\Omega r^2 - 1}\right)}}$$

One of the main objectives in considering an equi-ripple pass-band was to improve on the stop-band attenuation provided by the more simple Butterworth approximation.[16]

A short comparison between the pass-band of the Butterworth and the Chebyshev filters will explain. It is known that the attenuation of a Butterworth filter for $\omega \geq \omega_p$ (where ω_p is the pass band frequency) is approximately:

$$20\log_{10}\varepsilon\left(\frac{\omega}{\omega_p}\right)^n \qquad (1.21)$$

The Chebyshev attenuation is obtained from the low pass approximation of the filter's ***characteristics*** which is given as:[1][16]

$$\left|H(j\Omega)\right| = \frac{V_{IN}(j\omega)}{V_{OUT}(j\omega)} = \sqrt{1+\varepsilon^2 C_n{}^2(\Omega)} \qquad \textbf{(1.22)}$$

The parameter ε is defined by making use of the pass-band ripple $A_{\max}$.

$$\varepsilon = \sqrt{10^{0.1A_{max}} - 1} \qquad \textbf{(1.23)}$$

$A_{\max}$ is obtained by considering the loss of $H(j\Omega)$ at the pass-band edge frequency ω_p. Here the normalized frequency Ω is unity, and $C_n(1)=1$. Thus the pass-band ripple $A_{\max}$ must be:[1][16]

$$A_{\max} = 10\log_{10}(1+\varepsilon^2) \qquad \textbf{(1.24)}$$

The symbol ε, used in equation 1.24 is simply a definition for the amplitude of the ripple effect presented in the stop-band of a class II Chebychev filter.

Now, by looking at the low-pass approximation of the Chebyshev filter where for $\omega \gg \omega_p$ the term $\varepsilon C_n(\Omega) \gg 1$ the following can be obtained:[16]

$$A(\Omega)\big|_{\Omega\gg 1} \cong 20\log_{10}\varepsilon C_n(\Omega) \qquad (1.25)$$

We also know, from page 81 that for $\Omega \gg 1$,

$$C_n(\Omega) \cong 2^{n-1}\Omega^n \qquad (1.26)$$

and by making use of this expression, $A(\Omega)\big|_{\Omega\gg 1}$ reduces to:[16]

$$A(\Omega)\big|_{\Omega\gg 1} = A\left(\frac{\omega}{\omega_p}\right)\Big|_{\frac{\omega}{\omega_p}\gg 1} = 20\log_{10}\left[\varepsilon\left(\frac{\omega}{\omega_p}\right)^n 2^{n-1}\right] \qquad (1.27)$$

Considering the last three equations it can be seen that the Chebyshev filter approximation provides:[6][20]

$$20\log(2)^{n-1} = 6(n-1)dB \qquad (1.28)$$

***MORE* attenuation than a Butterworth filter of the same order.**

The second order Class II Chebyshev band-pass filter implemented in the design is depicted in figure 39. The reason for choosing the analogue technique for filtering the bandwidth of the ECG signal was purely because of the processing time

saved by making use of this analogue filtering technique. The micro processor is now free to handle a faster sampling rate which, as will be discussed later, keeps the design well within the limits of the Nyquist criteria for sampling an analogue signal.

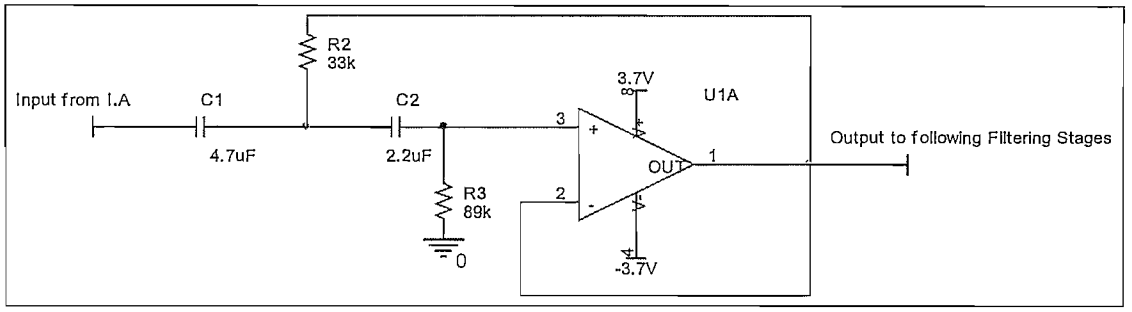


Figure 39: Class II Chebyshev 0.5Hz to 120Hz Band-Pass Filter

Figure 39 is a custom design for this specific application and forms part of the band select filter implemented on the ECG monitor. This circuit as part of the entire ECG monitor design including the values have been submitted as part of the patent application.

One might ask though, if better results in band-select filtering was achieved by improving on a Butterworth design by a Chebychev design, why is an Eliptic or Bessel filter not implemented to further improve on the Chebychev design. In order to gain a better understanding of the theoretical choices between the Butterworth, Chebychev and Eliptic approximations, let us consider a graphical representation of the responses of each.

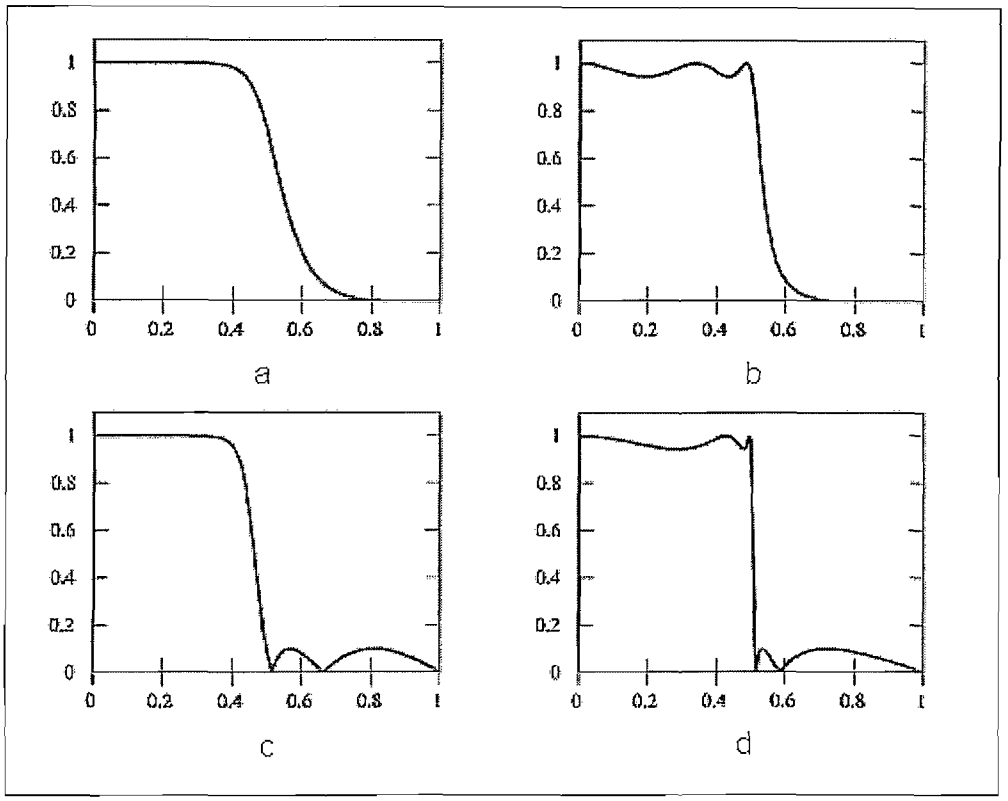


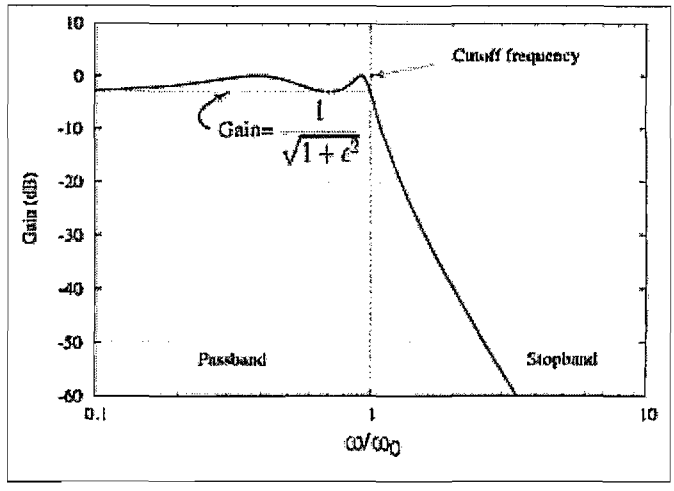
Figure 40: Analogue Filter Responses: (a) Butterworth, (b) Chebychev Class I, (c) Chebychev Class II, (d) Eliptic

Figure 40: All four filter responses were drawn (simulated) using a filter with the same number of coefficients.

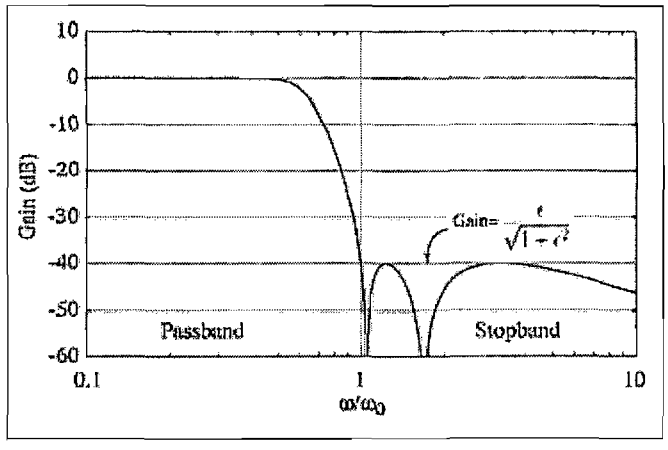
All aspects considered, it is clear from figure 40 that a much sharper response is delivered by a Chebychev filter overall than can be obtained by implementing a Butterworth filter. Put in practical terms, the same response obtained from a Butterworth filter can be obtained by making use of a smaller order Chebychev filter, which translates into less space required. Further more, it can be seen that the use of a class II Chebychev filter allows for much less or even no ripple in the pass-band, or band of interest. An in depth study of analogue filters will show that, the responses obtained from Chebychev filters are, in general, not as sharp as those obtainable by Elliptic filters of the same order, where of course, in practical terms the same ideology applies as for Butterworth and Chebychev filters. However, Elliptic filters, although

they are the most common approximations found in almost any analogue filter design, allows for much more ripple in the band of interest.[16]

An enlarged view of figures (c) and (d) in figure 40 depicted in figure 41 shows that a class II Chebychev filter, although it presents more ripple in the stop-band, presents a much sharper response with respect to the stop-band. The same logic will apply to the pass-band side of a class II Chebychev band-pass filter. Put more simply, a class II Chebychev filter de-attenuates and attenuates much faster than a class I Chebychev filter.



(a)



(b)

Figure 41: (a) Class I Chebychev Filter Response, (b) Class II Chebychev Filter Response

As the band of interest in the case of this application is so small, between 0.5Hz and 120Hz, much attention was given to finding a suitable midway solution that will allow for both sharp filter response and very little ripple in the pass-band. If filter response is poor, much of the band of interest will be lost due to unnecessary attenuation of wanted frequencies. In retrospect, if ripple is allowed in the band of interest, filtered data will be distorted. Because the bandwidth of the ECG signal is so

small, all frequency information is crucial, it simply is not feasible to allow for any unnecessary attenuation due to poor filter designs.

A further aspect of the analogue filtering technique used to be considered is the delay presented by almost any analogue filter.

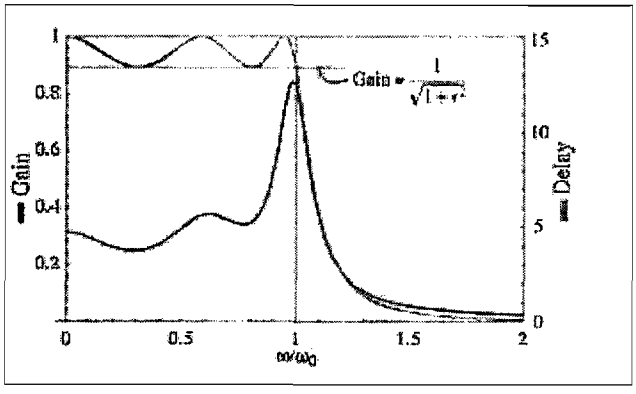


Figure 42: Typical Delay Presented by a Class I Chebychev Filter

Note that, from figure 42 it is possible to see that, the delay presented by a class I Chebychev filter is larger compared to that presented by a class II Chebychev filter as depicted in figure 43. Also, note that the ripple in the band of interest presented by a class I Chebychev filter is of significant larger amplitude than that depicted in figure 43, obtained from the output of a class II Chebychev filter.

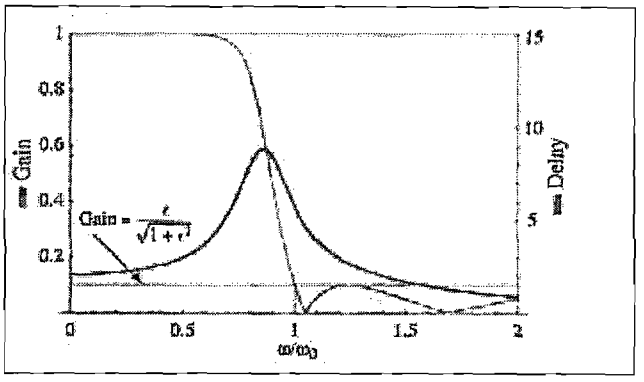


Figure 43: Typical Delay Presented by a Class II Chebychev Filter

Considering that the band of interest lies between 0.5Hz and 120Hz, the filter is designed to start passing frequencies from a frequency value slightly lower than 0.5Hz, so that at 0.5Hz, the least possible attenuation is still present. The same logic applies to the top end of the band. Thus, the little phase distortion that presents itself at the cross-over frequencies, as is graphically depicted in figure 43 (pass-band and stop-band frequencies) are of little influence to the actual band of interest or outcome of the filter.

It was also previously stated that, the family of class II Chebychev filters contains both poles and zeros and exhibits a monotonic behaviour in the band of interest as well as an equi-ripple behaviour in the stop-band, meaning that the zeros of this class of filters must lie on the imaginary axis in the s plane. Figures 44 and 45 were drawn with the aid of a digital oscilloscope capable of showing the poles and zeros of a filter. Both figures are a logarithmic representation of the gain of an 8^{th} order filter. Figure 44 represents the poles and zeros of a class I Chebychev filter and figure 45 that of a class II Chebychev filter.

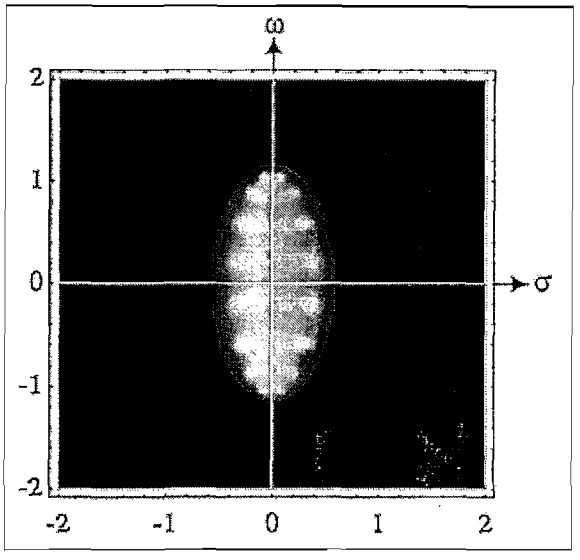


Figure 44: Digital Pole-Zero Representation of an 8th order class I Chebychev Filter

This graph was obtained making use of an 8th order class I Chebychev filter where, $s = \sigma + j\omega$, the stop-band ripple amplitude, ε, equal to 0.1 and the cut-off frequency, ω_0, equal to unity. The white spots are poles and they are arranged on the semi-axis. The poles obtained by the transfer function of this filter are those in the left hand plane of the depiction. The black areas on the graph correspond to a gain of 0.05dB or less, white corresponds to a gain of 20dB and more.

Please note: An 8th order filter was chosen for this demonstration simply because the graphical representation is much more spectacular and clear than that of a 2nd order filter for instance.

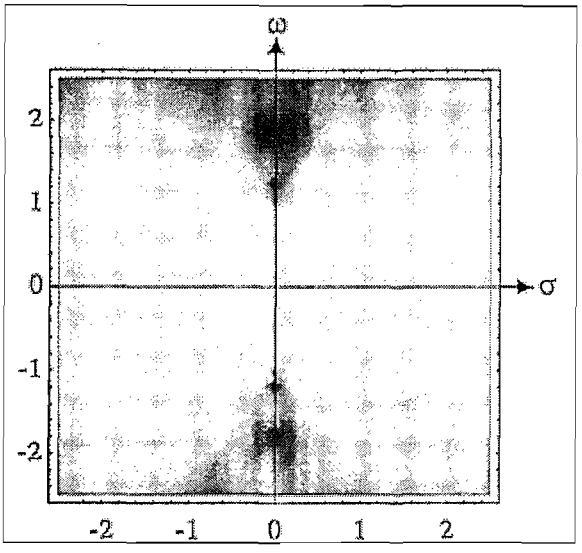


Figure 45: Digital Pole-Zero Representation of an 8th order class II Chebychev Filter

This graph was obtained making use of an 8th order class II Chebychev filter where, $s = \sigma + j\omega$, the stop-band ripple amplitude, ε, equal to 0.1 and the cut-off frequency, ω_0, also equal to unity. The white spots are poles and the black spots are zeros. All 16 poles can be seen. In the case of this Chebychev filter, all zeros have a multiplicity of two, thus 12 can be seen in the graph. The other four unfortunately lies outside the viewable area of the scope. Two on the positive ω-axis and two on the negative ω-axis. The poles of the transfer function are those on the left hand plane. The zeros of the transfer function are the zeros shown, but with a multiplicity of only one. Again, the black areas correspond to a gain of 0.01dB or less and the white areas correspond to a gain of 3dB or more.

For a better understanding of the origin of poles and zeros of analogue filters refer to any good textbook on the topic as is referenced in the references at the end of this dissertation.

Available space for construction of the entire circuit, ripple effects and delay functions were the dominant features when a choice was made to implement the

Chebychev filter. The best answer was the class II Chebychev filter with it's equi-ripple in the pass-band, and relatively sharp attenuation filter responses.

3. Common Mode Driver Assistance

- Selecting the ECG Bandwidth -

Aid in Selecting the ECG Band of Interest

To further aid in the process of extracting a good and clean ECG (as noiseless as possible) from the human body, the implementation of a common mode driver was thought to be necessary. The operational amplifier used in the common mode feedback circuit of the ECG monitor is a variation of the OP97 from ANALOG DEVICES. This op amp is a low power, high precision operational amplifier with high common mode rejection, in the order of 114dB.

The circuit basically applies an inverted copy of the common mode interference in the system to the subjects' body with the aim of cancelling the interference. As was described in the section covering the dedicated I.A design, common mode, the noise in the system appearing on both input lines to the I.A is dissipated across the external gain resistor of the I.A, R_g. A balanced copy of this common mode is fed into the inverting input of the op amp driving the common mode driver circuit and amplified roughly 90 times. The reason for an amplification of 90 is purely empirical. It is thought that this value should at least be more than the amplification applied to the incoming differential signals of the I.A itself. The output of the common mode driver is an amplified, inverted copy of the common mode on the human body. By feeding back this amplified inverted copy of the common mode to the body, the common mode itself is cancelled even before the differential signals enter the I.A.

The process of the common mode driver is a complex one to understand and tends to let one think in circles. Refer to appendix F for an in detailed technical description of the so called DRL approach for cancelling common mode.

Common mode is constructed of white noise. White noise is common mode appearing all over the frequency spectrum. In short practical terms, if the I.A senses some common mode on the two input lines, this common mode is dissipated across the external gain resistor. This piece of common mode representation at that instance is a good example of the common mode at any other instance. (Because white noise tends to have the same properties at any instance in time.[1][6][15][16] Thus, the common mode driver is actually feeding back an inverted copy of common mode which already passed the system, but the cross-correlation effects of all common mode is very high and this technique tends to suppress common mode in general. In short, the cross-correlation of the inverted common mode copy taken one instance back in time, with that present in the system one instance forward in time is so much that the two tend to cancel each other out.

No specific design theory exists for this technique, and as such, this technique also forms part of the patent application. For more specific details refer to the patent application presented in appendix E.

Further more, the common mode driver, which is basically in inverting amplifier, has a roll-off and a low-pass cut-off at about 160Mhz, the latter was build in for stability reasons. Whenever very high frequencies are present on the inputs of any active components, the components tend to become unstable and start to oscillate. This is a fundamentally important fact taught in almost any basic electronic course. These stability parameters are usually given in the datasheets of the components. For this reason the roll-off and cut-off at about 160MHz of the common mode driver. As such, high frequencies are not amplified and put back onto the human body to be sensed by the inputs of the I.A.

The value of 160MHz was chosen, as common mode outside the band of interest is already stopped by the band-select filter as discussed in the previous section with the aid of the capacitor network which precedes the I.A in the final design. As can be seen in figure 20, a capacitor network has been added in front of the I.A. This network has one goal in mind: To stop any frequencies above 530.5Hz from even entering the I.A, by filtering them at the input of the I.A. The value of 530.5Hz is of no significance except that, (i), the used I.A specifications indicates that it will become unstable when amplifying frequency content higher than 1MHz, and (ii), the capacitor values chosen were done with practical consideration. These values are easily obtainable and they are available in the component packaging sizes used to populate the final ECG monitor. The band limitation of the capacitor values together with the two $250k\Omega$ resistors, as depicted in figure 20 simply calculates to a value of 530.5Hz. The calculations of these values are shown in equation 1.38 in the section covering the evaluation of the filtering processes.

Why the $250k\Omega$ one might ask. These two resistors have one further goal in mind. According to medical specification, no current higher than $100\mu A$ may flow through a humans body due to external component application.[10][12][17], Considering that the front-end of the ECG monitor is power by a 3.7V battery, of which the voltage can only drop with time, the use of a $250k\Omega$ restricts the current flowing between any two electrodes to well below $100\mu A$ in case of any malfunction of the equipment.

Referring back to figure 20, the construction of the common mode driver can be seen in the bottom right hand corner as part of the front end design, functioning in parallel with the I.A design.

The gain of 90 which is applied to the common mode voltage retrieved from the I.A is calculated as follows:[1][6]

$$\frac{R_4}{R_2 \parallel R_3} = \frac{1M\Omega}{11k\Omega} \qquad (1.29)$$

and the cut-off frequency of 160MHz was calculated as follows from figure 20:

$$f_{-3dB} = \frac{1}{2\pi \times (10k\Omega * 0.1\mu F)} \qquad (1.30)$$

4. Applying appropriate amplification

– *Preparing the Signal for Digitization*-

Amplification before Digitization

As the amplification of an analogue signal is nothing new and not a focus area of this research, only a short explanation of why it was necessary to amplify the band-passed analogue ECG signal before it is digitized will be given.

Keep in mind that, when a signal is digitized, the actual voltage value of the analogue signal is compared to a reference voltage level connected to the ADC and then quantized into one of 2^B bit levels by the ADC circuitry itself. The value of which might differ from process to process, depending on the word length (amount of bits the ADC are able to quantize) of the ADC. When the reference voltage is very large compared to the incoming analogue signal, accuracy becomes a problem, for obvious

reasons. Quantization of signals with relatively small amplitudes, referenced against signals having large amplitudes, does not leave room to assign more bit-space (more accurate values) to the smaller signals low values. Mathematically it can be torn down as follows. If the referencing voltage value is 5V for example and a 10-bit linear ADC is used then the maximum value that can be represented is 5V and it will digitally be represented by a value of 1024 ($2^{10}=1024$). Let us now sample a signal with a maximum peak-to-peak value of 5V against this reference voltage. Having a 5V signal as input will yield a digital value of 1024. Having a 0V signal as input will yield a digital value of 0. Now, consider a 5V signal as reference and an incoming analogue signal with values between 1 and 5mV. In this case having *either* a 1 or 5mV signal as input will yield a digital value of 0 as output. The minimum quantization value of a B-bit linear system is $\frac{V_{fs}}{2^B-1}\approx\frac{V_{fs}}{2^B}$ [6][15], which yields a minimum quantization value of 4.88mV for a 10-bit ADC using a reference voltage of 5V.

Remembering that the systems operates from a 3.7V supply, including the microcontroller housing the ADC, amplification of the raw band-filtered ECG signal to levels acceptable by the ADC was necessary in order to obtain a better quantization factor. The fact that the ADC is houses inside the microcontroller means that the ADC uses the same supply voltage as the microcontroller as a reference voltage. Keeping this is mind and using the formulas given in the previous paragraph it is easy to calculate that the minimum voltage to be quantized by the ADC will be 3.6mV. Because the peak-to-peak voltage values of the ECG lies between 0.1 and 5mV as was stated and discussed on page 76, this minimum value of 3.6mV was not sufficient for correct ECG monitor operation. Amplification had to be designed so that the analogue signal to be digitized, would have a peak-to-peak value of 1V guaranteeing the accuracy of the digital values produced by the ADC. Amplifying the original ECG signal from between 0.1 and 5mV by a factor 100 results in values lying between 10 and 500mV. This in turn results in the total ECG signal having peak-to-peak values of roughly 1V. It is now relatively easy to see that the minimum quantization

specifications in order to obtain accurate values from the ADC being supplied by a 3.7V source are met with ease.

5. Entering the Second Filtering Process

- *Eliminating Network Interference* -

Band-Stopping Network Interference

Network interference consists of 50 or 60Hz pickup and harmonics, which, can be modelled as sinusoids. Characteristics, which might need to be varied in a model of power line noise, include the amplitude and frequency content of the signal. The amplitude can vary up to 50 percent of the peak-to-peak value of the ECG amplitude[17], while the frequency also tends to drift ever so slightly within 4% upward or downward from 50Hz or 60Hz (between 48Hz and 52Hz or between 58Hz and 62Hz)[19][21].

The latter is dependant on the grade or quality of power delivered by a power company. Figure 46 on the next page depicts how a power signal affects the ECG signal.

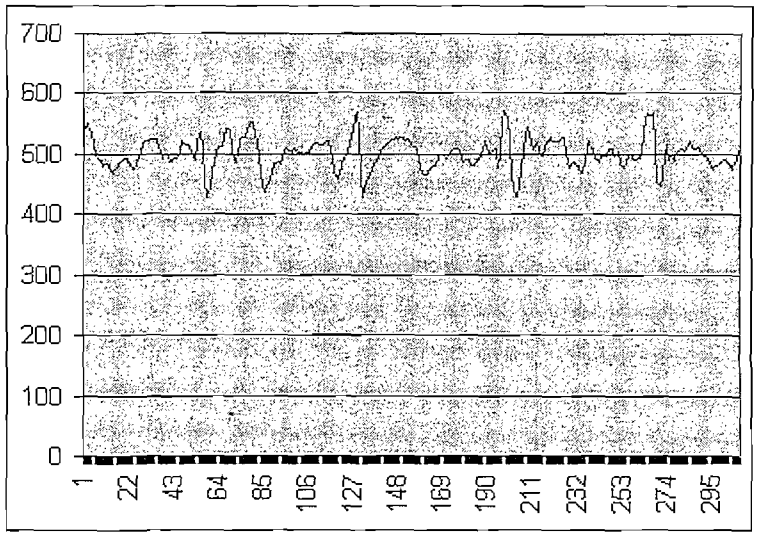


Figure 46: An ECG signal severely affected by Network Interference

Figure 46 is a crystal clear example of an ECG signal severely influenced by 50Hz pickup and/or the correlating harmonics. The depicted example was acquired with the ECG and heart rate monitor operating directly under a fluorescent tube without any network interference filters. It is clear when examining two different signals separately, that the 50Hz signal is unwontedly added to the signal of interest. Study figures 47, 48 and 49. In figure 47 a 100Hz sinusoidal signal is shown. Figure 48 shows a clean 50Hz sinusoidal wave, typical of a single phase power network delivering $230V$ for everyday use.

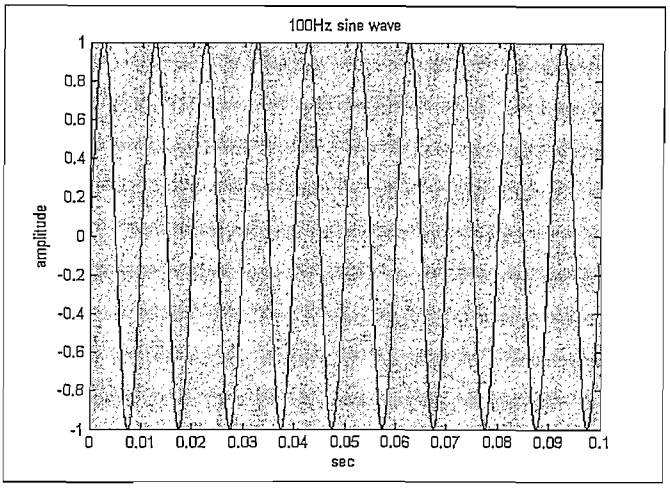


Figure 47: 100Hz Sinusoid

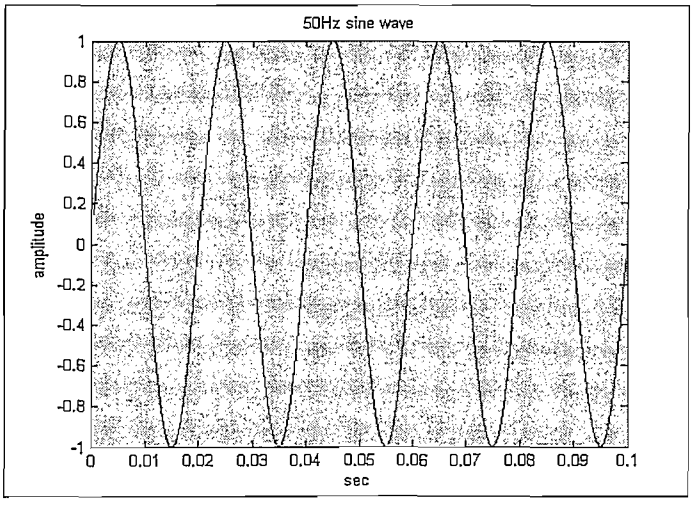


Figure 48: 50Hz Sinusoid

In the next figure (figure 49) it can be seen what the severe effects are of contaminating for example, a 100Hz sinusoidal data wave with an unwanted 50Hz sinusoidal signal.

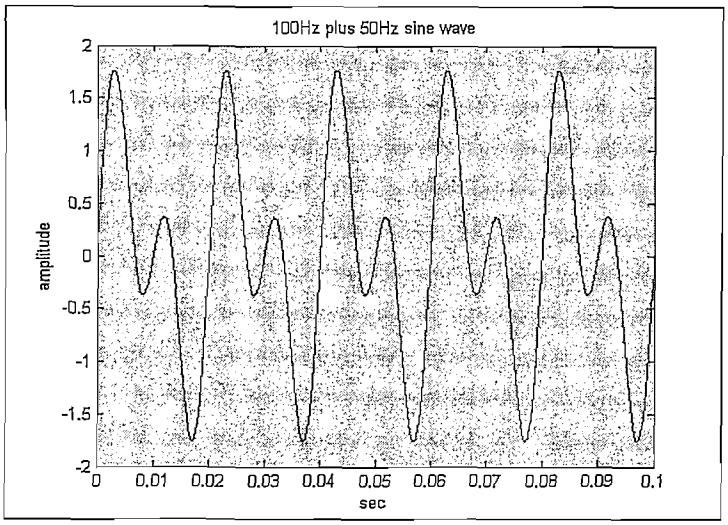


Figure 49: 100Hz Sinusoid contaminated by a 50Hz sinusoid

It is easy to see that not only the amplitude information but also the phase information of the original 100Hz sinusoid are contaminated by the insertion of a 50Hz pickup. But a data signal affected by purely 50 or 60Hz, can be dealt with in one way or another. A more profound issue arises when a data signal is corrupted by not only the network interference but also harmonics of the primary interfering signal. Figure 49 shows the effects of a 100Hz signal contaminated not only by 50Hz but also for example, by the fifth harmonic of 50Hz.

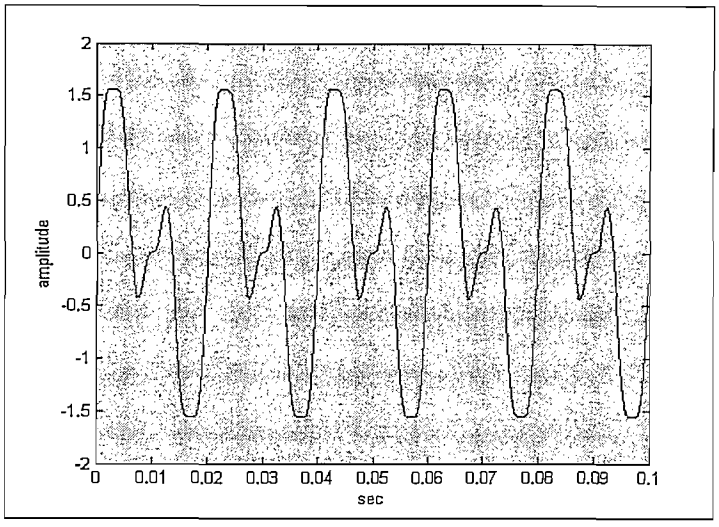


Figure 50: 100Hz sinusoid contaminated by 50Hz and the fifth harmonic of 50Hz

It can be seen from the centre, top and bottom of figure 50 that not only the amplitude of the original 100Hz signal is affected but a severe contamination of the phase information of the signal is present. But still this is not the end of the contamination. Theoretically it is known that when a harmonic of any kind is present in a signal, usually the harmonic itself also is not in phase with the original interfering signal.[1][6][16][21] Thus depicted in figure 51 on the next page is a 100Hz data signal contaminated by a 50Hz interfering signal. Added to that is the fifth harmonic of the 50Hz interfering signal but shifted by one fifth of the harmonics phase, in other words the harmonic itself is shifted in phase by its own harmonic number.[21] The calculations leading too these assumptions are shown on the next page:

A simple 50Hz sine wave can be presented by[1]:

$$\omega(t) = \sin\left[(2\pi f)t\right], with\ f = 50Hz \quad \textbf{(1.31)}$$

Any particular harmonic of the signal can be presented by[6]:

$$\omega(t) = \left(\frac{1}{h}\right)\sin\left[(2\pi f)t * h\right], \quad \textbf{(1.32)}$$
$$with\ f = 50Hz\ and\ h = (any\ harmonic)$$

Theoretically the phase shift of the harmonic can be presented by[1][6][21]:

$$\omega(t) = \left(\frac{1}{h}\right)\sin\left[(2\pi f)t * h + \left(\frac{2\pi f}{h}\right)\right], \quad \textbf{(1.33)}$$
$$with\ f = 50Hz\ and\ h = (any\ harmonic)$$

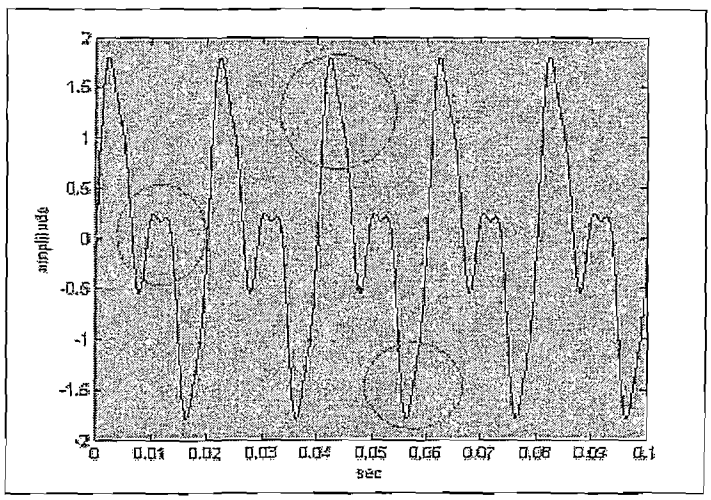


Figure 51: 100Hz signal contaminated by 50Hz and a phase shifted fifth harmonic

It can be seen from figure 51 that a further contamination and loss of information is immanent when the harmonic frequency is in itself shifted in phase from its parent frequency. By comparing figure 50 and 51 it is important to notice that the

phase at the top of the signal as well as in the middle and bottom of the signal is further defected by the addition of a complex contamination signal.

5.1 Choosing the Correct Filter - *Eliminating Network Interference* –

Network Interference, Filter Selection

Filtering any signal to rid it from the ever so present 50Hz or 60Hz pickup is a recursive task to be done again and again in almost every single project designed by an engineer or technician.

As mentioned earlier, in part II, covering the interlocking of different filtering techniques, making use of the power of both analogue and digital filtering techniques is crucial to the successful outcome of the ECG monitor. We already know by now that by filtering all the different types of noise in only one of the two domains, analogue or digital, will be problematic in very different ways and each one will present its own shortcomings. An all analogue filtering process will bring forth a very large design which will stretch beyond the practical space and packaging limits while an all digital filtering approach will bring forth time and processing issues which will result in not meeting the sampling requirements. (Refer back to section 7 of part II, covering the design of the front-end.) For these reasons and the flexibility to reasonably easily manipulate software filters a digital filter was implemented to rid the ECG signal of 50Hz network interference. (This also makes it easy to change the filter values when using the ECG monitor in an area where 60Hz in stead of 50Hz network interference is experienced.)

The digital filter was implemented in the software running on the microcontroller onboard the ECG monitor and was developed in low level C. In order to make use of the digital filter, the analogue signal exiting the Chebyshev band-pass filter of the previous stage had to be digitized. This was achieved by making use of the 10-bit onboard ADC of the microcontroller. (The microcontroller used in the application is a

PIC18F252 from Microchip.) Of course the necessary DC correction, amplification and voltage supply corrections as discussed in sections 3 and 4 earlier is already applied to the raw band-limited ECG signal before digitization.

After 5 different prototypes built and tested over a two year period a digital filter for ridding the ECG signal from network interference seemed the most practical way to go. Empirical testing showed the necessity for a 400^{th} order notch filter at least, to acceptably filter network interference out of the wanted signal. Implementing a 400^{th} order filter in the analogue domain will simply, from practical considerations, proof to be a task no engineer will ever take on. This solution will take up too much space and the original specification of light weight and small package will be defied. After careful consideration it was decided to cascade two 200^{th} order FIR notch filters in software, each with a notch width of 10Hz. It was calculated (taking into consideration the clock cycle speed of the microcontroller) that enough time would be available to digitize the signal and mathematically manipulate the signal to rid it of network interference. One might ask, remembering that the previous discussion of this problem; How is the signal correctly digitized by a microcontroller running from a single supply while the analogue filter output of the previous stage, selecting the ECG bandwidth, swings around $0V$? The solution to this problem will be discussed after the next section dealing with the digital signal processing of the ECG signal to rid it of network interference.

One further aspect to keep in mind is this; The bandwidth of the ECG lies between 0.5 and 120Hz. This is a very small area to operate in. Ridding this signal from network interference presenting itself around 48 to 52Hz or 68 to 62Hz calls for a very delicate procedure in order to prevent loosing too much of the information around this band. The latter will result in an even further destructed ECG signal simply because of information loss.

The last remaining issue is the actual digital process used to filter the network interference from the digitized ECG signal.

It was already discussed, in this section, that a 2 cascaded 200th order FIR notch filters was implemented to do the job. It is now time to have a closer look at the design of this filter before concluding part III of this dissertation, the design documentation covering all the filtering aspects of the ECG and heart rate monitor, with a short look at the encoding of the final digital processed ECG signal to ready it for RF transmission and the impact the encoding and RF transmission have on the digitization and digital filtering of the ECG signal.

Figure 52 depicts a typical visual representation of a digital filter.

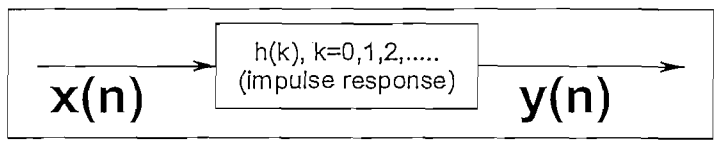


Figure 52: Conceptual Representation of a Digital Filter

The input and output signals of a FIR digital filter are related by the convolution sum as given in the next equation[15].

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k) \qquad (1.34)$$

It is evident from this equation that the impulse response of a FIR filter is of finite duration, since $h(k)$ for the FIR filter has only N values. An alternate representation for a FIR filter in the z-plane is given as follows[15]:

$$H(z) = \sum_{k=0}^{N-1} h(k)z^{-k} \qquad (1.35)$$

The FIR filter used in this application was developed based on a sampling frequency of 250Hz. Roughly double the bandwidth of the ECG signal and by doing so complying to the Nyquist criteria.

To understand why the Nyquist criteria should be complied to when digitizing an analogue signal, it is necessary to study the principles of digital signal processing (DSP). As an extensive study of digital signal processing falls outside the scope of this study but still is an integral part of the project to achieve the purpose of this research a short discussion and explanation of the most important aspects of digital signal processing and analogue to digital conversion processes will be presented here.

The following graphical representations of a normal ECG are presented both in the time and frequency domain to show the actual result of the FIR filter implemented in the design. The data used to simulate the design was constructed by two Dutch students and the simulation results are also based on filter software written by them. (In both depictions an excessive amount of 60Hz network noise was added and then removed by the FIR filters.) The reason for 60Hz in the simulations is purely based on the background of the two Dutch students.

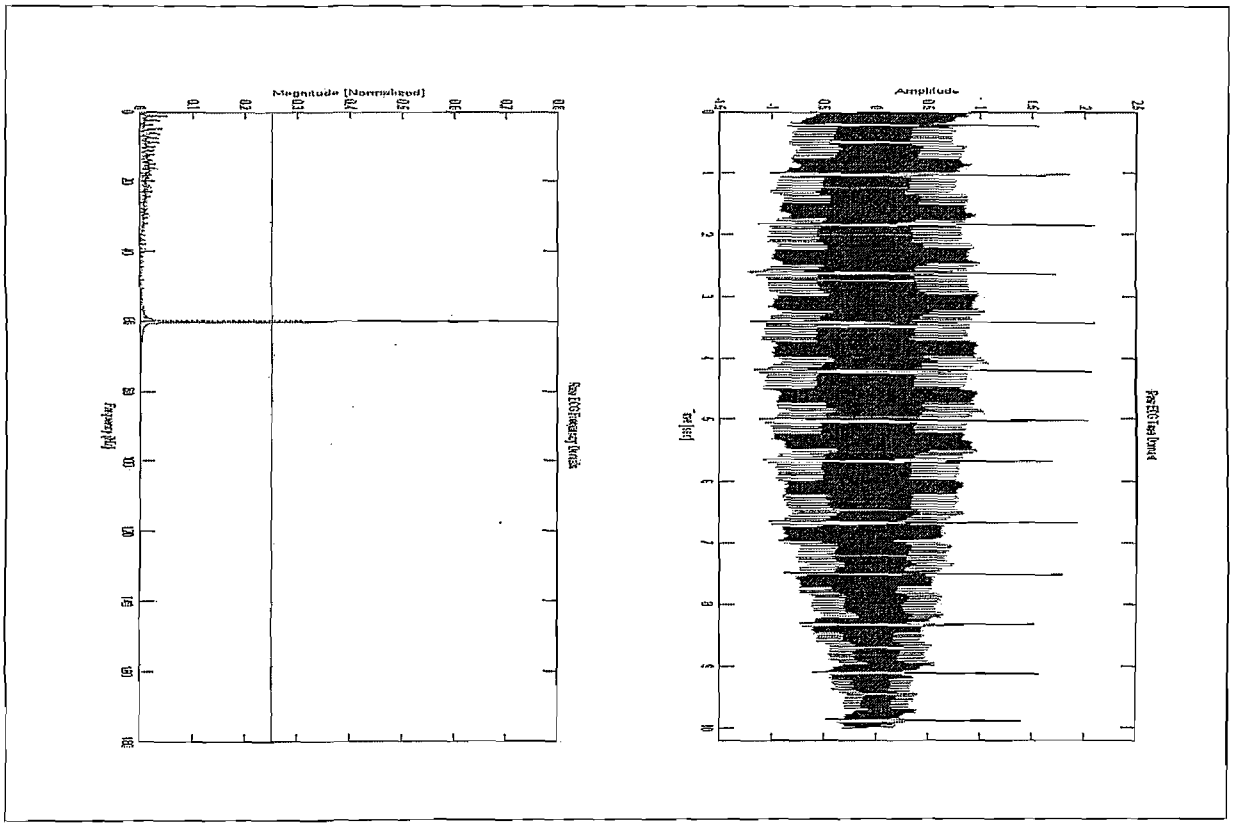


Figure 53: Raw ECG signal in time domain vs. Frequency domain

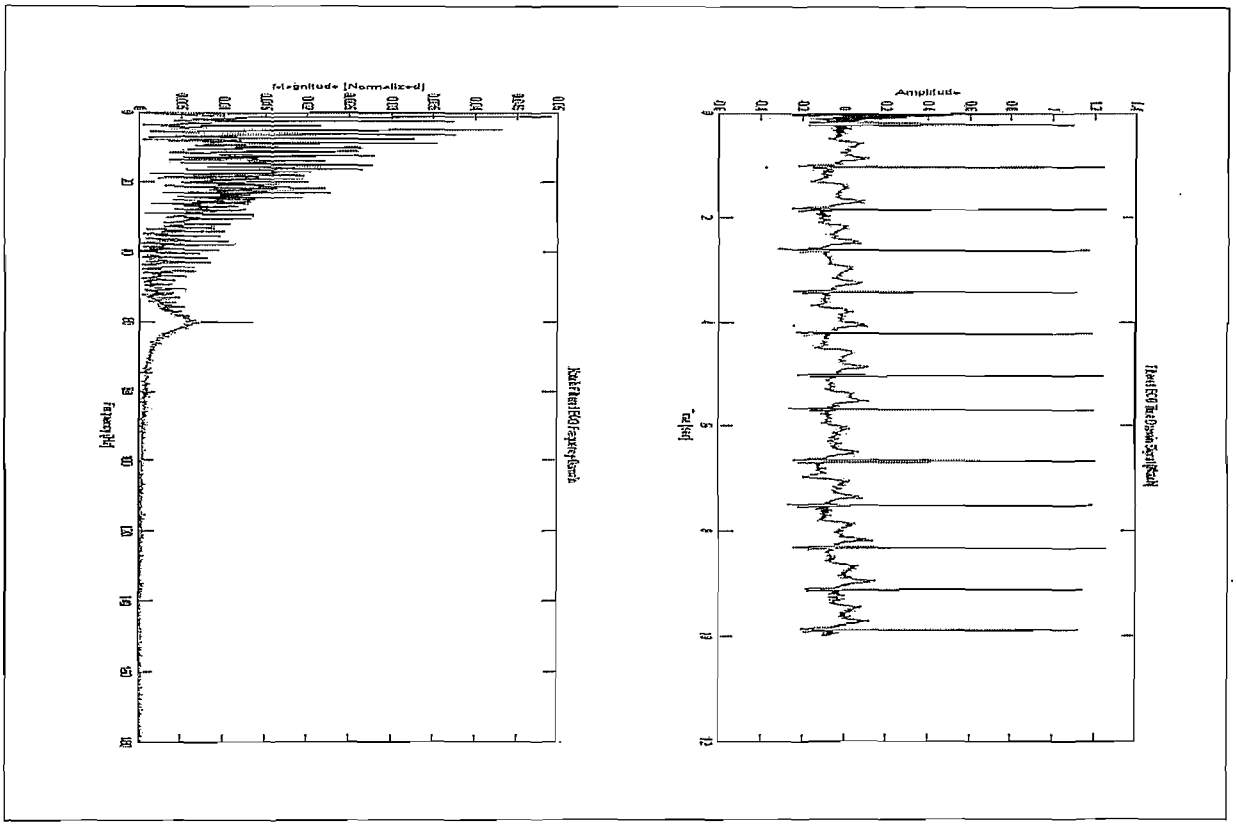


Figure 54: Notch Filtered ECG signal in time domain vs. Frequency domain

5.1.1 Understanding the Principles of the ADC process

Analogue-to-Digital Principles

It seems logical that, before any DSP algorithm can be performed, the signal must be in a digital form. Most signals in nature are in analogue form, as is the ECG studied in this project, necessitating an ADC process, which usually involves the following steps:[15] (As was done with the converted ECG signal before filtered for bandwidth, network and the other interferences described.)

- The signal is first sampled, converting the analogue signal into a discrete time continuous amplitude signal.
- The amplitude of each signal sample is quantized into one of 2^B levels, where B is the number of bits used to represent a sample in the ADC.
- Discrete amplitude levels are represented or encoded into distinct binary words. The length of the words is B bits.

Before continuing it seems necessary to provide the characteristics of both the analogue and digital signals.

An analogue input signal; A signal continuous both in time and amplitude.[15]

A sampled signal; A signal continuous in amplitude but defined only at discrete intervals. *Samples at time* $t = nT$.[15]

A digital signal; x(n) for n = 0,1,2,... This is a signal consisting at discrete points in time and at each time point can have only one of 2^B values. This is the signal of interest when filtering in the digital domain.[15]

Refer to appendix D for an introductory background on basic DSP fundamentals which will aid in understanding some of the terms and explanations in the next few sections.

Basic DSP fundamentals state why it is necessary to sample any analogue signal at a rate of at least two times the maximum frequency component present in the signal. In simple terms, this must be done in order to re-gain all of the information locked up in the original analogue signal after the digitization process.

One small detail, integrated in between the analogue part of the circuit and the digitization process remains unexplained. How was it possible to sample a signal coming from the output of an analogue filter and amplification stage running on a dual voltage supply with a microcontroller running on a single voltage supply? In other

words, how does the sampling process of a signal swinging *around* $0V$ as reference, with a microcontroller and ADC running from a single $0V$ to $+3.7V$ supply work?

Refer to figure 20. Here it can be seen that the system was developed with a dual voltage supply (±3.7V). The reason for this might not be so obvious. Normally it should be relatively easy to design an I.A circuit to run from a single voltage supply. Most I.A packages contain a reference pin which can be used to reference the I.C to any virtual plane, as was explained in part II, the design of the front-end. The more difficult issue to overcome was the design of the band-pass filter following the I.A. From basic electronic design concepts, the design of a Class II Chebyshev band-pass filter calls for a dual voltage supply. It also seemed logical to introduce $0V$ as the common point throughout the system in order to keep noise to a minimum level. If $0V$ was to be chosen as the common point, a dual supply at the front-end was a given in order to extract the full ECG signal. The effect of this decision was that the I.A was referenced with respect to $0V$ as discussed earlier and, that the band-pass filtering stage as well as the analogue amplification stage, runs from a dual voltage supply. The use of a single battery on the system due to weight and packaging constraints called for the implementation of a voltage inverter to be able to generate the negative voltage necessary for the dual supply. The inverter was chosen so that the frequency of operation was well beyond any bandwidth specifications of the ECG system in order for the band-pass filter to be able to filter out any noise or interference generated by the oscillation of the dc voltage inverter together with all the other noise filtered by this filter.

This brings forward the solution to the sampling issue at hand. After the filtered ECG signal exits the amplification stage of the analogue circuit it is fed through a series capacitor which acts as a dc filter, removing any unwanted dc levels added for whatever reasons throughout the analogue process. The next step was to lift this dc filtered ECG signal back up to half the voltage supply of the microcontroller in order to allow the microcontroller to be able to digitize the ECG signal correctly without any clipping or loss of signal information. By now it is known that, the maximum peak-to-

peak voltage value of the ECG signal will be 1V as this was determined by the analogue amplification stage before dc filtering. This means that the minimum and maximum voltage value seen by the analogue to digital conversion process will be $\frac{3.7V}{2}=1.85V$, this is half the supply voltage, minus and plus 1V which falls within the voltage supply specifications of the microcontroller. In other words 0.85V, and 2.85V respectively. Since the microcontroller makes use of a 10-bit ADC, in digital terms this 1.85V correlates to ± 512 or 513. (Remember that the maximum value to be quantized by a 10-bit ADC will be 1024.) The minimum and maximum digital representations of the ECG signal will never (in digital terms) extend beyond $\frac{0.85V\times1024}{3.7V}=235$ on the lower end and $\frac{2.85V\times1024}{3.7V}=789$ on the high end respectively.

The way the dc voltage level was added to the dc filtered signal was simply by adding two resistors of equal value to the circuit. In other words, a simple voltage divider was constructed around the incoming ECG signal after the series capacitor, and before the signal is digitized. One resistor was pulled to 3.7V and the other one to 0V. This adds half the supply voltage (as this is a simple voltage divider) to the incoming ECG signal and finalizes the ECG signal for digitization.

6. A Final Review

Design Review

Before continuing a visual representation of the entire electronic (analogue part) circuit will be presented as it was developed for monitoring the ECG signal. This includes the I.A, common mode driver, Class II Chebyshev band-pass filter, analogue amplifier / filter, dc filtering components as well as the dc level correction circuitry developed by which the raw ECG signal is processed before it is digitized, filtered for network interference in the digital domain, encoded for RF transmission and transmitted away from the ECG monitor. Figure 46 depicts this ***front-end*** circuitry for the ECG monitor.

It can be seen from figure 55 that the raw ECG signal is acquired from the human body by means of three electrodes, two of which is connected to the I.A through two $250k\Omega$ resistors and a third which is connected to the output of the common mode driver.

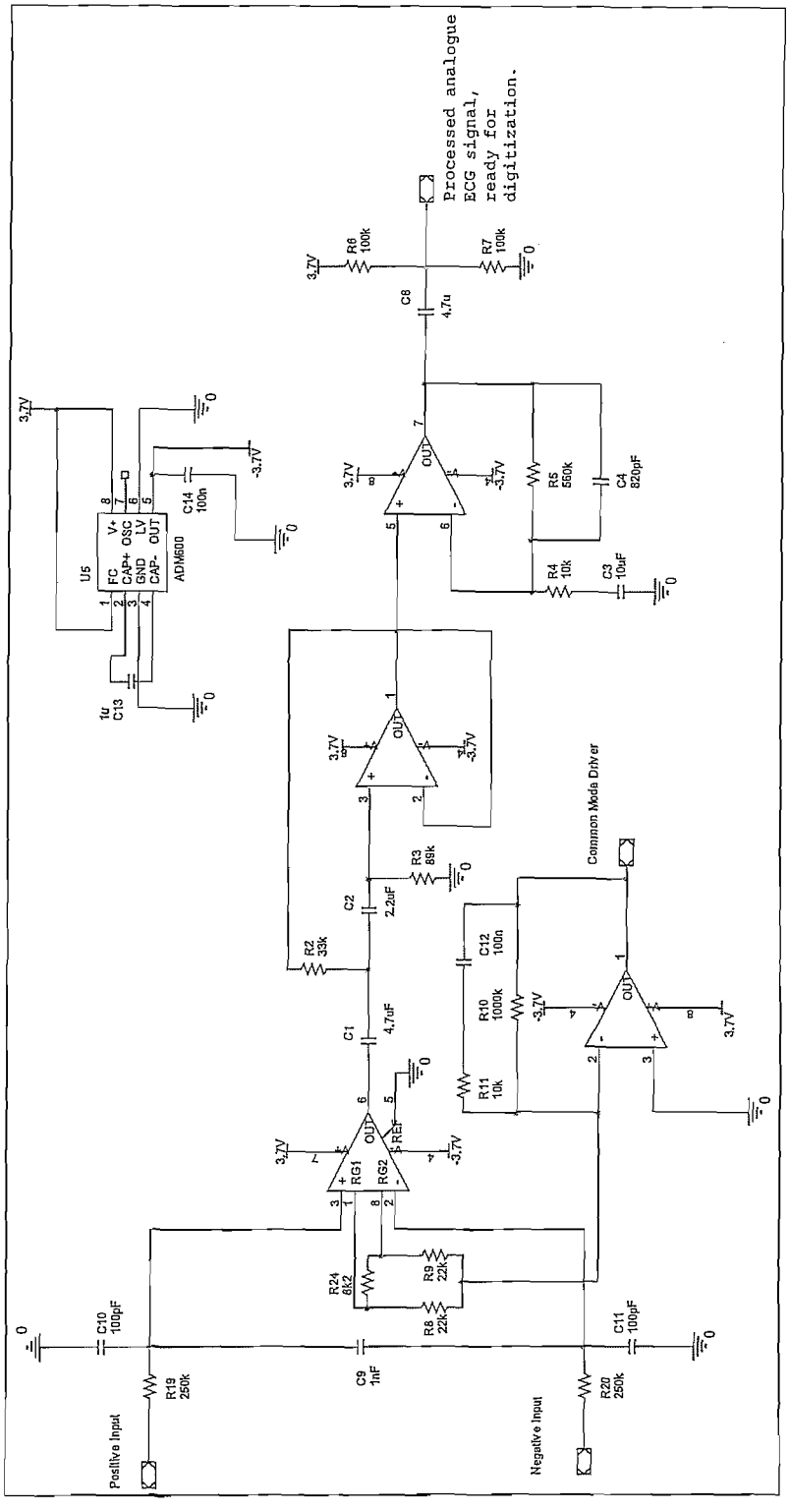


Figure 55: Final *front-end* ECG Acquisition Circuitry.

After the raw ECG signal is acquired by the I.A it is immediately band-passed by the second order Class II Chebyshev filter consisting of a single operational amplifier and assisted by C1, C2, R2 and R3. (Refer to figure 50 and the last part of the discussion on the ECG band selection for information on the assistance of capacitors C1 and C2 with the filtering process.) Immediately after band-pass filtering, the signal is amplified by the analogue amplifier consisting of a single operational amplifier assisted by R4, R5, and C3.

Non-inverting amplifier designs usually are very straight forward. The reason for this peculiar amplifier design is a simple one, yet it proposes a very elegant solution to a design problem in this particular ECG application. The band-pass filter is a non-inverting filter and thus the amplifier also had to be constructed in a non-inverting fashion because there is no further analogue circuitry and thus no further chance to again correct the signal if an inverting amplifier was used. (Basic electronics teaches that inverting amplifiers are much easier to design than their non-inverting counter parts.) A $820pF$ capacitor, C4 can be seen in figure 46 as part of the analogue amplifier design. This is not usually part of an amplifier design but was inserted in the circuitry to further attenuate all frequencies above 130Hz in the analogue signal even more before digitization.

This capacitor plays an important role in helping with the high-end cut-off frequency of the ECG signal. The operation of the capacitor in the circuit is quite simple. As can be seen the capacitor is in the feedback line of the output of the operational amplifier to the inverted input. The higher the output frequencies become, the more this capacitor tends to become a short circuit and, thus stop these frequencies from being passed and amplified.[6]

This specific design idea, the cut-off capacitor in the feedback loop of the amplification stage, was also incorporated as one of the key design features making the ECG monitor operate correctly under extreme conditions and as such formed part of the patent application documentation.

At the output of the amplifier a series capacitor can be seen C8, which dc-filters the ECG signal as discussed in section 7 of part II. Following the series capacitor, C8, two resistors R6 and R7 can be seen. It is these two resistors which acts as the voltage divider adding the correct amount of dc back into to the ECG signal thus pulling the entire signal up to swing around one half of the supply voltage of the microcontroller.

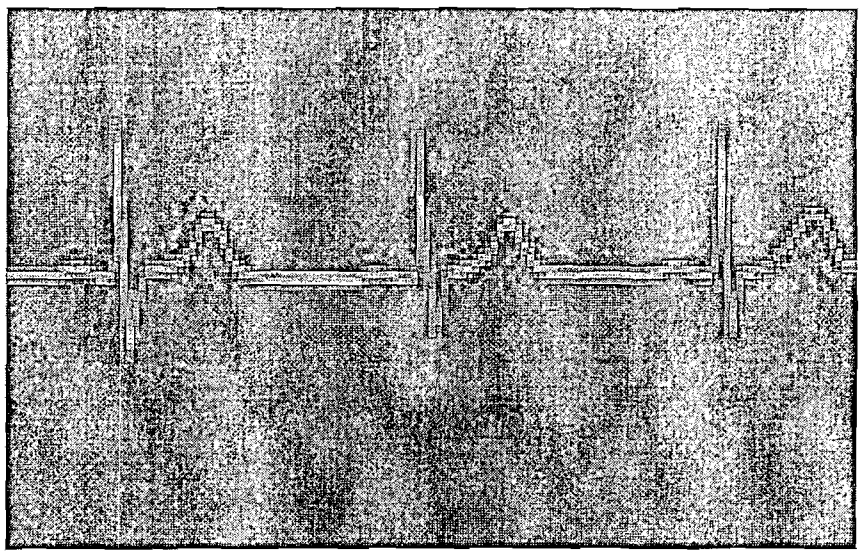
So far the design including the advantages and disadvantages of each one of the segments of the front-end of the ECG monitor has been discussed. This part of the monitor basically consists of an I.A, a few analogue filters, amplifiers and common mode rejection circuitry. This circuitry is the heart of the ECG monitor and this delicate acquisition and filtering design formed the heart of the research for this dissertation. As such it also contributed to 50% of the patent application as can be seen in appendix E.

The design of a very small, extremely accurate, portable ECG monitor running from a single battery at $3.7V$, with a very light weight has been accomplished. All of the weight and packaging considerations have been taken into account and the result is the circuitry depicted in figure 46 on page 118.

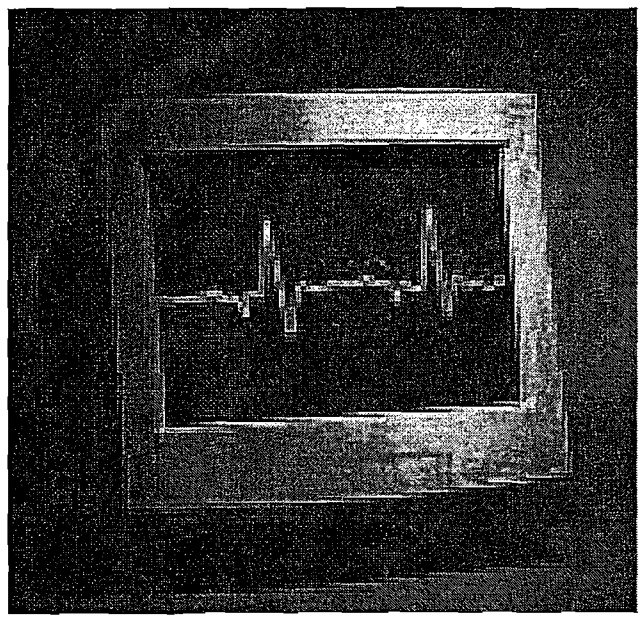
The construction of a very small, delicate analogue front-end to the ECG monitor has also been accomplished. This was possible, simply because almost one half of the filtering necessary is done in the digital domain, leaving room to have designed very small physical circuitry.

The raw ECG signal is acquired from the body by making use of a specifically designed I.A with the help of a common mode driver, as explained earlier, band-passed to extract the correct band of interest, amplified-filtered, dc-filtered and dc-corrected for digitization by the designed circuitry.

At this point it is possible to actually look at a perfect output of the entire circuitry on a pc or laptop. If neither one of these are available, the output can even be shown on a digital oscilloscope. The following two figures depict typical outputs of the circuitry.



(a)



(b)

Figure 56: (a)/(b) Typical Analogue Output of the ECG pattern before Digitization.

ECG Acquisition Support

1. Additional Designs Influencing the ECG Monitor

Monitor Performance –*additional influences*-

A few issues remain. The dc voltage inverter and the encoding process of the digitized ECG signal to prepare it for RF transmission. Both these components implemented onboard the ECG and Heart rate monitor (the voltage inverter as a hardware components as described earlier and the encoding procedure as a software process) will influence the performance of the monitor.

1.1 DC voltage Inverter

Inverter Operating Frequency & Noise

Depicted in the top right hand corner of figure 46 is an I.C with two capacitors connected to it. This is the dc voltage inverter used on the ECG and heart rate monitor. Remember that a single battery was implemented and that a dual voltage supply was necessary to design the I.A and the band-pass filter. (Refer back to part II, covering the design of the I.A). This dc voltage inverter was used to invert the voltage supply from the battery ($3.7V$) to $-3.7V$ in order to supply the I.A and the operational amplifier used the band-pass filter, as well as the amplification stage following the latter. These inverters are easy to come by, of the shelf components. The only issue to take into consideration when selecting one is the frequency of operation as most of these components make use of a switching architecture to invert the dc voltage[6][8]. To understand why the operation of a voltage inverter is dependant on a *frequency of operation* refer to any good text book covering the basics in *switching power supply electronics,* as this topic stretches beyond the scope of this dissertation.

As described in part III of this dissertation, the frequency of operation of the voltage inverter was selected after considering the operating frequency of the RF

transmitter onboard the ECG monitor as well as taking into consideration the ECG band of interest.

Selecting a voltage inverter operating at a frequency within the ECG band of interest will lead to additional noise-data at that specific frequency inside the band of interest. Taking into consideration the small bandwidth of the ECG signal, if this noise (frequency band) has to be filtered out, much of the information, about the ECG signal itself, locked up at that specific frequency in the ECG signal will also be lost. With this is mind, considerations about analogue or digital filtering techniques for ridding the signal of the inverter noise was not even investigated as the operating frequency of the inverter strictly could not be allowed inside the ECG band of interest.

The second consideration was the inverter interference with the RF components onboard the ECG and heart rate monitor. The carrier frequency of the RF modules onboard the monitor is 433.92MHz. With this in mind a few simple RF calculation allows for the extraction of the different intermediate frequencies (IF's) implemented on the RF module. (Refer to a good text book, eg. Paul H. Young, 2004, Electronic Communication Techniques, Fifth Edition, covering the basic topics of RF modulation and Frequency synthesizing for an in depth explanation on IF.) The IF of the specific RF module used for this application with a carrier frequency of 433.92MHz is 80kHz. With this in mind the operating frequency of the voltage inverter was chosen to be 147kHz. As can now easily be seen, it was possible to choose an operating frequency for the voltage inverter which does not interfere with the carrier frequency of the RF modules. Also, the IF is safe from interference because any noise at 147kHz is already filtered by the onboard analogue filters implemented on the ECG monitor. Most voltage inverters are available in a range of different inverting operating frequencies.

1.2 Coding of Digital ECG Data Before RF Transmission

RF Coding Considerations

nother issue needing attention is the process of encoding the digitized ECG data to prepare it for RF transmission. The reason for encoding data before transmitting the data points falls outside the scope of this dissertation but, for the sake of clarity a short explanation will be given as the encoding process greatly influences the processing time available on the microcontroller. As was previously discussed, processing time is the one big factor determining if the theoretical sampling rate as discussed in part III will be achieved.

When transmitting data over an RF channel a few critical issues need attention. First, the data rate at which transmission takes place is very important. Secondly a process called *bit synchronisation* needs to take place at the receiver end in order to correctly extract the transmitted data bits from the analogue RF signal. To assist the bit synchronisation process it is recommended that data transmitted be encoded so that every separate bit package transmitted contains an equal amount of '0's and '1's. In more practical terms, this means that an equal amount of frequency modulations (upward and downward from the carrier frequency) should take place for every transmission burst. This prohibits the RF system from having transmission bursts containing long strings of '0's or '1's in a row, or in other words transmitting at a single frequency continuously.

The process of preparing or correcting the data stream to be transmitted to have equal amounts of '0's and '1's is called encoding. To be more specific, the Manchester encoding technique was used in this application. (Manchester encoding is but one of many available encoding schemes used in telecommunication systems.) This process takes place in software after the digital filter for ridding the ECG signal from network interference has been applied to the data. Each byte of digital data representing a digitized point (quantized value) on the ECG signal is encoded and transmitted over the RF channel.

This process takes up a considerable amount of time. Again, also remember that the digital filter applied to the incoming digitized data takes up some processing time. The result is that the amount of time available to the microcontroller for sampling the incoming analogue ECG signal is limited. In order to free up more time for the microcontroller to maintain the necessary sampling rate as discussed in section 7 of part III, it is necessary to increase the transmission rate of data after filtering and encoding, as this is the only place where processing time can be regained in the digital domain (in software). But, here as everywhere else in electronic design, a limit is to be reached.

It can be calculated that a transmission rate of 57600Bps is necessary to keep sampling the incoming analogue ECG signal at the desired sampling rate as was discussed on pages 106 through 114 in part III. This transmission rate will also leave enough time available for digitally filtering the digitized ECG signal, encoding the separate data bytes and transmitting them away continuously without loosing information. The calculation was done as follows:

Each data byte transmitted by the RF transceiver contains 10 bits, 8 data bits plus one start and one stop bit. Transmitting 10 bits at 57600kBps would result in a transmission time per byte as follows:

$$\frac{1}{57600Bps} \times 10bits = 173.61\mu s/byte \quad (1.37)$$

This means that to be able to sample the incoming analogue ECG signal at a rate of at least 240Hz, (twice as fast as the maximum frequency component of approximately 120Hz in the ECG signal) the signal needs to be sampled at a rate of:

$$\frac{1}{240Hz} = 4166.66\mu s$$

Meaning that the incoming raw analogue ECG signal needs to be sampled every once $4166.66\mu s$

$173.61\mu s$ are already lost every time a data point is transmitted, as can be seen from equation 1.37 on the previous page. Further more, to set up or align the transmitter and receiver with each other, 25bytes of 0xAA, two bytes 0xFF, two bytes 0x00, one byte 0xCC, one byte 0x33 and one byte 0x55 needs to be send over the RF channel before a data point can be transmitted. The 25 bytes 0xAA aligns the receivers bit slicer with the incoming data stream, the two bytes 0xFF and 0x00 aligns and clears the UART on the receiving ends microcontroller and the three bytes 0xCC, 0x33 and 0x55 are the crucial RF header bytes to indicate a start of data to the software on the receiving end of the system. (Refer to appendix C, as well as any good text book covering RF transmission for an in depth explanation of the latter.)

The total time lost for each one of these transmission are:

$$\left[\frac{1}{57600Bps} \times 10bits\right] \times (25+4+3)bytes = 5555.55\mu s$$

It is clear that not enough time is available to, even *only* transmit and sample, as the sampling process itself takes about $6\mu s$ per sample. (This sampling time is a given for sampling a 10-bit value from the datasheet of the PIC18F252 datasheet.)

The solution to this problem did not come as easy as was expected. As this was a crucial element to correct it needed urgent attention. The success of the entire system boils down to the ability to sample and transmit an ECG signal in real time. The solution came at a very late stage in the development of the system after numerous testing opportunities and will be discussed in the next section on the evaluation of the system.

* Technical detail on components to be found on the CD in the back cover

2. External Components Influencing the ECG Monitor

Monitor Performance –*additional influences*-

Now that the design of the ECG and heart rate monitor in itself is complete and in depth discussion about the construction and design decisions have been given the time has come to look at the output of the system.

Unfortunately, as was discussed in the late sections of part I, the ECG monitor can not operate as a stand alone unit. Though it is possible to view the output of the ECG monitor as a single unit, the outcome of the project as a whole, calls for a fully functional, real-time-*remote* ECG and heart rate monitor. This imposes the need for a few subsystem designs in order to operate the ECG monitor as a functional system.

For the clarity of this discussion, refer to the last few pages of the patent application documents in Appendix E as well as figure 4 on page 16 in part I. These sketches give a very accurate indication of the setup of the system as an entity.

The additional subsystems and special items designed as support systems to the ECG monitor are listed below:

1. Data Relay Units
2. Hand Held Computing Unit
3. High Level Analysis Software
4. ECG-Electrode Leads
5. ECG Watertight Electrodes

These subsystems did not form part of the original research but, during continuous testing it became all the more apparent that certain critical areas of the *idea* needed more attention in order to make the system function according to original specification of: *Real-Time-Remote ECG & Heart Rate Monitor.*

2.1 RF Data Relay Units

Direct, Real Time RF transmission data loss

As was discussed in part I of this dissertation, the one advantage of a real-time remote ECG and heart rate monitor should be that, the data acquired from the athletes must be available continuously during a sporting event.

Initial tests of the ECG monitor, simply transmitting to a receiver connected to a PC next to a sporting field yielded considerable pleasing results. Information was transmitted from a single person walking around on the field to almost anywhere around the field. Of course, steel and concrete structures on such a field must be taken into consideration, but this is a minor issue. Data was received from the monitor at the requested rate with a minor transmission loss of a few data packets every time the subject turned his back on the receiving unit. This, in part, is a result of the so called line-of-sight issue in RF systems as was discussed in the later sections of part I.

Early on in the implementation of the ECG monitor after a single test during a practise session of a North West University Rugby Institute rugby team, it was realised that the communication between the ECG monitor on the player and the PC next to the field could not be a direct one. Too often the player turns his back on the receiving end of the system, and data was lost. This could be expected as rugby is a sport in which a player runs and participates in movements in any one of many directions.

The solution to this problem came when a set of data relay units was designed and integrated as part of the entire system. *Refer to the DVD accompanying this dissertation for a video on the operation of the entire system, including the data relay units.*

The idea of integrating data relay units into the system brought with it one major issue to be overcome in order to re-establish even the most basic of communications. However, the solution to this problem brought forward a system with a communication system so redundant, constant communication can almost be assured. (This is a very delicate statement, made in hindsight of the fact that there is no such thing as constant RF communication assurance.)

The idea of an RF data relay unit included at least a microcontroller and an RF transceiver module. This would mean that communication from the PC or hand-held computing unit next to the field could be established to the RF data relay units, and from there the request, data or information could be relayed to the ECG monitor on the field. Having four of these relay units around the field would implicitly bring forth the situation where, no matter in which direction the athlete wearing the ECG monitor is facing (assuming that the relay units can be placed in a rectangle format around any sporting field), the ECG monitor will always be in direct line of sight with any two RF data relay units. This solved the line-of-sight problem and with it the data loss issue. However, if the receiving unit next to the field, whether it is a PC or the hand-held computing unit, the RF data relay units and the ECG monitor on the field all operate on the same frequency, RF crosstalk will most certainly bring forth the destruction and

loss of any RF communication on the field. Also, how does the receiving unit or hand-held computing unit *know* which one of the RF data relay units are in line-of-sight with the ECG monitor in order to send a request to that specific relay unit.

After considerable time spent on finding an idea for solving this problem, the following solution proved, not only to solve the issue at hand, but also brought with it some advantages. Each one of the RF data relay units have been given a digital I.D. Assume that the I.D's of the four relay units are A, B, C and D. A request destined for a specific ECG monitor is always transmitted to relay unit A first. This relay unit will then acknowledge the receipt of the request to the transmitting PC or hand-held unit. If an acknowledgement is not received, the request will be transmitted to relay unit B, and so on. The unit that receives the request will in turn pass the request on to the ECG monitor which will acknowledge the receipt thereof. The same logic applies here, if the acknowledgement is not received, which ever relay unit tried to establish a connection will pass the request on to the next relay unit in line. This relay unit will try to establish the connection and retrieve the data from the ECG monitor. This loop will continue until one of the relay units establishes a connection, retrieves the data and transmits it back to the requesting PC of hand-held unit next to the field. It is important to understand that, once the request for data has been acknowledged by any one of the data relay units, the process is disconnected from the PC or hand-held unit and is solely a function of the data relay units. The PC or hand-held unit only takes over the communication loop management once an answer is received from any one of the data relay units.

Now, the issue of crosstalk still needs attention and with it, the advantage brought forward by this solution. To rid the system of the fatal crosstalk issue discussed earlier, it was necessary to implement not only one, but two different RF frequencies for usage between the PC or hand-held unit, the RF data relay units and the ECG monitor. A frequency of 433.92MHz was implemented between the PC or hand-held computing unit and the RF data relay units. From here the requests to the ECG monitor is transmitted on a carrier of 173.225MHz. This meant that the RF data relay units received two different transceiver units, one at each RF frequency. The

uncalled advantage brought forward by this design is constant communication. The PC or hand-held unit can now, for instance send a second request out to the data relay units, retrieve data from there or cancel a current operation while the other ECG monitor communication establishment between the RF relay units and the ECG monitors on a different request is in progress. By the end of the RF data relay units, each one housed two microcontrollers, one handling communication to and from each RF transceiver, the two RF transceivers and two different antennas, one for each transceiver. These RF data relay units are powered from a 12V battery which can be recharged when flat. They are mounted on poles and placed on the four corners, or in a rectangular pattern around a sporting field. They can also be mounted on the walls of a gym for instance.

2.2 The Hand-Held Computing Unit

Direct, Easy Access, Data availability

Incorporating a microcontroller for all control purposes, an alpha numeric, membrane switch technology keypad, a liquid crystal display unit and an RF transceiver, the hand-held computing unit was designed as an ease of access, portable data viewing instrument.

It is not always desirable or even convenient to have a PC set up next to the sporting field. For whatever reasons, it might be more comfortable to have a small packaged, easy to handle, lightweight instrument where data retrieved from the ECG monitor can be handled, viewed and stored. This unit is called the hand-held computing unit and can be carried in the hands of the coach or sport scientists next to the field. The idea also immediately makes the unit fully portable, meaning that the person viewing the data is not restricted to the area where the PC is set up.

Though this unit has its advantages, it comes with one big disadvantage. Information analysis on this unit is not possible. During the beginning phases of the

design of the hand-held unit it was thought that a liquid crystal graphical display could be used in this unit. This would have made it possible to actually display the incoming digitized ECG on the display as it is sent away from the ECG monitor on the field. However, the time-based electronic specifications of this type of display make it very slow. According to the datasheets supplied by the manufacturers of these types of displays, the time needed for the microcontroller to update, refresh and flush the display unit with new data is longer than the time available in between transmitted sampled ECG data points received by the hand-held unit. In practical terms, it should be simple to understand that, if all of the relayed data from the ECG monitor is not collected by the PC or hand-held unit, a distorted or inaccurate representation of the ECG signal will be obtained. For this reason it is only possible to view the heart rate of the athlete on the hand-held unit, and not the ECG signal itself. (A simple calculation on the part of the ECG monitor or hand-held unit software allows for extracting the heart rate from the ECG monitor.) As such, whenever the hand-held unit is used as the primary data collection unit, the ECG data itself will not be available. The heart rates are however being stored in onboard eeprom for later download to higher level software running on a PC for analysis.

Both the hand-held computing unit and the high level software running on a PC are able to indicate when the heart rate of an athlete shows discrepancies when compared to previous similar conditions. From the high level software it will also be possible for the sport scientists to see when discrepancies in the ECG of an athlete present itself. *It is in this where the true value of the system lies. Being able to predict when an athlete is over-performing or is on the verge or collapsing due to stress of the heart.*

The RF transmission systems onboard all the units are designed to be able to reach a maximum distance of 600m. This ensures that all the components making up the system will be able to reach all around a sporting field. Meaning that for instance, the hand-held unit may be carried all around the field and even up onto a pavilion and still be able to communicate to and from the RF data relay units.

2.3 Analysis Software

Analysing the data

An integral part of any analysis project, is the actual output of the system. This output contains the analysed data or, at least presents the data in such a fashion so as to empower the user to analyse the data. This might include graphical representation of data, sorted values or even data logged in a database according to certain specifications.

Because the high level analysis software accompanying this real-time remote ECG monitoring system forms part of another study and was not developed as part of this research an in detail discussion of it will not be presented here. However, because it forms part of the supporting subsystems of the ECG monitoring equipment a DVD with a video illustrating the output and functionalities of the software has been included at the end of this dissertation. Refer to appendix G for the DVD.

2.4 Electrode Leads

Special Wiring

During the first testing opportunities three comfortably long pieces of cut wire were used to connect the ECG electrodes fixed to the human body to the ECG and heart rate monitor. The outcome of these tests indicated that a certain amount of unaccounted noise was appearing on the ECG signal. Figure 48 on the next page is a representation of the output. It was soon discovered that when the ECG electrode leads are kept still, at least with respect to the body, the noise disappears. Once the leads are allowed to move, the noise is back.

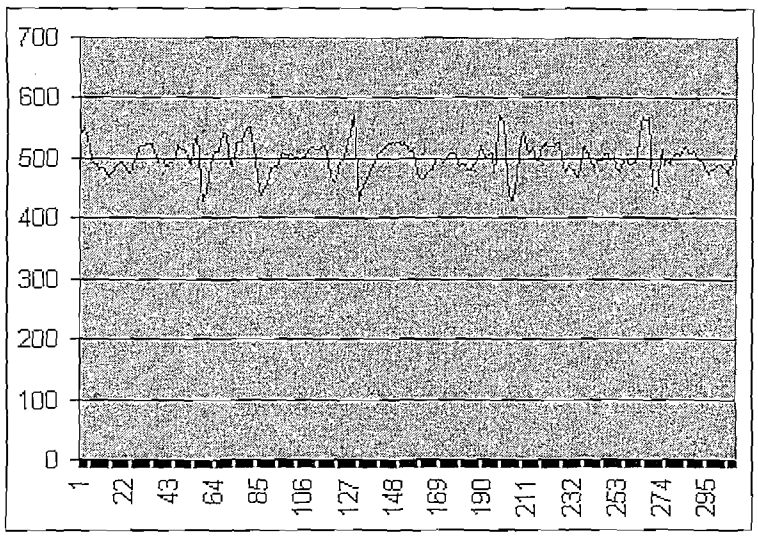


Figure 57: Unaccounted Noise Appearing on Sampled ECG Output

Refer back to part III of this dissertation. The noise in the graphical representation above seems to be a combination of network interference as well as motion artefact. What is more, the sample taken over roughly 300 points which correlates to 1.25 seconds worth of sampled ECG, contains noise which does not seem to be constant.

It was thought that a very soft wire can be used to serve as the leads between the ECG electrodes and the monitor. It was suggested by experts in the field, that a very special soft wire used in the military environment might help in reducing the noise by reducing movement of the wire itself. This solution later proved the suggestions false.

After numerous testing and different wires tested the results indicated that some attention should be given to a special packaging method to house the ECG leads. The packaging should keep the wires in position with respect to the electrodes and the monitor itself. Having the wires moulded into an epoxy or polyurethane rubber solution together with the monitor might be the best solution. This is still an ongoing

study as the final packaging of the ECG monitor was still underway by the completion of the research for this dissertation.

Another method for reducing external interference linking onto the ECG leads might be to integrate a wire shielding driver onto the ECG and heart rate monitor. This solution will call for the use of shielded electrode leads. The inner core will be used to transfer the actual ECG signal from the ECG electrodes to the monitor and the outer shielding will be used to stop external disturbances from disrupting the signals in the inner core. This technique should also greatly improve the performance of the ECG monitor in areas where high levels of network interference is experienced as this interference coupling method is mainly a combination of capacitive and inductive methods[1][6]. Having a shield around the inner core at a different constant potential with respect to the outside of the leads should prove to stop coupling of noise to the inner core. This technique was not implemented in the design and is discussed under the section covering possible improvements in part V on page 163 of this dissertation.

2.4 Special ECG Electrodes

Watertight ECG Electrodes

Numerous tests showed that the use of standard of the shelf ECG electrodes will not withstand the high specifications for this system to deliver the accuracy expected of it. One of the major differences between this development and the other heart rate monitors available, as was discussed in part I of this dissertation is the fact that this development makes use of the actual ECG signal. Not only to calculate the heart rate but also to reconstruct a graphical representation of the ECG acquired from an athlete in real time.

As was also briefly discussed in the late sections of part II on page 70, the movement between muscles and bone causes a disturbance of the ECG signal called motion artefact. In the same way movement between the ECG electrodes and the skin

causes motion artefact, but on a different level. Because the ECG electrodes and the conducting gel used between the electrodes and the skin does have some form of resistance, some impedance can be measured between the skin and the electrode. For the sake of this argument, the value of this impedance is not important. If the electrodes are to be moved around on the skin, the impedance measured between the two changes. This in turn forms a voltage divider with the input of the I.A to which the two ECG electrode leads are connected. If this input voltage keeps on changing, the dc levels (reference plane) of the input signal shifts around, which in turn, causes noise to be generated and injected into the signal at the front-end. This is one of the dominant reasons why electrodes able to stick to the body are used and simple re-usable conducting metal plates covered in conducting gel are not implemented. (The conducting gel used with ECG electrodes and with normal ECG monitors consists of a mixture of silver (Ag) and Silver-Chloride (AgCl) assisting the conductance of electrical signals from the skin.)

Tests showed that the normal ECG electrodes available at the local drug store and in hospitals are not suited to withstand the amounts of perspiration of athletes during sporting activities. This is acceptable seeing that these electrodes are used for short periods of time, and where they are used for longer periods of time, the patient is sleeping, under operation or in hospital in bed.

As stated in the last paragraph, the normal ECG electrodes proved to loosen from the skin surface with excessive amounts of perspiration. A company by the name of *Bio-Detek* in New York was contacted with the request to manufacture a special electrode with specific watertight specifications. The electrode sizes, shapes and watertight duration were specified and the result after testing these electrodes was an electrode able to withstand clean water for almost three days. Though some difficulties are still experiences with perspiration, these electrodes perform much better than the standard available electrodes. Although in depth analysis and testing of the electrodes itself was not done and did not form part of this research, it is thought that the salt in the perspiration of the human body reacts with the glue on the ECG electrodes, loosening them from the skin after some time.

3. Development Summary

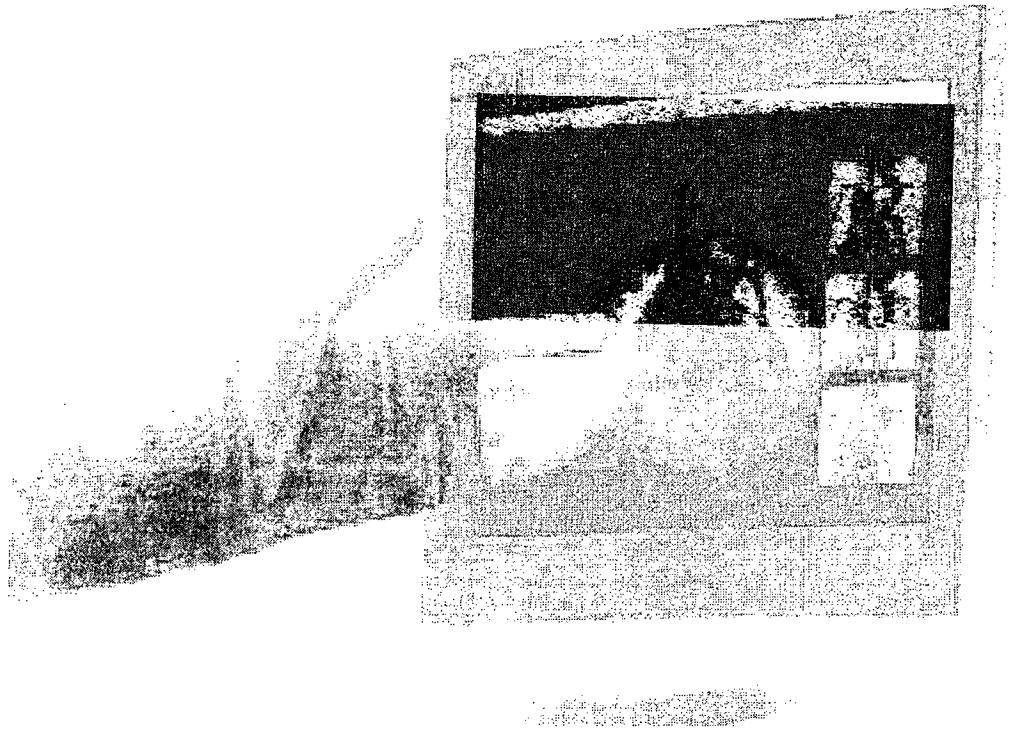
Subsystems Overall

Though all the subsystems assisting the ECG monitor, and forming part of the ECG data acquisition equipment in its whole were designed with the greatest care, it can still be shown that improvement on certain aspects of the ECG monitoring equipment is immanent.

This development is a first of its kind. The research stretched over a period of two years, and in this timeframe all design, development, testing and implementation took place. Considering any new development, this is a very short time span which, intrinsically left under-research, under-developed and gaps for further improvement.

The next part of this dissertation focuses on the evaluation of a few of the major role-playing parts.

Evaluating the Designs



1. Evaluation System as a Whole

Evaluation in the Broader Sense

Part I of this dissertation gave a brief explanation of the problems encountered when making use of currently off the shelf available heart rate monitors. A brief discussion on the advantages of having an ECG and heart rate monitoring system with the added functionality of transmitting the heart rate to a hand held computer unit in real time was also presented. A summary of the background research as well as literature study done before and during development of the ECG monitor was also given.

The text then went on to say that the purpose of this research is to design a fully functional ECG and heart rate monitor capable of tracing an ECG, determining the heart rate from the ECG signal, and transmitting the data to a hand held computer unit in real time. Elaboration on the design of the broader system surrounding the real time ECG monitor (data relay units, RF communication methods, the hand held computer unit etc.) was also presented as all of these subsystems are a necessary part of the outcome of the research, (although not the main focus of the research) to justify the design of such a sophisticated ECG and heart rate monitor. Without the mentioned subsystems, the end result of the research would not be visible and thus could not be tested and evaluated.

1.1 Subsystem Implementation and Overall System Evaluation

Overall Evaluation

To be able to evaluate the ECG monitor and more specific the front-end filter design, the broader system had to be implemented to assist in this task. Needless to say that the implementation of all these subsystems at once gave rise to a few unforeseen issues, the most prominent of which was the RF communication

issues. All of the RF ground planes and antenna choices had to be re-worked as the maximum distance obtained with the first field tests were about 50m. The Antenna choices and antenna ground plane designs were not covered in this dissertation. Communication design, RF techniques and antenna choices fall well outside the scope of this dissertation, but seeing that it formed an integral part of the success of this development, an in depth study of this field was required before any practical systems could be designed. It was also soon discovered that the original IF bandwidth of the RF communications system was twice as large as what was needed to transfer all of the ECG information from the athlete to the control units next to the field. Once these design errors were corrected the reachable RF transmission distances increased to about 800m without any loss of data at a rate of 57600Bps. (Refer to the fourth page of appendix B covering bandwidth explanations for an elaboration.)

1.1 Sampling Rate Evaluation

ADC Sampling Evaluation

Remember that part IV of this dissertation was concluded with the hanging issue of the system not being able to transmit all of the sampled data points of the digitized ECG signal away fast enough to still comply with the sampling theorem specifications. A discussion of the solution to this issue seems imminent as this was the first problem under scrutiny and a failure in this critical area could have meant that the system as a whole would be doomed.

A quick review of the issue at hand will refresh the readers mind. As was discussed in the last sections of part IV the problem was this: To enable the transmission of data over an RF channel, it is necessary to align the transmitter and the receiver with each other in order to assure correct *data slicer* operation on the side of the receiver and thus correct transmission of any data. (A data slicer is a complex piece of electronic equipment allowing the circuitry to extract a digital "0" and a digital "1" from incoming data which is represented as "1's" and "-1's" extracted from an analogue signal. The differences in carrier modulation, or in other words, the

differences in carrier frequency received are representative of a "1" or "-1". (Again, refer to any good text book covering RF modulation techniques for an in depth explanation of RF modulation and de-modulation.) This is a fundamental RF design issue. The amount of data (bytes) necessary to align the transmitter and receiver at the transmission speeds used in this application caused the software running on the microcontroller onboard the ECG monitor to run out of processing time. The result was that the sampling theorem discussed earlier in part III, could not be met.

The time it takes to transmit 25 alignment bytes, 4 UART alignment bytes and three header bytes, as was discussed on pages 126 through 128 in part IV, to ensure correct RF communication, took up more time than was available for sampling the analogue ECG signal and still comply with the sampling theorem stating that the minimum sampling frequency must be at least two times the highest frequency component in the signal sampled. And this is still not taking into consideration the processing time necessary to run the digitized ECG data points through the software network interference filter as well as the time necessary to encode the data bytes before RF transmission. What is more, the time it takes the microcontroller to actually sample the signal and switch on and off the RF transmitter also need to be added to the equation.

It is also worth mentioning that the microcontroller used on the ECG monitor is a controller from the PIC series, specifically an 18F252 which is driven by a 20Mhz crystal which relates to a clock speed of 50ns.

To understand why exactly 25 alignment bytes, four UART alignment bytes and three header bytes was used to assure correct RF transmission is a discussion for another dissertation on RF communication. However, this information can be found in the datasheet of the RF transceiver units implemented in this design supplied with the technical documentation in appendix D.

After the solution to this problem presented itself it seemed like a simple one indeed, but one that was crucial to have in order to realize it. In order to explain the solution, some fundamental background on RF transmission needs to be supplied.

Once an RF receiver is switched on many of the internal components need to settle at the operating frequency. The data or bit slicer needs to settle at an average preset voltage level in order for it to be able to distinguish between voltage values above and below this average value. (These voltage levels above and below the average value indicates a "1" or "-1".) In very simple terms, this is how bit slicing works. A voltage level higher than this average level presents itself as a digital 1 and a voltage level lower than this value presents itself as a digital 0. The problem is this: Long runs (transmitted strings) of 0's will have this average voltage level drop, and continuous runs (transmitted strings) of 1's will have this average voltage level increase. This results in the receiver not being able to distinguish between 0's and 1's correctly, simply because the average voltage level is changed, in other words the data slicing process becomes corrupt and the so called transmission loss occurs.

What is important is that the initial voltage level of $0V$ needs to be lifted to the average voltage level after the receiver is turned on and a carrier signal is detected. For different RF receivers specifications may differ, but in this case for the specific receiver used in this project the time needed to lift the average voltage level to the correct value is at least 5ms. (Refer to appendix D for the origin of this information.) In other words, after the receiver detects a carrier signal another 5ms at least must go by so that the receiver can get this bit slicing reference voltage to the correct level.

In order to help the receiver with this operation the common practice is to transmit a string consisting of even amounts of 0's and 1's from the transmitter after the receiver was switched on. In this case 25 bytes of 0xAA (binary: 10101010) was transmitted. By doing so the settling time of the receiver may be shortened somewhat.

Doing the calculation results in the following:

$$\left[\frac{1}{57600Bps}\right]\times 10bits\times 25bytes = 4.34ms$$

Now, by doing the same calculation for the remaining 7 bytes (4 UART synchronization bytes and 3 header bytes) to be transmitted before a data byte can be sent it is found that the total transmission time for setting up the receiving end of the system results in 5.55ms as explained on pages 133 through 134.

Understanding this, the same logic can be applied in the reverse direction. It is imminent to understand that just as it takes some time for this average bit slicing voltage to get to the correct voltage level it also takes some time for it to drop from this reference voltage. *And it is in this where the solution to the problem lies.*

Running the microcontroller at 20Mhz, it takes $6\mu s$ to sample one point on the incoming analogue signal. The reference voltage of the receiver on the receiving end can not drop from the correct value far enough in this period of time to result in data loss. Meaning that; The software on the receiving end was changed to keep the receiver switched on continuously. On the transmitter end (ECG monitor) the software was changed to set up the receiver immediately after the unit is switched on. In other words, the 25 bytes of 0xAA are transmitted immediately after the unit comes online as is the 4 UART alignment bytes. From here the microcontroller samples a single point on the incoming analogue signal, passes it through the FIR filters, encodes the data point for transmission, transmits the 3 header bytes and the data point and returns for another sample. Put simply, the alignment procedure is carried out only once from where the software is in a loop to sample and transmit only the header bytes and the data points. The processing time gained by this software change can be calculated as follows:

$$\left[\frac{1}{57600Bps}\right]\times 10bits\times 4bytes = 694.33\mu s$$

Subtracting this from the original value gives:

$$(5.55\times 1000)\mu s - 694.33\mu s = 4.855ms$$

To be able to sample at a rate of at least 240Hz, twice the highest frequency component value in the ECG signal it is necessary to sample a point at least every $4.166ms$. It should now be clear that by making this change to the software this specification is met. To put this modification into perspective it would now theoretically be possible to sample and transmit a new point every $694.34\mu s + 6\mu s$ (where the $6\mu s$ is the time it takes to sample a point) not taking into account the time it takes the microcontroller to operate. This relates to a possible sampling frequency, F_s of 1427.87Hz.

1.2 I.A (Front-End) Design Evaluation

I.A Evaluation

Refer back to figure 55. The analogue front-end part of the design includes an I.A for acquiring the raw ECG signal from the human body assisted by a common mode driver. This part of the design is followed by an in-line band-select filter and a non-inverting filtering-amplifier.

The only practical way to evaluate this part of the design lies within the boundaries of a theoretical testing procedure. This includes testing the frequency responses of the filters by frequency sweeps, testing the filters for phase responses and doing an amplification test on the final part of the design. Although this testing could not have been left until after the final design, as it is an integral

part of the design to make the ECG monitor function correctly, the results will be discussed here.

Starting at the I.A, it is not even worth mentioning that the output of the I.A will be of a wide-band nature. As to answer the question of how wide?; This information can be found in the data sheet of the specific component. The reader is urged to take a quick look at the design again.

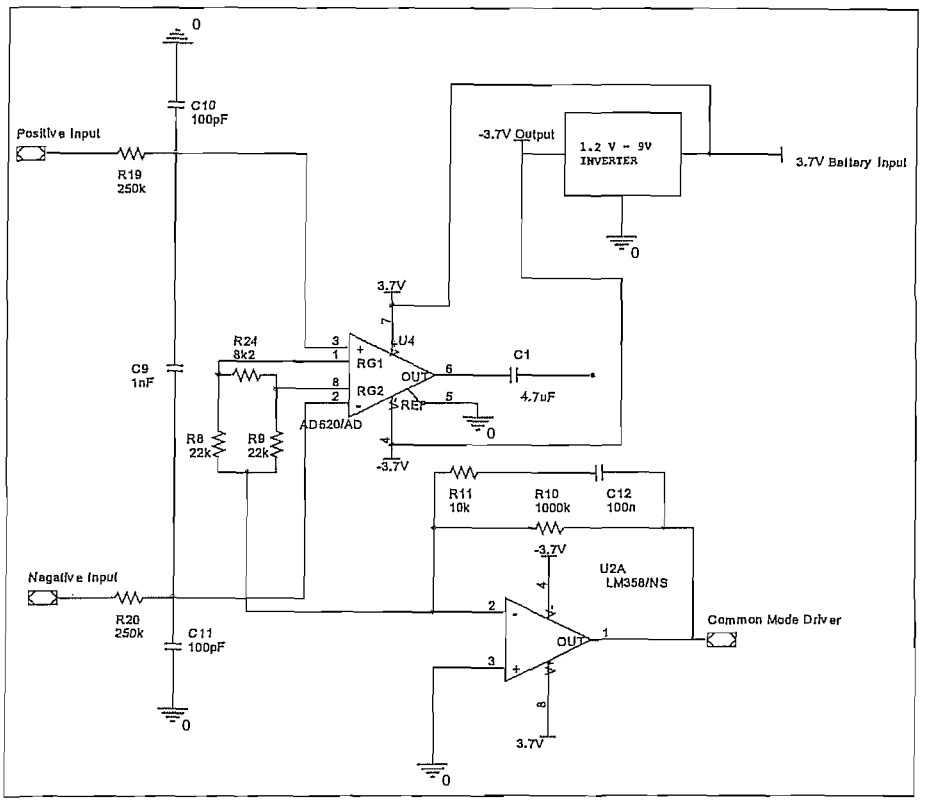


Figure 58: Final I.A Design Assisted by a Common Mode Driver

Figure 49 depicts the final I.A design implemented on the ECG monitor. (Extracted from figure 46.) Referring to the data sheet of the AD620 I.A used in the design it can be seen that the operating bandwidth of this component is about 1MHz which extends the bandwidth capabilities far beyond that necessary for this application. This wide-band output of the I.A also extends far beyond the boundaries within which the following operational amplifier used in the band-pass filter will stay

stable. When, theoretically testing the design, this was the first issue needing attention. It was necessary to look at possible design techniques to help band-limit the output of the I.A. To answer the first question that arises when looking at figure 49 namely: What are the roles of the $250k\Omega$ resistors, 100pF and 1nF capacitors on the input lines of the I.A? It is to band-limit the output of the I.A. These components create a simple passive low-pass filter through which the raw ECG signal passes, even before it enters the I.A. These results were discussed in more detail as part of the overall filtering sequences build onto the ECG monitor on page 94. The band to which the signal is limited is 0Hz through 530.5Hz and is calculated as follows:

$$LPF\ value = \frac{1}{(2\times\pi\times 250k\Omega)\times(1nF + 2\times 100pF)} \quad \textbf{(1.38)}$$
$$= 530.5Hz$$

The theory for adding capacitors in parallel is forthcoming. This design technique already rids the incoming signal of much of the contained high frequency content and immediately creates an intrinsically stable environment for the upcoming operational amplifiers to operate in. The result of this design is shown in the following graphs on pages 148 through 150. Figure 50 illustrates the simulation result of the I.A with no passive filter design on the input whilst figure 51 illustrates the frequency sweep result of the I.A design including the passive filter at the input of the front-end.

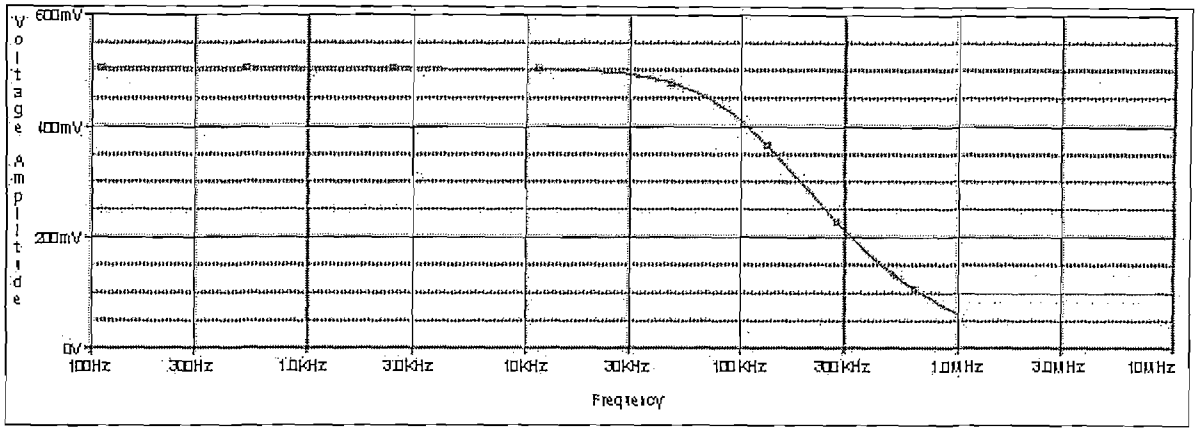


Figure 59: Frequency Sweep of I.A with no Passive filter

It is easy to see that the I.A (AD620) starts attenuating the amplitude of frequencies above roughly 30kHz by some margin and almost completely suppresses frequencies above 1Mhz. This is an intrinsic characteristic of the I.A. No attenuation is applied to frequencies in the range of 0Hz through 120Hz, the area of interest to this design. Furthermore, figure 51 illustrates the effect of the passive low-pass filter constructed in front of the I.A to suppress frequencies above 530Hz completely even before the signal enters the I.A.

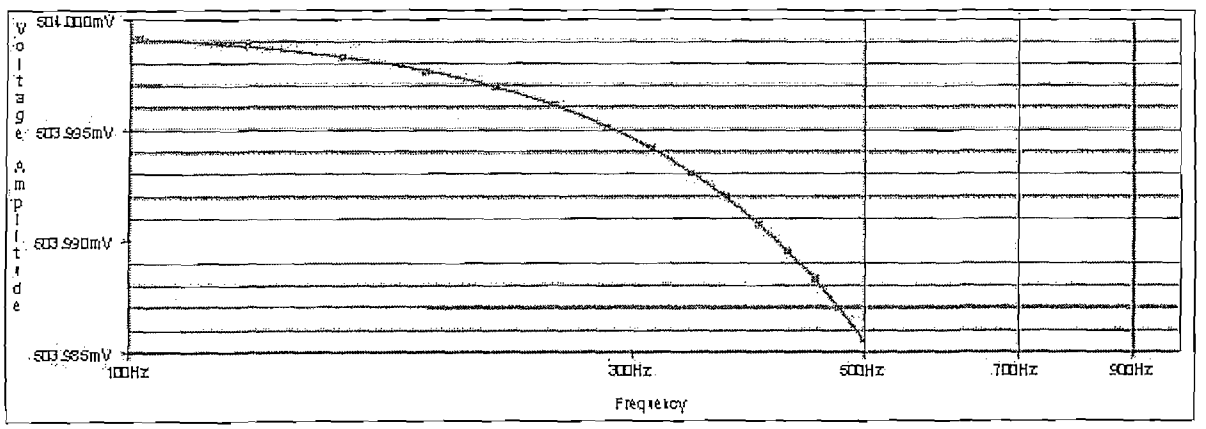


Figure 60: Frequency Sweep of I.A with Passive filter

What can also be seen from both the frequency sweep graphs is the amount of amplification applied by the I.A. One of the characteristics of an I.A is the amplification applied by the component. The amount of amplification can be controlled by an

external resistor setting. (Refer to part II of this dissertation for an in depth discussion on the I.A design.) As discussed in part II of this dissertation covering the I.A design, and can also be retrieved from the data sheet of the component, a specific formula applies to the amplification of the I.A. The formula governing the amplification of the AD620 is as follow[14]:

$$G = \frac{49.4k\Omega}{R_G} + 1 \qquad \textbf{(1.39)}$$

From here it can be calculated that the gain applied by a resistor of $8.2k\Omega$ as depicted in figure 49 on page 146 is:

$$G = \frac{49.4k\Omega}{8.2k\Omega} + 1 = 7$$

For the purpose of the frequency sweeps in figures 50 and 51 a $1k\Omega$ gain resistor and an input signal of 10mV was used for illustration purposes which resulted in a gain of 50.4 as can be seen from the two graphical representations.

Remembering that the peak-to-peak voltage values of the raw ECG signal lies roughly between $2-8mV$ the amplitude outputs of the I.A are between $14-70mV$. The design modification made to the input of the I.A was considered successful as it clearly band-limits the output of the I.A to under 530Hz and allows for the rest of the filtering circuit to operate well within a region of stability. This can again, theoretically be justified by the graphical outputs of the frequency sweep operations performed on the I.A design, as they are depicted in figures 50 and 51.

1.3 Chebyshev Band-Pass Filter (Front-End) Design Evaluation

Evaluating the Band of Interest

Now that the output of the I.A is limited to a bandwidth of 530Hz and peace of mind has been obtained about the stability of the operational amplifiers with regard to high frequency common mode inputs for the rest of the circuit, let us take a look at the evaluation results of the band-select filter.

One of the best ways to look at the results expected from the band-pass filter is again, making use of theoretical evaluation methods, by looking at the frequency response of the filter. This was done, as the previous frequency sweep evaluation of the I.A design, with the help of the software simulation package, OrCad 9.0. Figure 52 illustrates this frequency response.

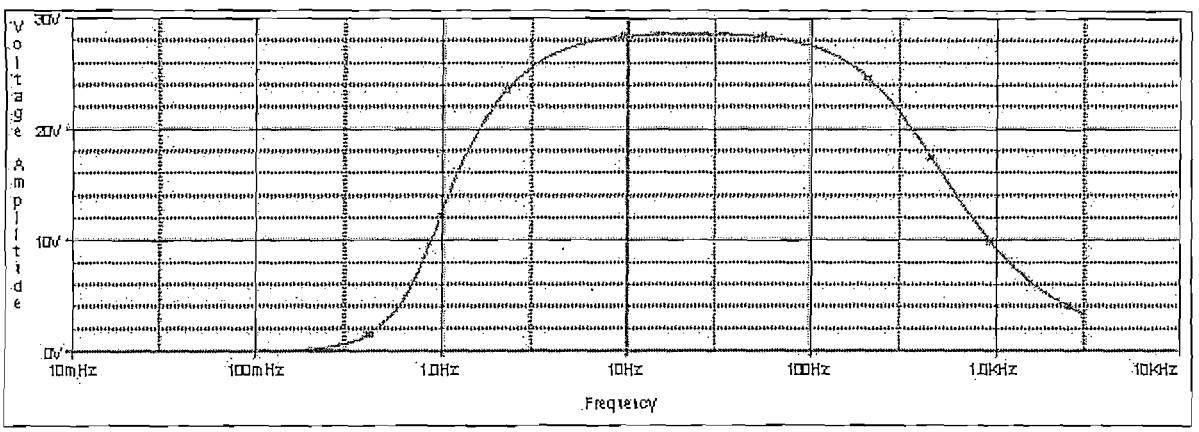


Figure 61: Frequency Sweep of Chebyshev Band-Pass Filter

Again, looking at figure 52 a gain resistor of $1k\Omega$ was used, simply for the purpose of illustration. The already band-limited signal entering the band-pass filter is further band-limited to a pass-band between roughly 0.5Hz and 120Hz. The question of why some of the frequency content above 120Hz still passes the filter, when it is said that the signal is band-limited to between 0.5Hz and 120Hz, might be raised. The reason for this result is a simple one, yet obtained again from practical consideration. Remember that one of the crucial design specifications of the ECG monitor was to

keep it as small as possible for packaging reasons. The band-pass filter implemented was a simple second order filter and striving towards an ideal filter response with a second order filter is nearly impossible. It is evident though, that all frequencies upwards from 120Hz are attenuated somewhat. This reason, along with the other advantages of a class II Chebyshev filter as discussed earlier imposed the decision to implement this filter. Referring back to section 7 in part II of the design documentation, it is now evident in the evaluation of this filter that no major ripple is detectable in the pass-band or the conversion-band, and that the attenuation achieved in the stop band of this filter is excellent for such a small order.

As figure 53 demonstrates, combining this result (green graph) with the band-limiting effect (red graph) of the passive filter in front of the I.A makes for a very successful band-pass filter effect on the raw ECG signal. Figure 54 demonstrates the combined effect of the passive low-pass filter, I.A, band-pass filter and amplification stage.

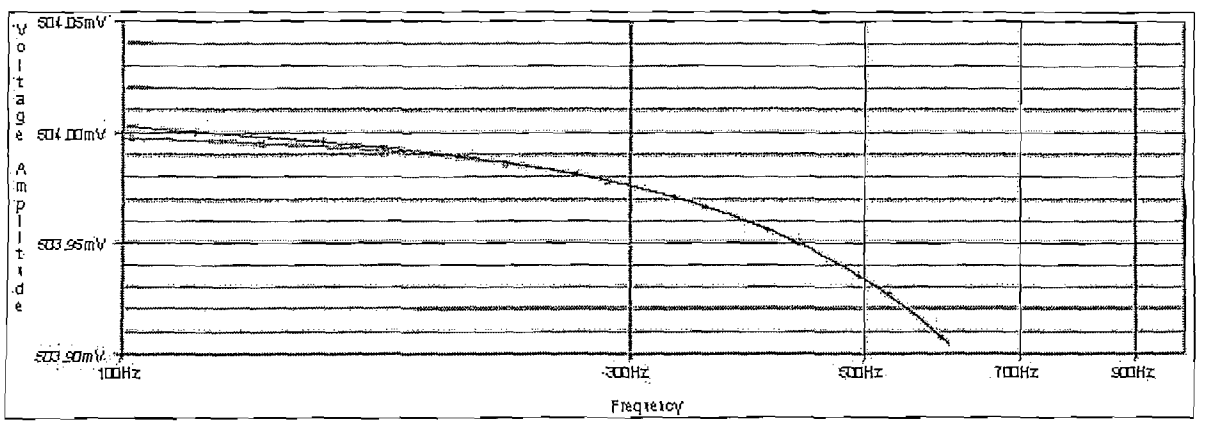


Figure 62: Enlarged Overlay of I.A and Band-Pass Filter High-end Outputs

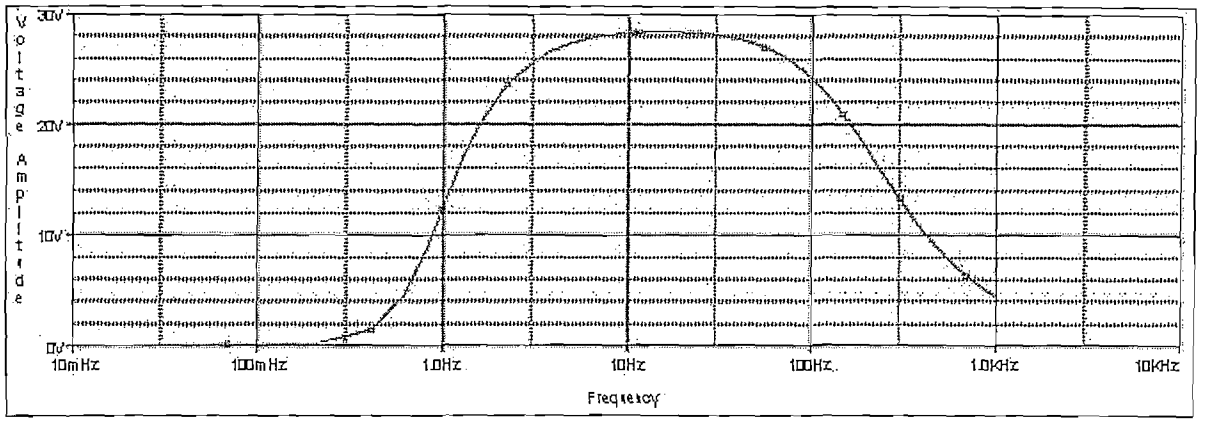


Figure 63: Result of I.A, Band-Pass Filter and Amplifier Stages Combined

Taking into account that this ECG monitor design called for a very small, light weight package that needed to conform to athletic standards the use of more clever and elegant designs were necessary in order to reduce component counts as well as operating currents. Making use of the passive low-pass filter implemented in front of the I.A combined with the band-select filter following the I.A and a further bandwidth restriction introduced by the implementation of a capacitor in the feedback loop of the amplification stage (refer back to the amplification design in part III) unfolded a delicate and classic filter design, which practically, proved to be the solution to the space and weight constraints put on this project.

1.4 (FIR) Network Interference Filter Evaluation

Software Filter Evaluation

As this part of the filter design was implemented in software, the physical results of the evaluation could be seen much more clearly than was the case with the analogue circuit performance results. Simply by changing the values of the software filter parameters, the outcome of the filter can be changed in real time, for comparison reasons.

Keeping the following diagram in mind and having the actual FIR filter specifications as designed in software at hand, it is possible to see that the

elimination of 50Hz network interference is possible after a digital signal is passed through this filter.

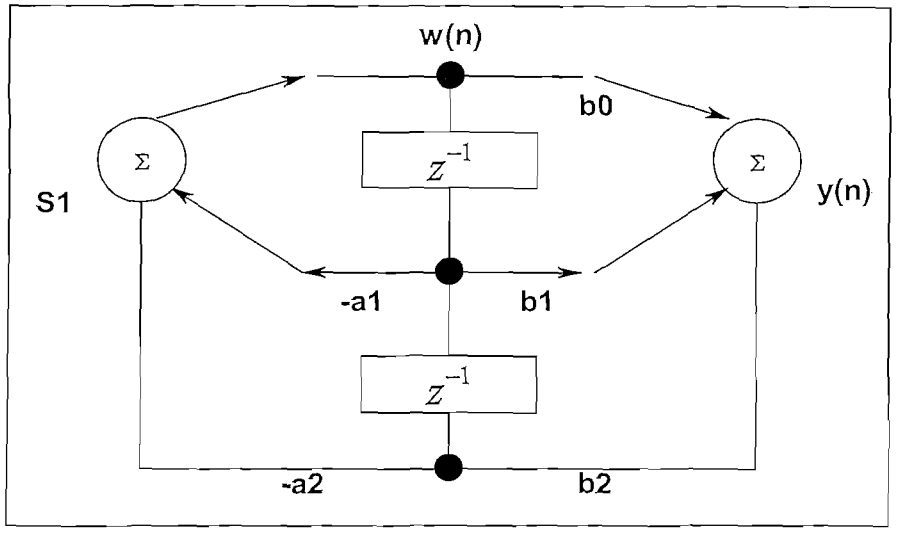


Figure 64: 2nd Order FIR Filter Structure

Figure 55 shows the basic theoretical architecture for an FIR filter. Although it uses blocks to indicate the different components it serves just as well. The main components are coefficients and data memories, analogue input units, multipliers and a controller. (The obvious components are not shown here.) [15] Normally the components necessary to implement an FIR filter is off the shelf and cheap to come by. At each sampling instant, a new data sample, $x(n)$, is read from the ADC of the microcontroller and saved in data memory. Each input data sample and the corresponding coefficient are fetched from memory simultaneously and applied to the multiplier. The products are then accumulated to yield the output sample. The computation of each output sample, $y(n)$, requires *N* data-coefficients fetched from memory and *N* multiplications and accumulations.

As discussed in part III on pages 97 through 116, two 200th order notch FIR filters were cascaded. The reason for cascading the filters is simply to reduce processing power needed and to reduce the complexity of the software necessary to implement on a simple microcontroller. Furthermore this simplifies the process of

passing sampled points through the software filter. Remembering that the computation of every output sample, $y(n)$, requires *N*-coefficients fetched from memory as well as *N* multiplication computations, implementing a 400th order FIR notch filter in a single step would require twice as much memory space as well as considerable larger variables. Seeing that the largest variables to be housed on a PIC18 series family microcontroller is 32bits, and multiplication operations on these variables take up considerable more time than multiplication operations on 8 and 16bit variables, cascading two 200th order filters made for the best solution.

Mathematically the FIR filter was implemented on the microcontroller in software (using low level C as the programming language) as follows:

$$y(n) = b(1)x(n) + b(2)x(n-1) + ... + b(mb+1)x(m-mb) - a(2)y(n-1) - ... - a(ma+1)x(m-ma) \quad \textbf{(1.40)}$$

where n-1 is the filter order and m is the current sample.

The input output description of the filter operation in the z-plane is as follows:

$$Y(z) = \frac{b(1) + b(2)z^{-1} + ... + b(nb+1)z^{-nb}}{1 + a(2)z^{-1} + ... + a(na+1)z^{-na}} \quad \textbf{(1.41)}$$

The filter implemented was a type II FIR filter which means always implementing an even order filter.[16] This type of filter was chosen because for odd numbered FIR filters, the frequency response at the Nyquist frequency is necessarily zero.[16] The results of the filter are depicted in figures 56 through 58.

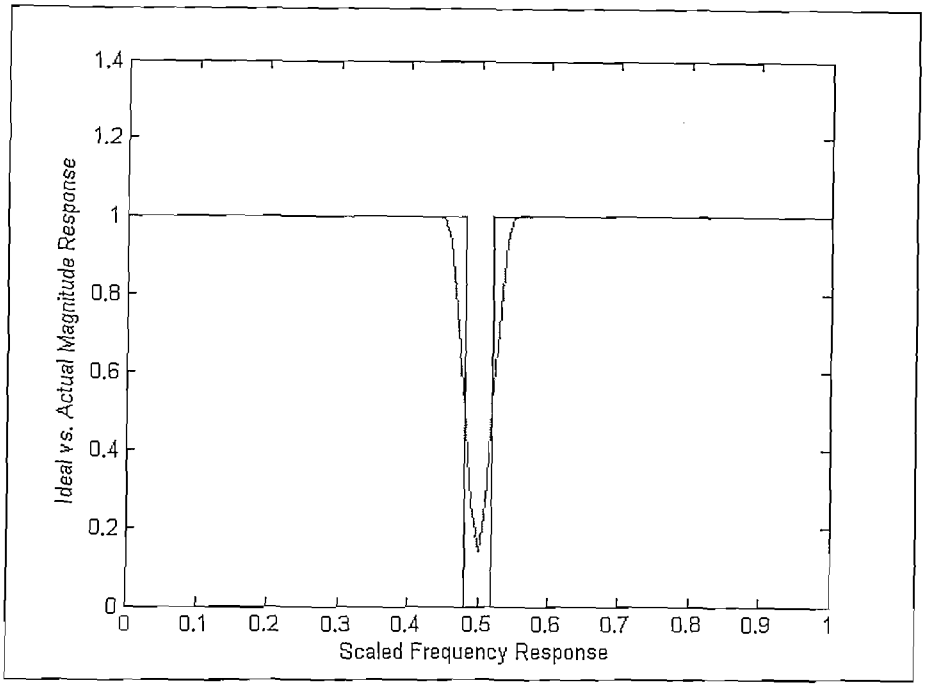


Figure 65: Ideal vs. Actual Filter Response

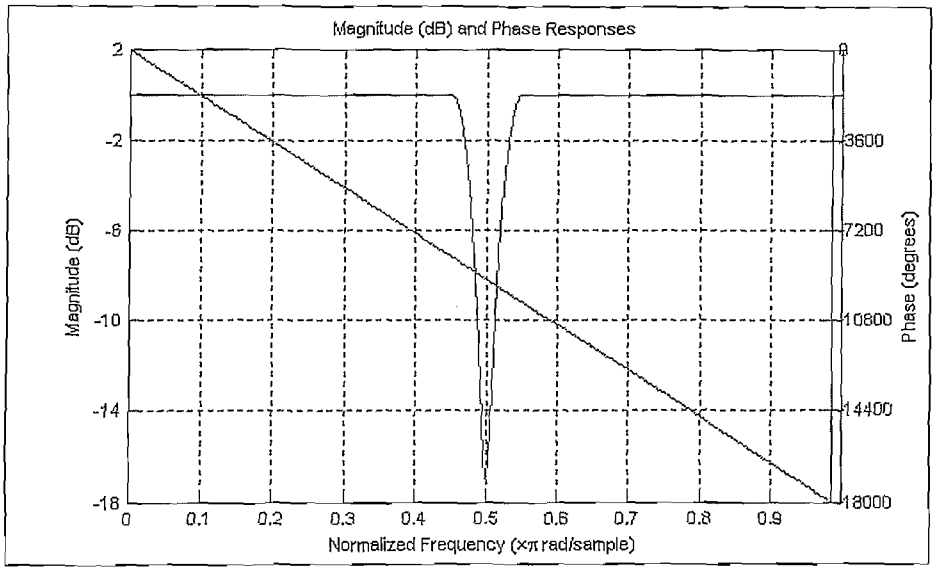


Figure 66: FIR Filter Notch and Phase Response

It can be seen in figure 56, that even with a 200th order FIR filter implemented, the actual filter response (graph in green) still differs a great deal from the ideal response (graph in blue). Increasing the filter order though, will result in a loss of

processing speed and power as well as bring with it all the issues as discussed on page 154, and will again start influencing the rest of the microcontroller operation. The band stopped by cascading two 200th order FIR filters lies between 48Hz and 52Hz with a little attenuation of signals 4Hz upward and downward from these values.

Figures 57 and 58 depict the actual filter magnitude and phase response over a period of time. The *blue* graph represents the filters magnitude response whereas the *green* graph represents the filters phase response.

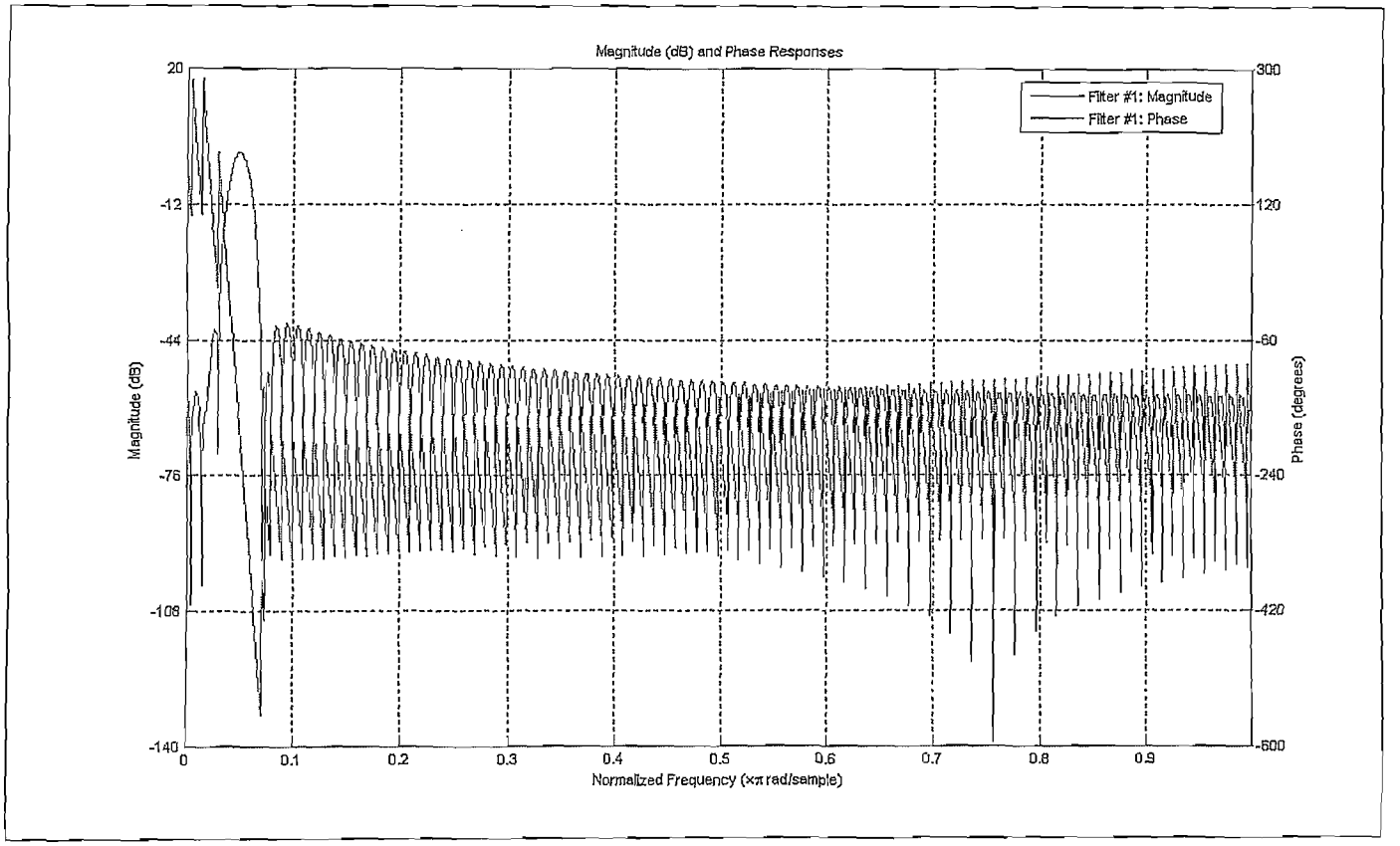


Figure 67: 200th Order type II FIR Filter Magnitude and Phase Response

With everything taken into account, processing speed, filter order, cascading of FIR filters and sampling speed, the next figures, representing filter output, clearly shows that the filter operates extremely well as a 50Hz notch filter in software.

Figure 56 through 59 results were obtained by simulating the software filter in MATLAB R13.

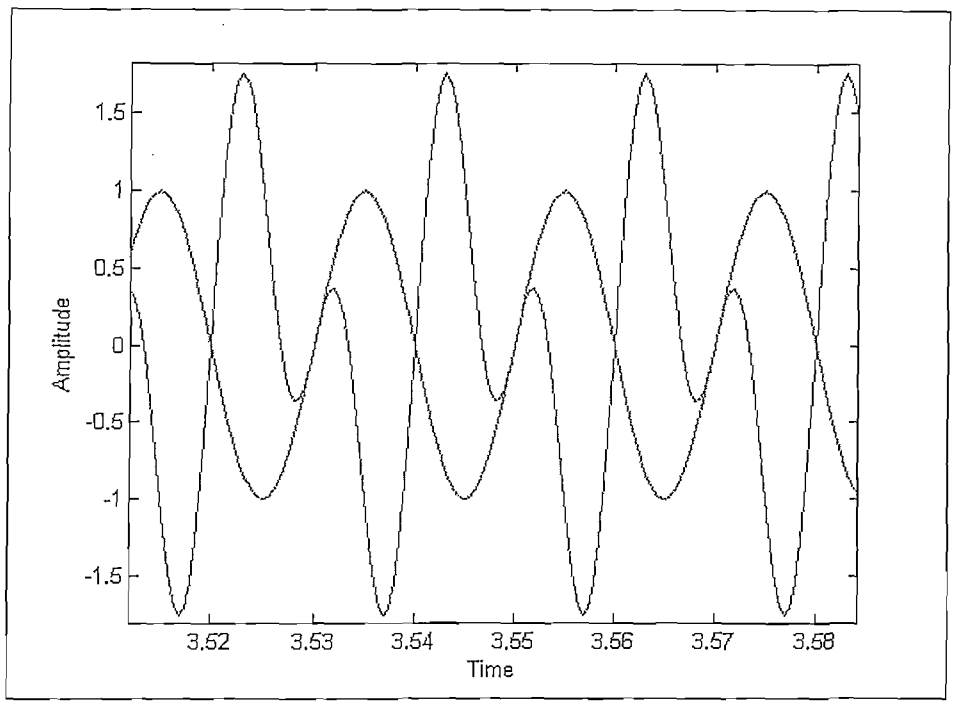
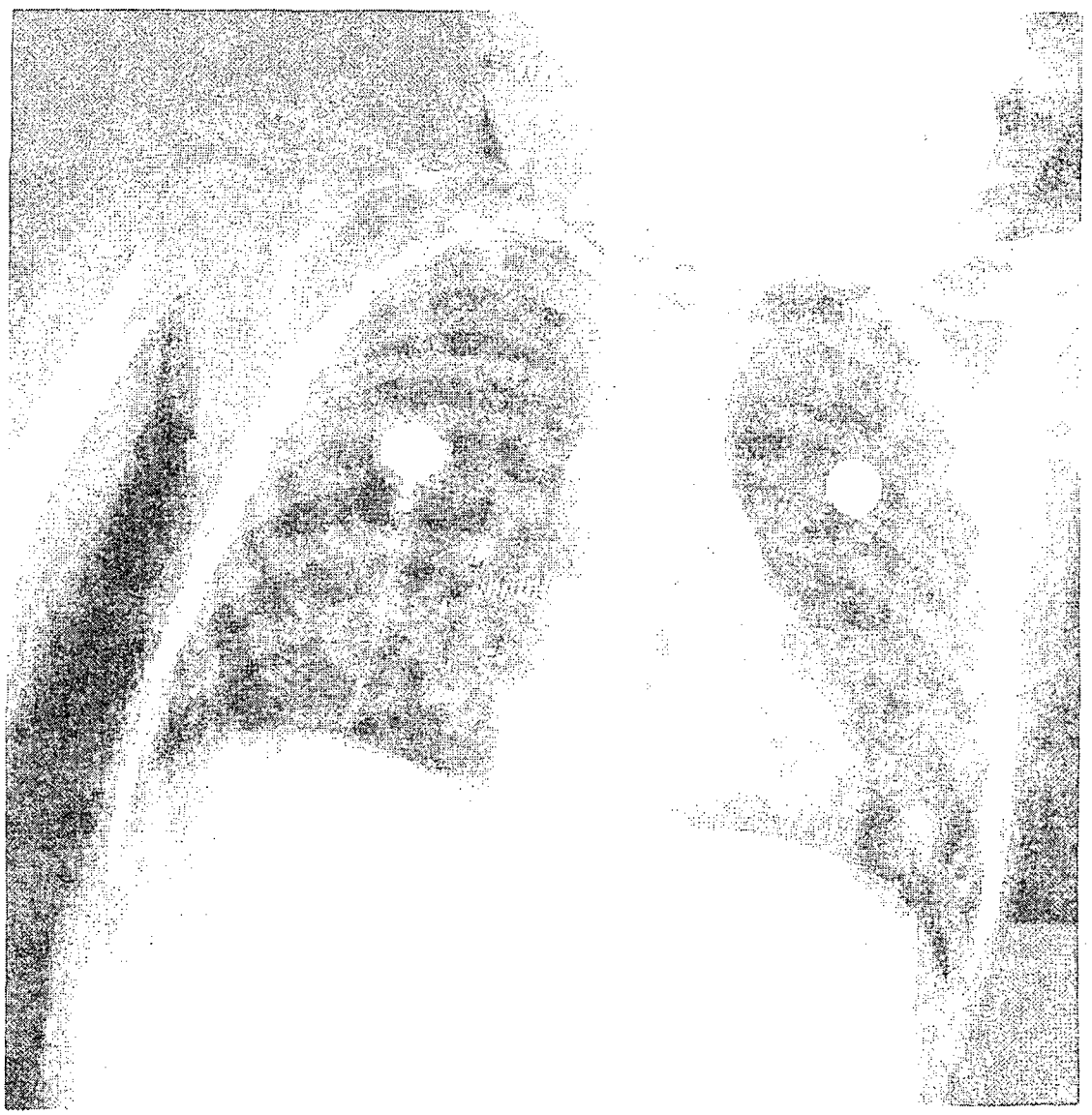


Figure 68: Unfiltered Input vs. Filtered Output Signal

The blue graph in figure 59 represents a (100+50)Hz signal to be passed through two cascaded 200th order type II FIR filters. The red graph represents the clean 100Hz output signal as it was filtered in software. Notice the phase shift of the output signal. For the purposes of this application, the phase shift is not an issue. What is more, whenever the filter needs changing to filter 60Hz in stead of 50Hz network interference, it is easy to redesign and change the software accordingly as the only changes involve changing the software filter parameters.

Tying Together the Knots



1. The System as an Entity

Unification

In an epoch where the human live as a success driven species it has become a necessity to strive for perfection. Not only in what can be seen, but also in the invisible details. The success of this research and the resulted product rested purely on this philosophy.

A successful outcome for this research meant presenting the sports world with a working ECG monitor that can operate under strenuous circumstances. But even more basic than that, understanding the basic principles of filter design, implementation, manipulation and development, as this was the resting foundation for a successful outcome. Furthermore the design needed to be integrated into a larger product where it could be put to use. This larger product overall includes the RF data relay units, the hand-held computing unit as well as the high level analysis software. The research presented, in part, for this dissertation focused mainly on the design of the filtering processes and how they needed to be manipulated and implemented to support the outcome of the project. Though, by filtering alone it would not be possible to retrieve, manipulate, transmit and display a real time ECG signal.

The story of the research is not one of success only and by far not one that is not to be improved upon. Designing a filter to rid a signal from a single interfering frequency might seem like a simple idea, but when space, weight, power consumption and processing power becomes critical, and one interfering frequency becomes a few, many issues arise when the analogue and digital worlds are wed in order to satisfy specified requirements.

The main constraints introduced by any analogue to digital conversion process in a real time digital signal processing system have already been discussed throughout the text and the following is but a simple outline of these issues.

- The use of a finite number of bits to represent data introduces an intrinsic error of which the quantization error is the most prominent. This is propagated into subsequent signal processing.
- High resolution ADC components are slow, in general. Although for this application the sampling rate does not need to be extremely high, some improvements may be possible with other DSP techniques such as the over sampling technique.[16]
- ADC processes are subject to a variety of other issues such as temperature shifts and non-linearity issues.
- If the ADC contains a sample and hold circuit, this output will be wideband which will increase the noise at the ADC input.
- Aliasing errors from analogue signal energy, (perhaps the most difficult to solve of all) outside the band of interest is always present.
- To reduce aliasing, band-limiting analogue filters need to be introduced.
- Analogue band-limiting filters are bulky and the higher the order, the bulkier they become.
- Introducing active components such as operational amplifiers to assist with analogue band-limiting, intrinsically introduces more noise into the overall system.

Listing these common topics, each one perhaps to be covered in a dissertation of its own, might seem like paranoia but the issues, designs and solutions spreading from each one of these listed topics, justifies a research and dissertation on their own.

2. Recommendations for Possible Improvement

Possible Areas to be Improved On

Fancying an end product not to be improved on seems to be the dream of every designer. However, reaching this goal seems to be near impossible. It is often the case that the production process takes up so much time that, by the time the first version reaches the market, an improved version is already constructed. The latter also seems to be the case with this newly designed ECG and heart rate monitor.

2.1 Improving the Sampling process

Sampling Improvements

Refer back to section 1.2 of the evaluation part of this dissertation. The possibility of a sampling rate increase, leads to the first recommendation for an overall system performance improvement. One of the fundamentals taught by digital signal processing experts is the idea of over-sampling. In practise, over-sampling a signal means, sampling an analogue signal at a rate much faster than is indicated by the *Sampling theorem*. The ratio between the actual sampling rate and the suggested rate is referred to as the over-sampling rate and is given by:[15][16]

$$Over-sampling\,rate=\frac{F_s}{2f_{\max}} \qquad (1.42)$$

The trend in many digital signal processing systems is always to over sample to exploit the practical implications of the over-sampling theorem. At the analogue to digital interface some of the main benefits may be[15]:

1. Simplification of the anti-aliasing filter
2. Support for anti-aliasing filtering with variable cut-off frequencies
3. Reduction in the ADC noise floor by spreading the quantization noise over a wider bandwidth.

The possible improvements by implementing these changes may be using an ADC with fewer bits, thus still increasing the time available to sample and still achieve the same signal to noise ratio performance as a higher resolution ADC.

2.2 Improving Band-Pass Filtering With the Aid of the Amplifier

Improving on Band-Selection

s the amplification of an analogue signal was not part of the main focus of this research, not much attention was given to a special design of an amplifier. As discussed earlier, a simple non-inverting amplifier was constructed to begin with. This was done in order to lift the voltage values of the analogue ECG signal before the sampling process. It should be possible though, to construct an amplifier that will help with the band-limiting of the signal. All tests and simulations run lead to this assumption. Have a look, for example, at amplifier circuitry shown in figure 60 on the next page:

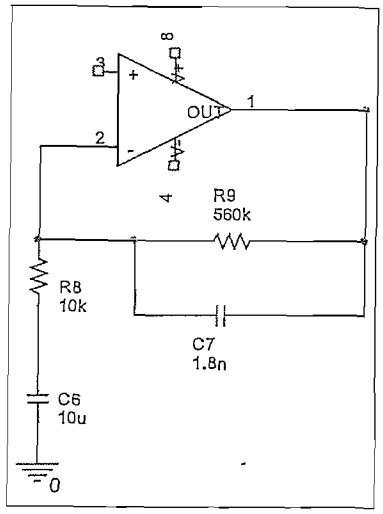


Figure 69: Non-Inverting Amplifier

Figure 60 depicts a standard non-inverting amplifier, except for one component, C7. This capacitor is not part of a standard amplifier with a gain set to 1. To keep component count to a minimum and current consumption as low as possible, the value of C7 could be adjusted to further aid in the limiting of the bandwidth of the ECG signal before the ADC process. This capacitor acts as a simple cut-off at higher frequencies and can be implemented in a very small space. It is possible to change the band-pass filter following the I.A as discussed and implemented with the addition of some gain in the filter itself. The problem usually is simple, as taught by filter theory: Creating a band-pass filter with gain usually calls for much higher order filters than first or second order filters.

2.3 Shielding Driver Design

Improving Signal Quality by ECG-Lead Shielding

Tests showed that, the movement of the wires leading from the ECG electrodes attached to the athletes body, to the ECG monitor acts as antennas, contributing to an enormous amount of noise and base line drift of the ECG signal. Refer back to page 134 through 136 and the discussion on *special wiring*. It should be possible to use a type of wire with a shield around the main conducting wire and then

design and construct a shielding driver that will actually drive this shielding at a specific potential. Have a look at the following depiction:

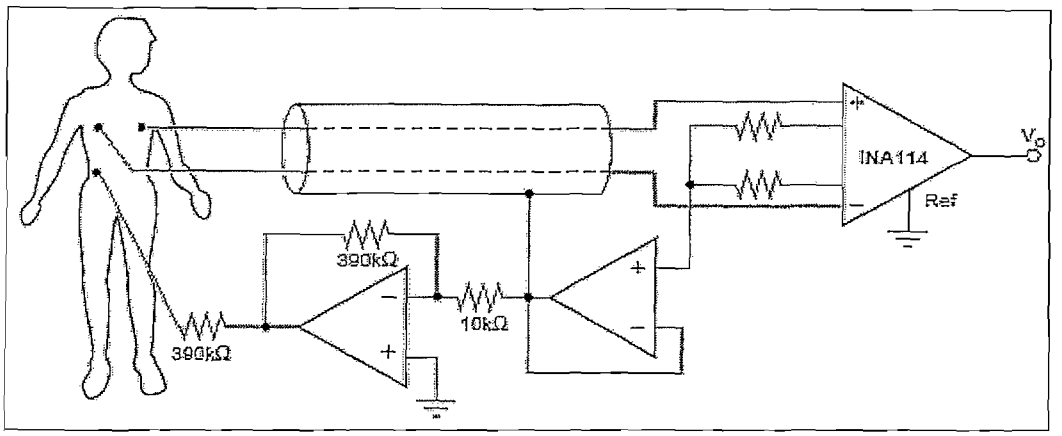


Figure 70: Possible Shielding Driver Construction

Assuming that the operational amplifier in the bottom left hand corner of the depiction represents the common mode driver as discussed in part III, it seems possible to take a copy of the common mode rejected by the I.A across the gain resistors, possibly amplify them and drive the shielding around the ECG leads at a voltage level equal in time, but amplified from the common mode present in the ECG signal in order to keep the leads from picking up any extra noise as a result of movement, touching or nearby external sources. This is a topic needing much more extensive research and suggesting a possible additional project all by itself.

3. A Final Word

Synergy in a Design

A tremendous amount of research and work is currently under way to improve the output of the ECG monitor in sporting conditions for example water-proofing the monitor itself. Both hardware and software are receiving attention.

Hardware can be made smaller by means of etching processes and software can almost always be made faster. Taking into account that the current size of the ECG monitor is 62mm x 32mm including the transmitter and receiver and that the reaching distance of the system is 600m in open space, the success of the system depended solely on the correct filtering and processing of the acquired ECG signal. Further improvements in software might include not transmitting the entire ECG signal after sampling but only the difference between samples to reduce transmission time even further. Hardware components are already all populated with 0603 surface mount components, but size may be further reduced when all components start becoming available in the new 0402 format. Another improvement might be to have the entire ECG acquisition front-end etched onto a single IC.

Though the non adaptive, analogue filtering techniques are faster, much faster, than digital filtering methods, for this research, it did not always seem to be the best choice in the application. Packaging, size and weight were important aspects to keep in mind when designing the ECG monitor for the sporting environment. Filtering techniques will never be perfected, especially not to the extent where no further improvements can be made. It is important to remember though, that the filtering process and the design of filters is an art. Whether constructing a robust filter to keep voltage supply lines clean or weaving a delicate line of filters together to retrieve a small ECG signal from the human body, knowing and understanding the basics and keeping at them are important. Having the analogue and digital worlds meet and complement each other is a delicate interrelationship to be understood and managed throughout an entire design.

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APPENDIX A

A short description on SA nodes, AV nodes, AV bundles and Purkinje fibres

The P wave arises when the impulse from the SA node sweeps over the atria. The QRS complex represents the very rapid spread of the impulse from the AV node through the AV bundle and the Purkinje fibres and the electrical activity of the ventricular muscle.[3]

The initial depolarization arises in the sinoatrial (SA) node, located in the right atrium. The SA node is the normal pacemaker for the entire heart and so its discharge rate determines the heart rate.

The link between atrial depolarization and ventricular depolarization is a portion of the conducting system called the atrioventricular (AV) node, which is located at the base of the right atrium. The action potential spreading through the right atrium causes depolarization of the AV node.

After leaving the AV node, the impulse enters the wall between the two ventricles via the bundle of His (atrioventricular bundle). A layer of non-conducting connective tissue, pierced by the bundle of His, completely separates each atrium from its ventricle. The bundle of His divides into right and left branches which leaves this non-conducting septum and makes contact with Purkinje fibres.

The Purkinje fibres rapidly distribute the impulse throughout much of the ventricles. Finally, the Purkinje fibres make contact with
non-conducting-system ventricular myocardial cells, via which the impulse spreads through the rest of the ventricles.

APPENDIX B

Sudden Death Syndrome (SDS)

Sudden Death Syndrome (SDS) is an umbrella term used for the many different causes of cardiac arrest in young people. Doctors and medical study provides medical information on the most common causes of unexpected sudden cardiac death in the young (under 35). These conditions include thickening or abnormal structure of the heart muscle and irregularities of the electrical impulses that upset the natural rhythm of the heart.

Sudden Death Syndrome events are defined as non-traumatic, non-violent, unexpected occurrences resulting from cardiac arrest within as little as six hours of previously witnessed normal health.

It is often difficult to consider that someone who is apparently young and fit may be at risk. There have been a number of reported incidents of misdiagnosis culminating in a tragedy that could have been avoided.

Sporty youngsters stress their heart the most. If they have an underlying cardiac abnormality they are more likely to be at risk. Sport itself does not lead to cardiac arrest but it can act as a trigger for a young person to die suddenly by exacerbating an undetected condition.

The majority of young sudden deaths are due to inherited forms of heart muscle disorder and irregular heart beat. Hypertrophic Cardiomyopathy is the most common of these conditions. Recent research in the USA by Dr. Barry Maron shows that 1 in 500 people have Hypertrophic Cardiomyopathy alone - just one of the many cardiac condition responsible for young deaths.

APPENDIX C

- RF -

BASICS NEEDED TO GET STARTED

1. INTRODUCTION

You should notice as you read this text, that certain terms keep repeating themselves. These terms are also usually the biggest headache giving problems when designing telecommunication systems.

- **Bandwidth** - Information signal bandwidth. The bandwidth necessary to transmit a certain amount of information given certain specifications.
- **Information Rate** – A measure of the maximum signal rate of change that affects audio and video sharpness. Also a measure of the maximum bit rate in the digital world.
- **Noise Interference** – Measured against bandwidth. Signal-to-noise ratio for analogue and digital signals. (Examples are: Timing jitter and bit error rate for digital systems.)
- **Distortion** – Frequency distortion and phase distortion and amplitude distortion in analogue systems.
- **Multiplexing** – The spreading of signals by time, frequency of phase to allow for transmitting them simultaneous.

2. TELECOMMUNICATION BACKGROUND

In telecommunication we will focus our attention on HOW information is transferred from one place to another over electronic channels. Information in the form of sound or visual images is processed into electrical signals by transducers. For example, a microphone is the transducer for converting a voice signal to an electronic signal. Further electronic processing can convert these signals into a digital format.
Once we have the signals in a suitable format the next job is to determine the best way for transmitting the information over long distances.

The next figure illustrates the basic idea of transmitting information and receiving the information on another end.

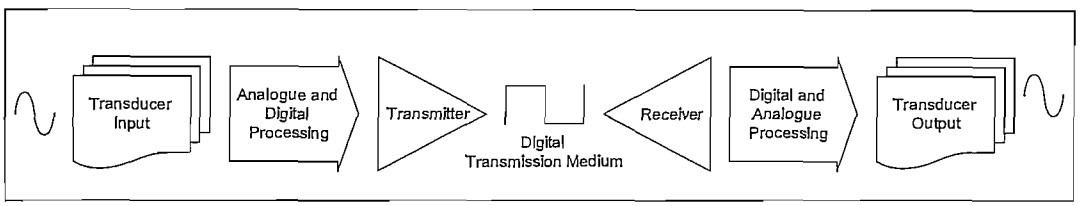


Figure 71: Basic Transmission and Receiving Model

Typical mediums used for transmitting information are:

1. Transmission lines
2. Optical Cable
3. Space (RF)

Distances and broadcast coverage involved usually result in vast energy losses. To overcome this problem very sensitive receiving and processing systems are required before the signal can be processed into the desired form for the user.

The main focus of this brief introduction will fall on RF (Radio frequency) systems. This is most probably the more complex of all transmission mediums but all the

techniques can be implemented and used for design on almost any other transmission system.

Most of the information being communicated over electronic networks falls into a frequency range below 4MHz. (Thus, the rate at which data is communicated.) The information is found in discrete and continuous form. However, the transmission facilities and circuits are preliminary analogue (meaning continuous) and can usually be characterized by radio frequency (RF) sinusoids.

We will work with frequencies below microwave frequencies (about 1000MHz). Designs for these frequencies can be realized by passive (lumped) components. For frequencies higher than microwave frequencies, design elements simply become too small, and transmission line-theory must be studied.

2.1 RESONANT FREQUENCY, CIRCUIT Q AND BANDWIDTH

Inductors store energy in magnetic fields rounding them. Capacitors store energy in the space between conductors. The energy is stored during one half of the ac cycle (signal) and returned to the circuit during the other half. Any energy lost during the cycle is associated with a *dissipative resistance* and gives rise to a quality factor, Q.

Definition:
The circuit Q is defined as the ratio of maximum energy stored to the amount lost per ac cycle.

The Q of a circuit is very important in electronic communications because it determines the 3dB bandwidth of resonant circuits. (Refer back to filter design and the 3dB point.)

Bandwidth of the overall system limits the amount of information that can be transmitted through the system but also, the amount of noise that can enter the system.

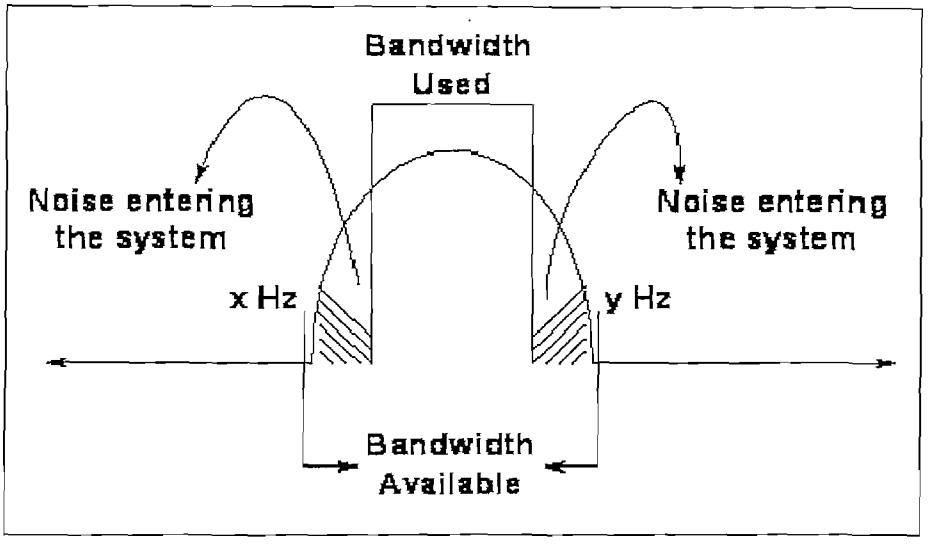


Figure 1(a) : Bandwidth utilization of a typical communication system

Definition:
Bandwidth of a system is calculated from Q and the resonant frequency of the circuit by:

$BW = \frac{f_o}{Q}$ or $B \geq \left\{ \frac{f_i}{\log_2 M} \right\}$, where M = number of phases in a constellation.

EXAMPLE 1:
Determine the BW and resonant frequency of the following circuit assuming that the Q of the circuit is 1.

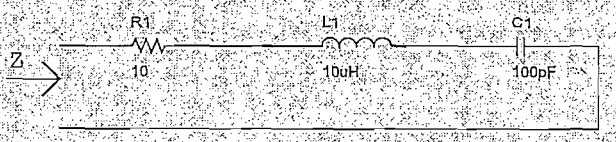


Figure 2 : Series RLC circuit

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

$$\omega_o = \frac{1}{\sqrt{LC}}$$

SOLUTION:
The Bandwidth of the circuit is 159.2kHz and the resonant frequency is 31.6M rad/s or 5.03MHz.

We are able to manipulate the Q of a circuit by changing the value of R or the combination of L/C with the following respect:

If different values of R are substituted in the series LRC circuit, the Q changes in accordance:

$$Q = \frac{X_L}{R}$$

$$Q = \frac{X_C}{R}$$

Where $X_L = \omega L$ and $X_C = \omega C$

The center frequency f_o does not change. If R remains constant but L increased and C decreased proportionately, the Q is also changed. Again the center frequency remains unchanged.

2.2 GAIN OF TRANSMISSION SYSTEM CIRCUITS

The gain of a system is computed as the product of the gain *or loss* of each individual stage of the system.

For convenience, the gain of individual stages of a system is converted to decibels (dB) to allow simple addition of the individual stage gains for determining the complete system gain. Converting a numerical gain value to a decibel value requires the use of logarithms.

The replacement of gain multiples by decibel-gain sums is based on the well established principle that the addition of the logarithms (logs) of two numbers is equivalent to the log of the product of the original two numbers.

$$\text{i.e } \log a + \log b = \log(a \times b)$$

The base of the logs that we use is 10.

Remember: $\log_{10} N = b$ **is equivalent to** $10^b = N$

If $10^x = N$ and $10^y = M$ then x and y are the logarithms of N and M, respectively. The sum of the logarithms is x + y, for which the antilog is computed as:

$$10^{x+y} = 10^x + 10^y = N \times M$$

Definition:

In electronics, the decibel is defined as the ratio of power or, for example, power gain, $\frac{p_o}{p_i}$. The logarithm base is 10 and, to minimize the occurrence of magnitudes less than unity, the logarithm is multiplied by 10. The definition of gain in decibels is:

$$gain\ in\ dB = 10\log_{10}\left(\frac{p_o}{p_i}\right) = A_p\,(dB)$$

2.3 POWER LEVELS (dBm and dB)

A very useful way to express power levels is to express them in decibels (dB) relative to some reference power level. Two of the most frequently used reference levels in communication systems are dBm which has a reference level of 1mW, and dBW (or more commonly known as just dB) which has a reference level of 1W.

The power level P is converted to dBm using:

$$P(dBm) = 10\log\left(\frac{P}{1mW}\right)$$

And to dB using:

$$P(dBW) = 10\log\left(\frac{P}{1W}\right)$$

The point of having the power expressed in dBm is that circuit gains and losses are usually expressed in dB and we can operate on the power levels using very simple arithmetic once the conversion has been calculated.

EXAMPLE 2:

(It is not necessary to understand example 2 at this stage but rather to see how power levels are calculated by making use of the dB scale.)

A receiver antenna has an output voltage of $10\mu V$ (the carrier only) when connected to a 50Ω receiver.

1. Determine the power level on the antenna in dB and dBm.
2. The receiver has 1 RF amplifier with 10dB of gain and a mixer with 6dB of conversion loss, followed by a multi-pole filter with 1dB of insertion loss. If available IF (Intermediate Frequency) amplifiers have 20dB of gain each, determine the number of IF amplifiers necessary to provide at least 0dBm (1mW) to the detector. (See Figure 2)
3. Sketch a block diagram of a superheterodyne receiver showing the power level, in dBm, at each point.

EXAMPLE 2 CONTINUED...

SOLUTION:

1. $$P = \frac{(10\times10^{-6}V)^2}{50\Omega} = 2\times10^{-12}W = (2pW)$$

$$p(dBW) = 10\log\left(\frac{2\times10^{-12}W}{1W}\right) = -117dB$$

$$p(dBm) = 10\log\left(\frac{2\times10^{-12}W}{10^{-3}W}\right) = -87dBm$$

2. **Remember the idea of converting to dBm and dB is this: We can add them together.** With a 10dB gain, the RF amplifier output is -87dBm + 10dB = -77dBm. Following 6dB of loss due to the mixer and 1dB of filter insertion loss in the pass-band, the IF input power is : $P(dBm) = -77dBm + (-7dB) = -84dBm$.

The IF system must provide an overall gain of $\frac{P_o}{P_i}$ or $P_o(dBm) - P_i(dBm) = 0$.

Thus the IF amplification stages need to provide $0dBm - (-84dBm) = 84dB$ of amplification.

3.

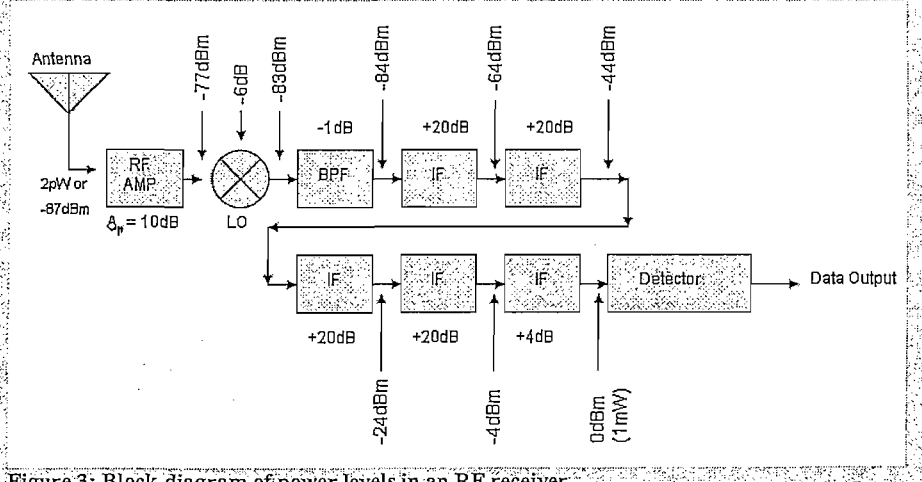


Figure 3: Block diagram of power levels in an RF receiver

BY DEFINITION:

POWER	POWER	Comment
dBm	**mW**	
0dBm	1	
+3dBm	2	3dB *above* 1mW
+10dBm	10	
+30dBm	1W (1000mW)	Also = 0dB (=0dBW)
-10dBm	0.1	40dB below 1W

Once you get used to working with dBm power levels, you really do catch on to the convenience of this technique and will quickly learn to recognize typical power levels, such as those in the table above.

APPENDIX D

Basic DSP Fundamentals

Sampling is the acquisition of a continuous signal at discrete time intervals and this is, most probably, the most fundamental concept in real-time signal processing. An example of a sampled analogue signal is shown in figure 41.

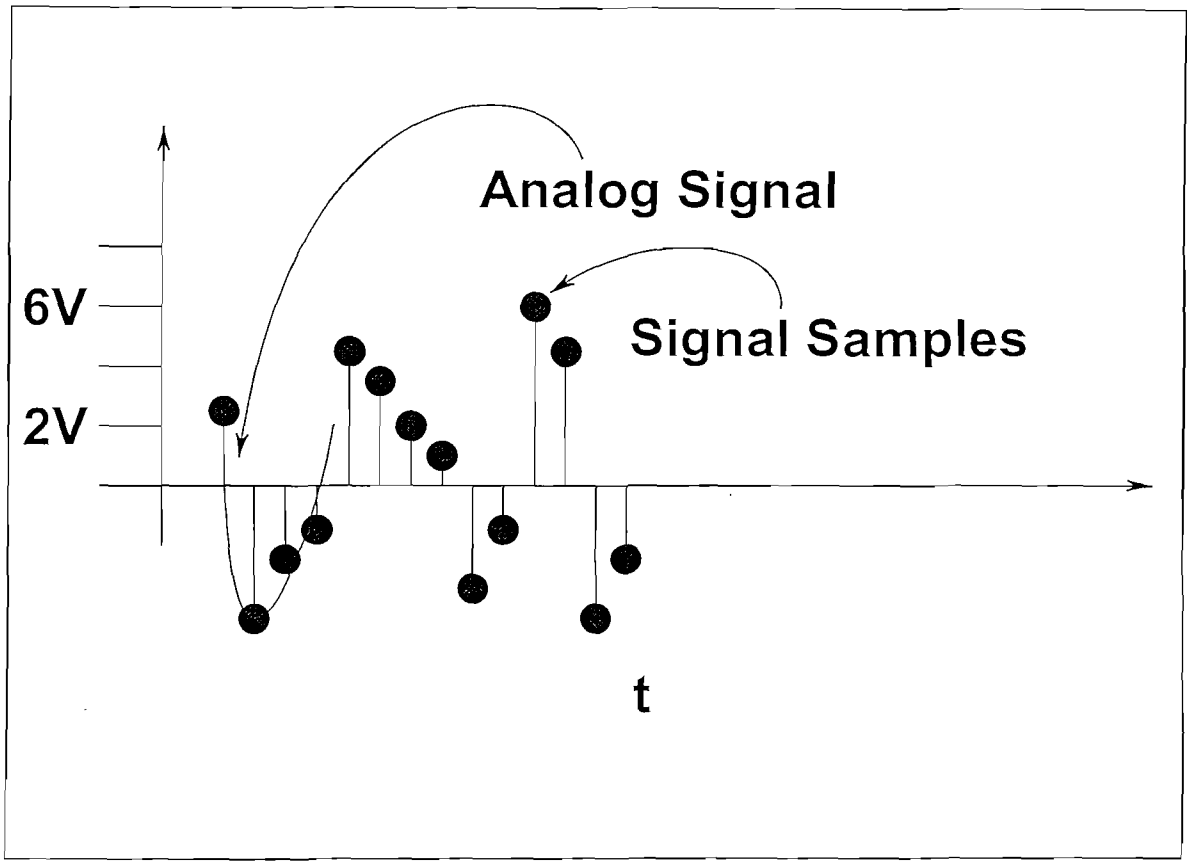


Figure 72: An Example of an Ideal Sampled Signal

For this discussion an intuitive presentation of the sampling theorem will be given, which specifies the rate at which an analogue signal should be sampled to ensure that all the relevant information contained in the signal is captured or retained by sampling, leading to the Nyquist criteria.

The Sampling Theorem reads as follows: **If the highest frequency component in a signal is f_{max}, then the signal should be sampled at the rate of at least $2f_{max}$ for the samples to describe the signal completely: $F_S \geq 2f_{max}$ where F_S is the sampling frequency.**[2][4][15][16]

Sampling at less than the rate specified by the sampling theorem leads to a folding over or *aliasing* of *image* frequencies into the desired frequency band so that the original signal cannot be recovered if it was to be converted back to an analogue signal.[15] An important aspect about digital signals is that the signal often contains significant energy outside the highest frequency of interest and contains white noise, which invariably has a wide bandwidth. Take for example, telephone signals. The highest frequency of interest is roughly around 3.4kHz, but speech signals may extend far beyond 10kHz. Thus, the sampling theorem will be violated if we do not remove the unwanted noise or signals outside the band of interest. In practice, this is achieved by first passing the signal through an analogue anti-aliasing filter. This is what was achieved by making use of the Class II Chebyshev band-pass filter implemented after the I.A. Refer back to figure 20.

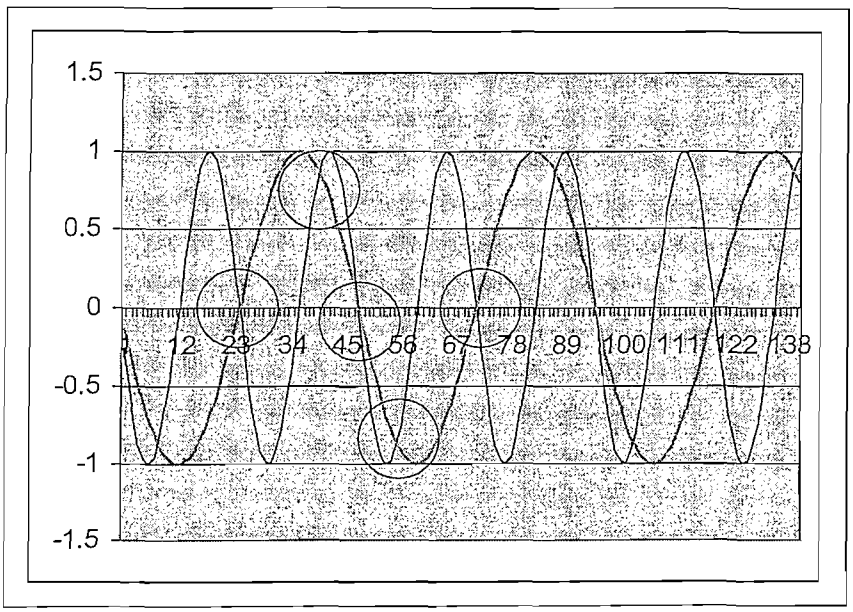
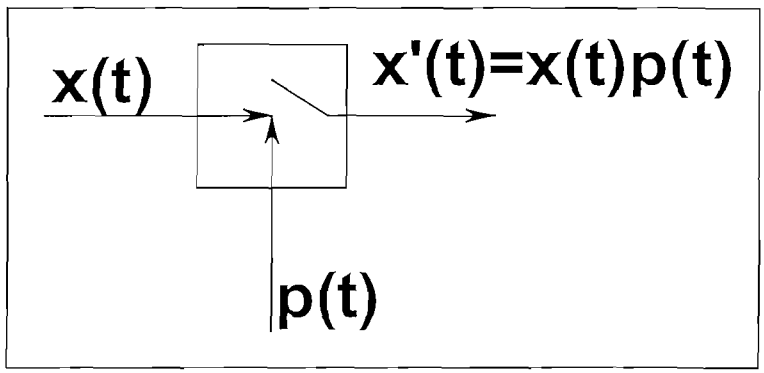
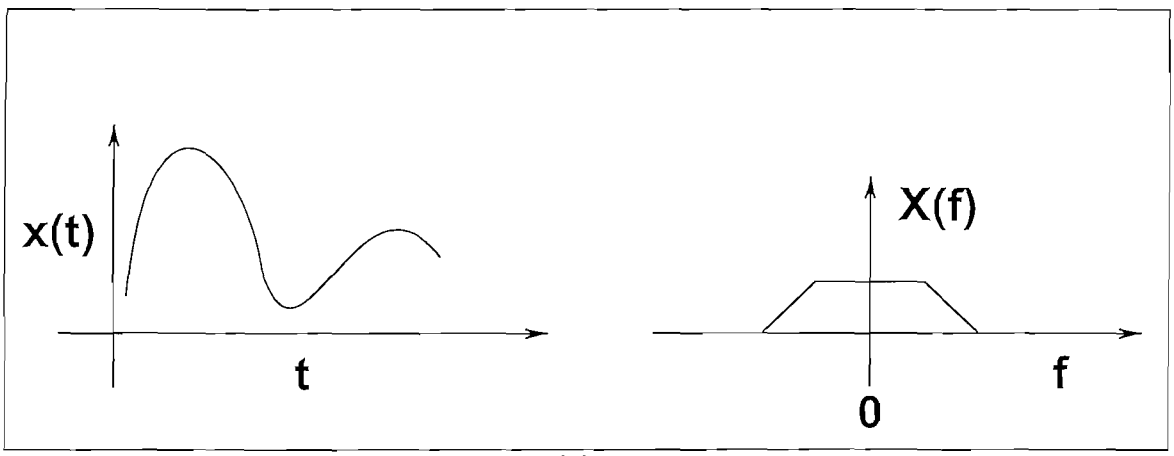


Figure 73: An Example of aliasing in the time domain

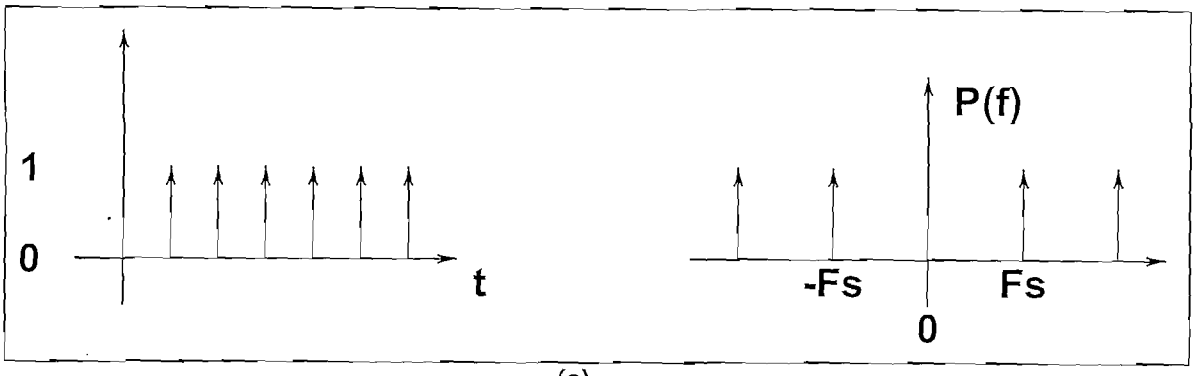
Depicted in figure 68 above is an example of aliasing in the time domain. Notice that the two signals have the same values at the sampling points indicated, although their frequencies are totally different. To put it simply, suppose we sampled a time domain signal at intervals of T seconds, that is, a sampling frequency of $\frac{1}{T}Hz$. It can be seen from figure 68 that another frequency component with the same set of samples as the original signal exists. Thus the frequency components can easily be mistaken for the lower frequency component and this is what aliasing is all about.



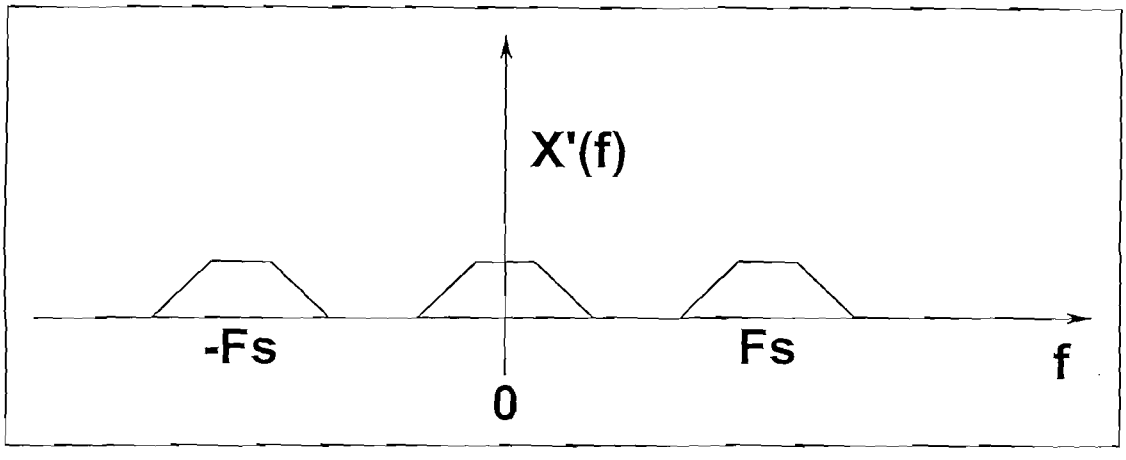
(a)



(b)



(c)



(d)

Figure 74: Time and Frequency Domain Representations of the Sampling Process

Figure 69 shows the sampling process. This is a process which can be regarded as the multiplication of an analogue signal $x(t)$ by a sampling function, $p(t)$, (Figure 69 (a)) which consists of pulses of unit amplitudes, width dt and period T. The spectra of $x(t)$, $p(t)$ and their product is also shown in figure 69 (b). Note that $X'(f)$ is the convolution of $X(f)$ and $P(f)$. Basics in signal processing, teaches that multiplication in the time domain is equivalent to convolution in the frequency domain. (Refer to any good textbook covering the basic topics in digital signal processing for a more elaborated discussion on the latter two topics.)

When taking a look at figure 69(d), the following should be kept in mind:

The spectrum is the same as the original spectrum (eg. figure 69(a)), but repeats at multiples of the sampling frequency, Fs. The higher order components which are centred on the multiples of Fs are referred to as image frequencies. Furthermore, if the sampling frequency, Fs, is not sufficiently high the image frequencies centred on Fs, for example, will fold over or alias into the base band frequency.[15] Look at figure 70 on the next page for a graphical representation. In which case, the information of the desired signal is indistinguishable from its image in the fold-over region. Also, the overlap or aliasing occurs about the point F_N, that is, half the sampling frequency.[16] This frequency point, F_N, is variously called the folding over frequency or the Nyquist frequency.

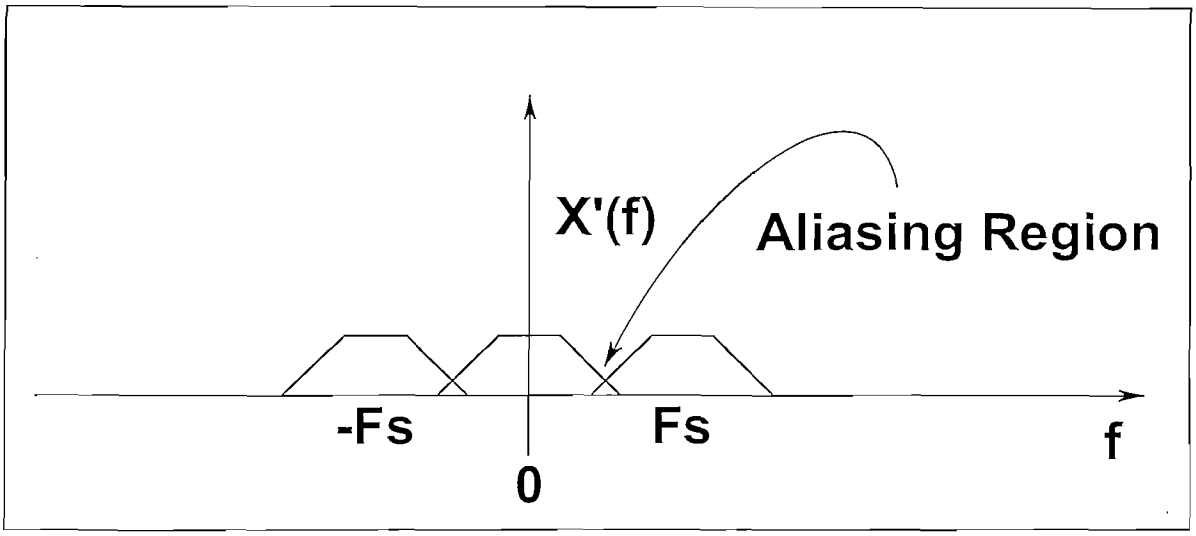
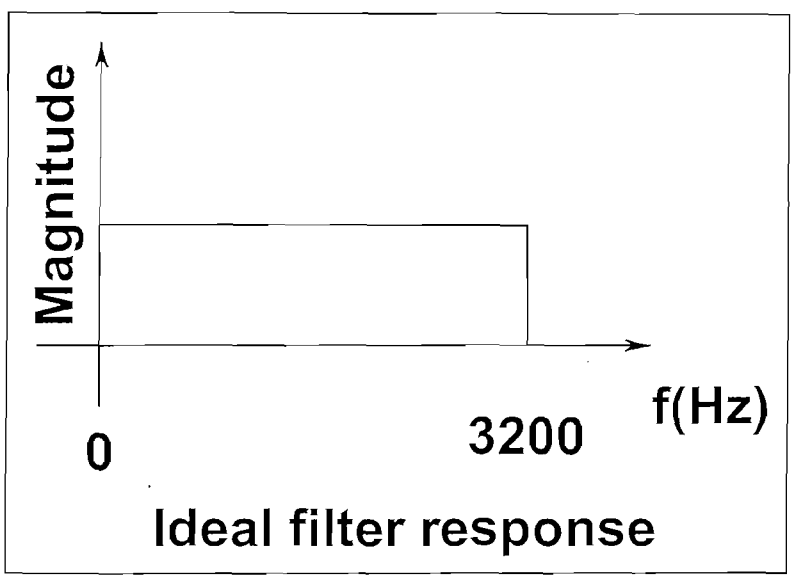


Figure 75: Spectrum of an Under-sampled Signal Showing Aliasing.

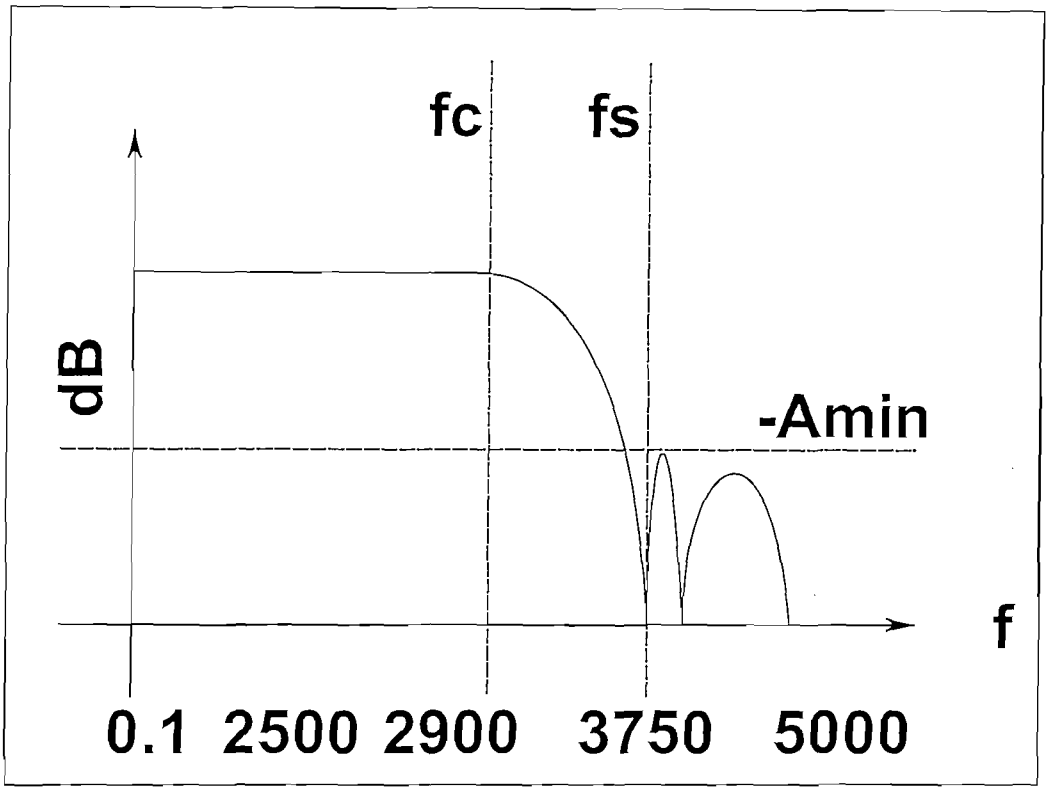
In practice, aliasing is always present because of the ever so present noise and signal energy outside the band of interest. The problem is deciding on an acceptable level of aliasing and designing the anti-aliasing filter.

To reduce the effect of aliasing, sharp cut-off anti-aliasing filters are usually implemented in the analogue domain to band-limit the signal.[15] Together with this the sampling frequency is increased as to achieve a wider separation between the signal and the image spectra.

Ideally, the anti-aliasing filter should remove all frequency components above the fold-over frequency, that is, it should have a frequency response similar to that of figure 71(a). A more practical response however is depicted in figure 71(b). Here f_c and f_s are the cut-off and stop-band frequencies, respectively. It is worthwhile to note from figure 71 that, the practical response introduces an amplitude distortion into the signal as it is not flat in the pass-band. Also, any components greater than f_s will be attenuated by $A_{\min}$, a minimum attenuation, but those between f_c and f_s, the transition-band, will have their amplitudes reduced monotonically. This can be seen in figure 71(b).



(a)



(b)

Figure 76: Ideal and Practical Frequency Response of an Anti-Aliasing Filter

The anti-aliasing filter should provide sufficient attenuation at frequencies above the Nyquist frequency, F_N, this is because of the non-ideal response of practical filters. For practicality, the effective Nyquist frequency is usually taken as f_s. [15]

When specifying the anti-aliasing filter it is useful to take the ADC resolution requirements into account. Thus a filter would be designed to attenuate the frequencies above the Nyquist frequency to a level not detectable by the ADC, for example to less than the quantization noise level. Thus, for a system using a B-bit linear ADC, the minimum stop-band attenuation of the filter would typically be[15][16]:

$$A_{\min} = 20\log\left(\sqrt{1.5}\times 2^{B}\right) \qquad (1.36)$$

where B is the number of bits in the ADC.

The use of an analogue filter at the front end of a DSP system also introduces other constraints, such as phase distortion. In most cases, the steeper the roll-off (in other words, the narrower the transition band) the worse the phase distortion will be. This means that it will be more difficult to achieve a good match in amplitude in these regions. However, the use of steep roll-off filters makes way for cheaper analogue to digital converters as well as slower sampling rates.

APPENDIX E

International Patent application

Beste Dawie en Kollegas

SUID-AFRIKAANSE PATENT AANSOEKNOMMER 2006/07480 GETITELD: "REAL TIME MONITORING SYSTEM AND METHOD OF ELECTRICAL SIGNALS RELATING TO AN ATHLETE'S HEART ACTING" IN DIE NAAM VAN NOORDWES-UNIVERSITEIT

Ons bevestig en herinner u vriendelik daaraan dat hierdie patent op 7 September 2006 deur ons korrespondente Mnre DM Kisch Ing van Pretoria / Sandton as 'n voorlopige aansoek ingedien is.

Ons moet nou voor of op 6 September 2007, óf 'n finale patent in Suid-Afrika indien, óf indien ons internasionaal met die patentering wil voortgaan 'n sogenaamde PCT-aansoek in Geneva Switzerland indien.

Ek sou graag persoonlik met u die detail en verdere moontlike stappe bespreek in plaas van 'n lang brief en 'n poging om die prosedures te verduidelik.

Ons sal ten minste teen die einde van Julie 2007 opdrag aan DM Kisch moet gee om óf 'n aansoek finaal in Suid-Afrika in te doen, óf as ons internasionaal wil gaan, met die PCT-aansoek voort te gaan. Alle nuwe toetse en inligting wat u in die tussentyd bekom het sal bygewerk moet word en alle resultate en stawing van u bewerings, soveel as moontlik, wat in die voorlopige patent gemaak is, sal bygewerk moet word.

Indien u beoog om met 'n PCT-aansoek voort te gaan sal dit baie goed wees as 'n besigheidsplan ook voorberei kan word en kan Dr Rudi van der Walt uiters kundige en praktiese advies en ervaring bydra. U kan hom skakel as Direkteur van die Institusionele Innovasie kantoor. Ons sal hom ook baie graag by enige afspraak wil betrek.

Ons sien daarna uit om van u te vernеem en bied hiermee ons volle samewerking en hulp aan om die Universiteit se intellektuele eiendomsregportefeulje verder uit te bou. Ons verneem graag so spoedig moontlik van u en kan u deur Me Willemien Botha van ons kantoor met myself en Dr Rudi van der Walt 'n afspraak skeduleer. Ons is selfs ook meer as bereid om na u kantore te kom en selfs 'n koppie koffie by Wiesenhof saam met u te geniet.

Vriendelike groete
FRANS KRUGER
REGSDIENSTE
INSTITUSIONELE HOOFKANTOOR
NOORDWES-UNIVERSITEIT

APPENDIX F

The driven-right-leg (DRL) common mode driver feedback approach.

The goal of this description is to shed some light on the DRL approach in the presence of an I.A, in order to improve the common mode performance of the I.A used to acquire an ECG signal. The implementation presented here is termed a *driven right leg* amplifier as an inverted copy of the common mode voltages is fed back to the body via the right leg reference connection.

Usually a classical three op-amp approach for obtaining the ECG is followed. As was described in part II of this dissertation, the usual technique for overcoming the interference of the common mode signal is to employ a differential amplifier. Such an amplifier rejects the common mode interference and yet amplifies the small differential bio-potential signal obtained from the human body. Furthermore, as was described in part II of this dissertation, one of the limitations of the so called two-stage differential amplifier is its dependence on resistor matching.

An improved version of a differential amplifier was shown ion page 44 in figure 12. This circuit comprises of two stages and is commonly termed a classical instrumentation amplifier as was described in that section. This topography overcomes many of the limitations of the single and dual op amp solutions. Notably, the first stage provides high differential input impedances that minimize the effect of source impedance mis-match. In addition this stage also provides some differential gain. The second stage is identical to that of a simple differential amplifier. However, the inclusion of differential gain *ahead* of this stage gives rise o an overall CMRR improvement.

The overall differential gain A_d, of this amplifier is the combined product of the differential gains of each stage, and can be expressed as follows:

$$A_d = \left(1 + \frac{R_1 + R_1^1}{R_g}\right)\left(\frac{R_3}{R_2}\right)$$

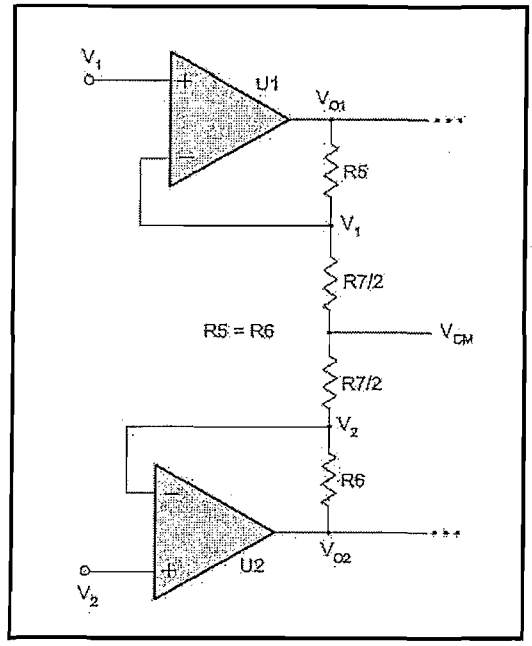
It can be shown that providing the input op-amps, $U_1 \; and \; U_2$, are considered to have identical characteristics, then overall CMRR of this 2-stage amplifier is given as:

$$CMRR = CMRR_{2nd}\left(1 + \frac{R_1 + R_1^1}{R_g}\right)$$

It should be noted that the overall CMRR improvement factor is the differential gain of the 1st stage. However it is important to realise that the overall CMRR is still limited by the resistor matching of the 2nd stage.

Now, using negative feedback, is one more method of improving the CMRR further. If the common mode signal, V_{cm}, was known, then it should be possible to subtract this signal from the input to the amplifier, leaving only the differential signal, V_d. If no common mode signal is present at the input of the amplifier, then the effective CMRR of the differential amplifier becomes infinite. However, this technique relies heavily on the determination of the common mode voltage.

Fortunately, the symmetrical nature of the classical I.A provides a simple method of accessing this voltage. Providing again, that R_1 is equal to R_1^1, the common mode voltage can be accessed by splitting R_g into two equal resistors. Refer to the following illustration.



To use this voltage, V_{cm}, to cancel the common mode voltage on the body, an additional op amp is employed to *invert* the signal. Adding this inverted signal to the body potential will then achieve the desired ***negative*** feedback result. In this way the body is used as the summing junction in the feedback system. the addition of the inverted common mode signal to the body is conveniently achieved through the reference electrode connection.

APPENDIX G

DVD Video and full colour pictures for Visual reference of system operation.

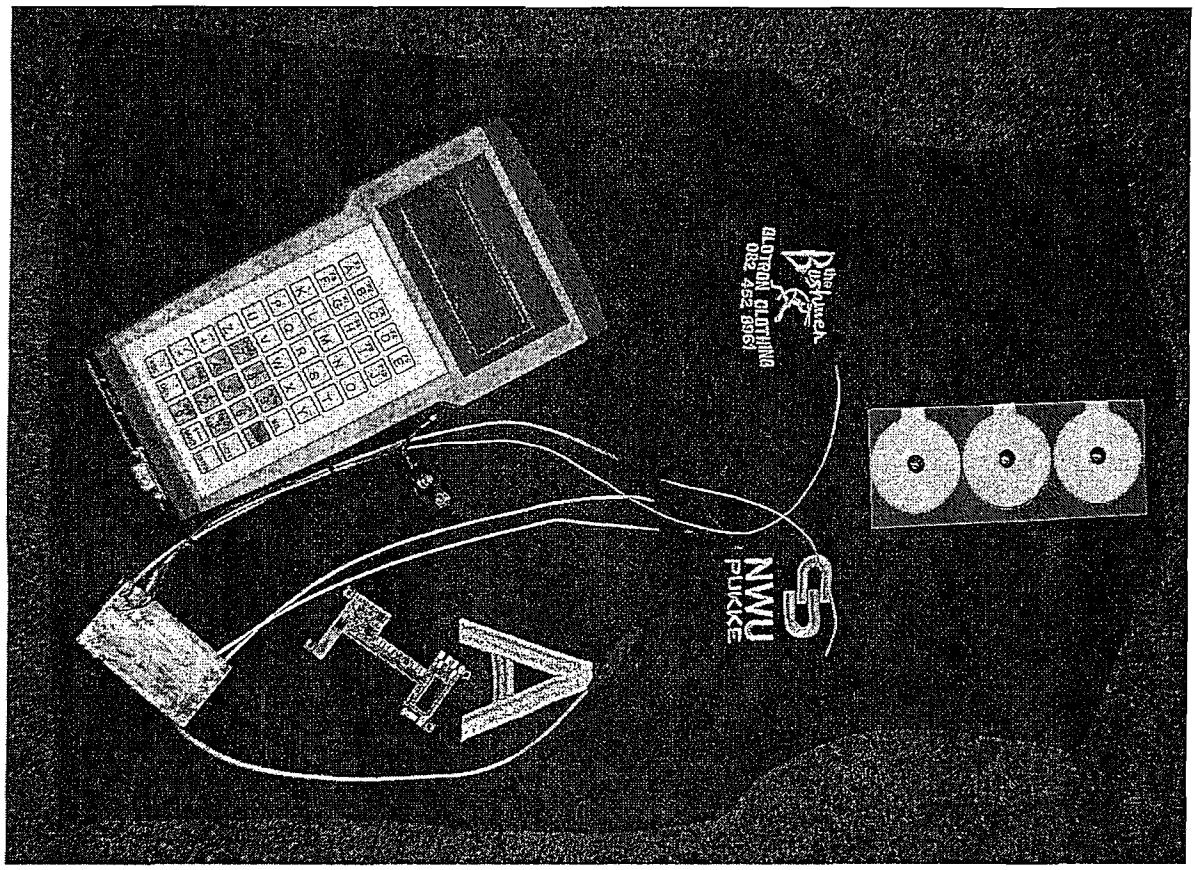


Figure 77: Hand Held Computing Unit, Bare ECG monitor, Molded ECG monitor, Special ECG Electrodes & Suggested Sports Vest for Testing

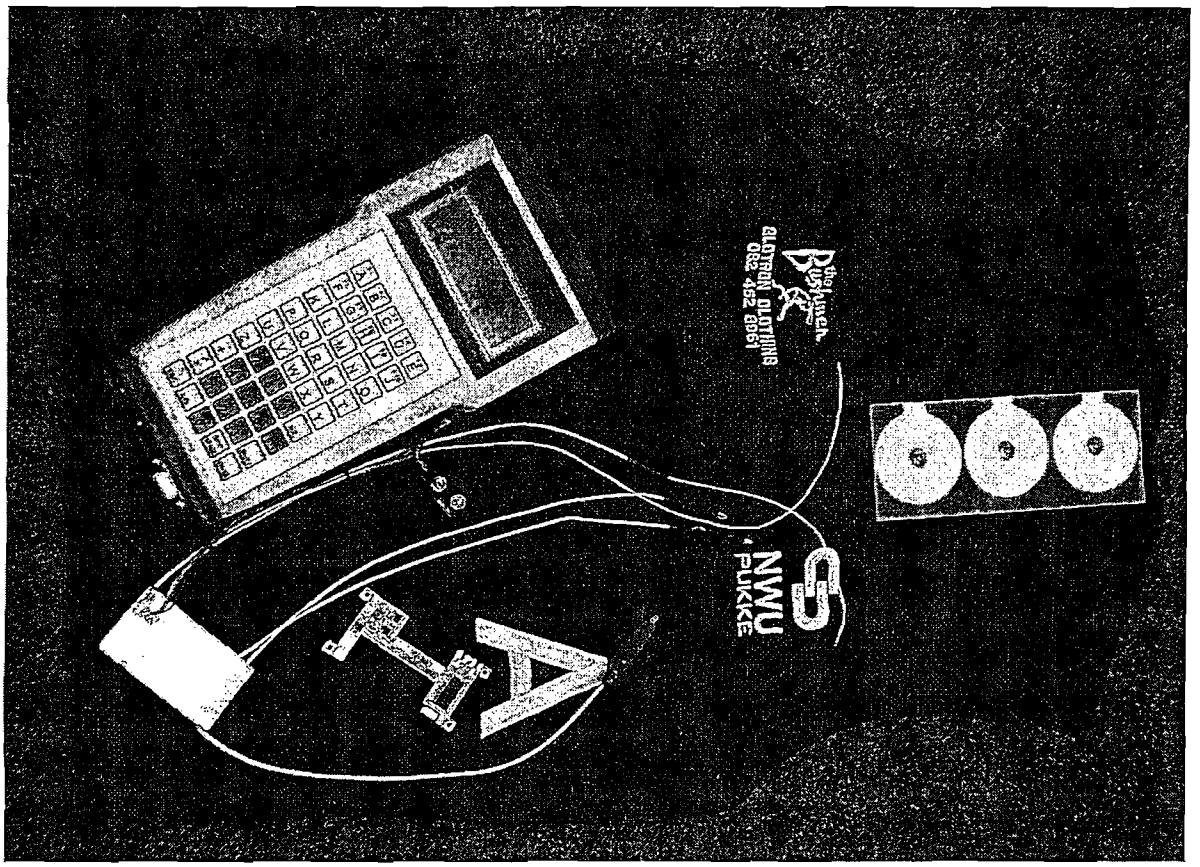


Figure 78: Hand Held Computing Unit, Bare ECG monitor, Molded ECG monitor, Special ECG Electrodes & Suggested Sports Vest for Testing

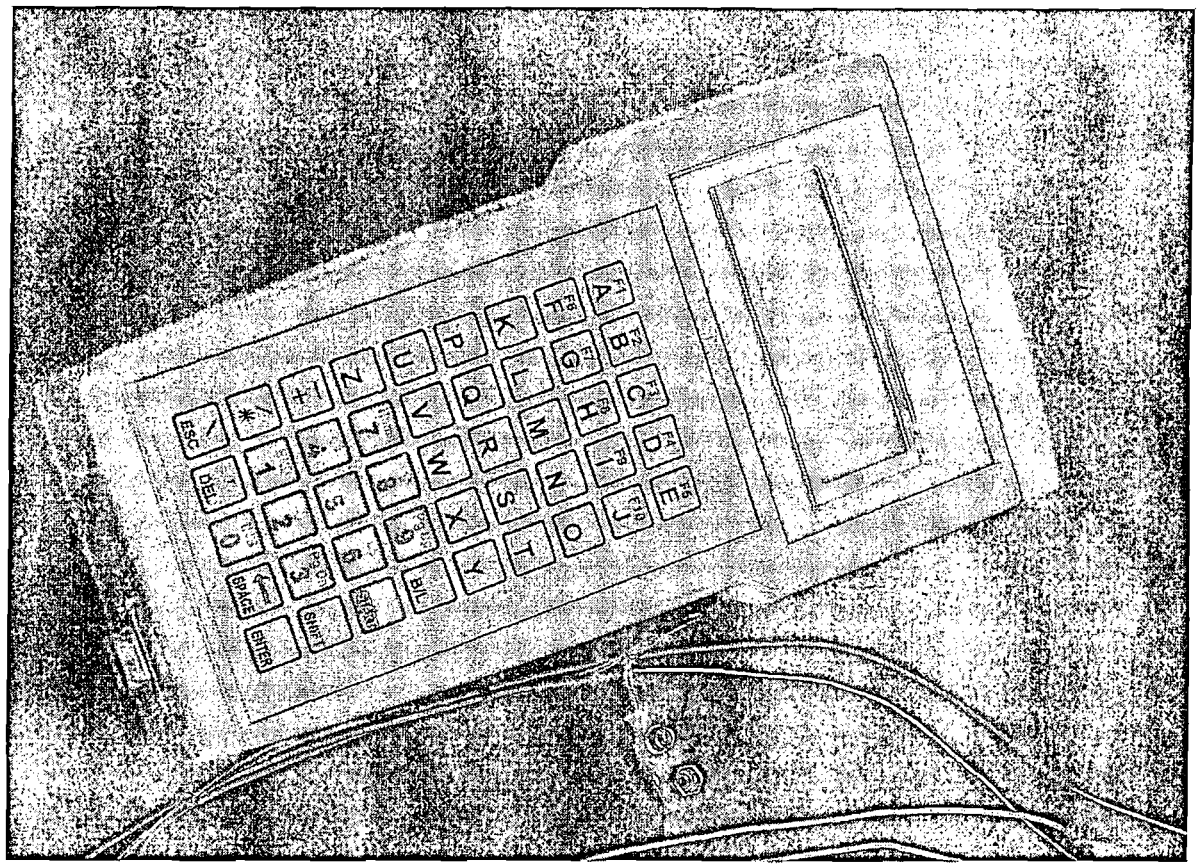


Figure 79: Close-Up Picture of Hand-Held Computing Unit Showing the LCD, Membrane Switch Technology Keypad, RS232 i/o Interface and Unit Size

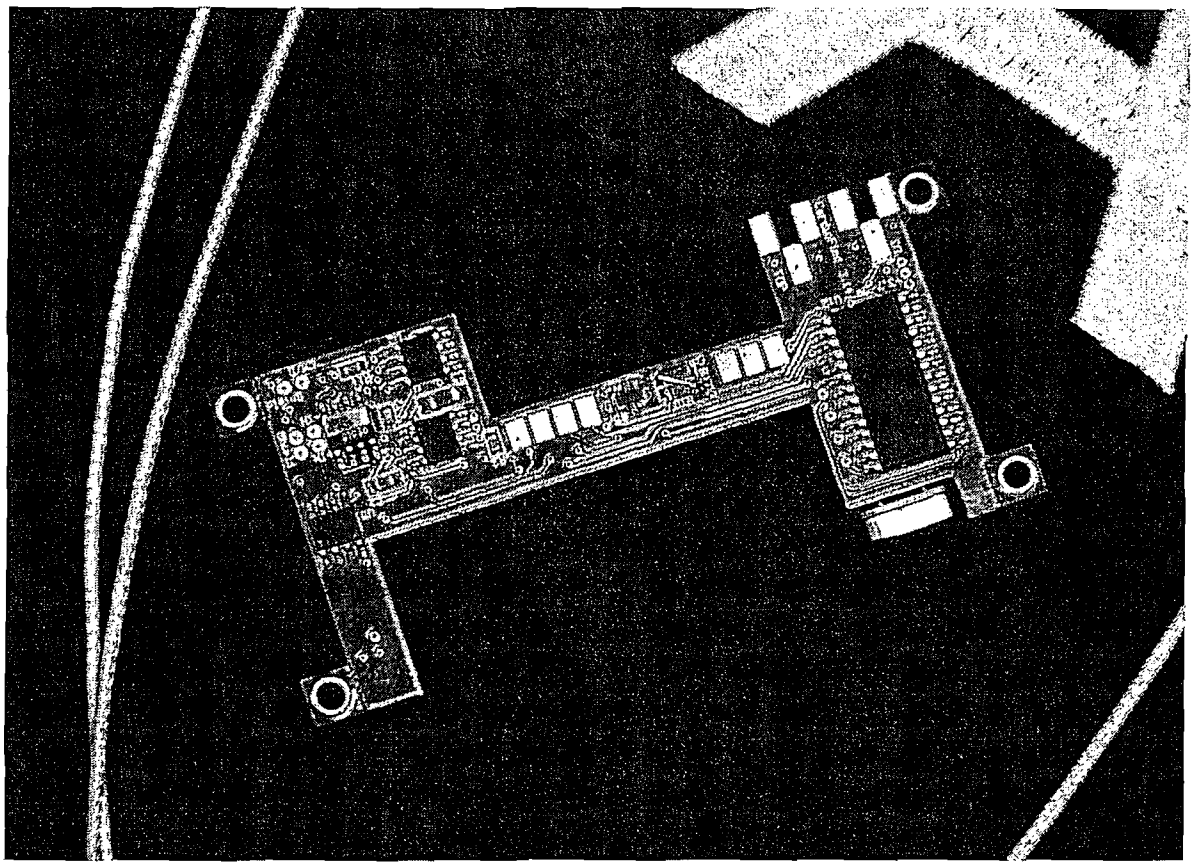


Figure 80: Close-Up Picture of Bare ECG and Heart Rate Monitor as Developed During this Research (RF Transmitter & Receiver not Included)

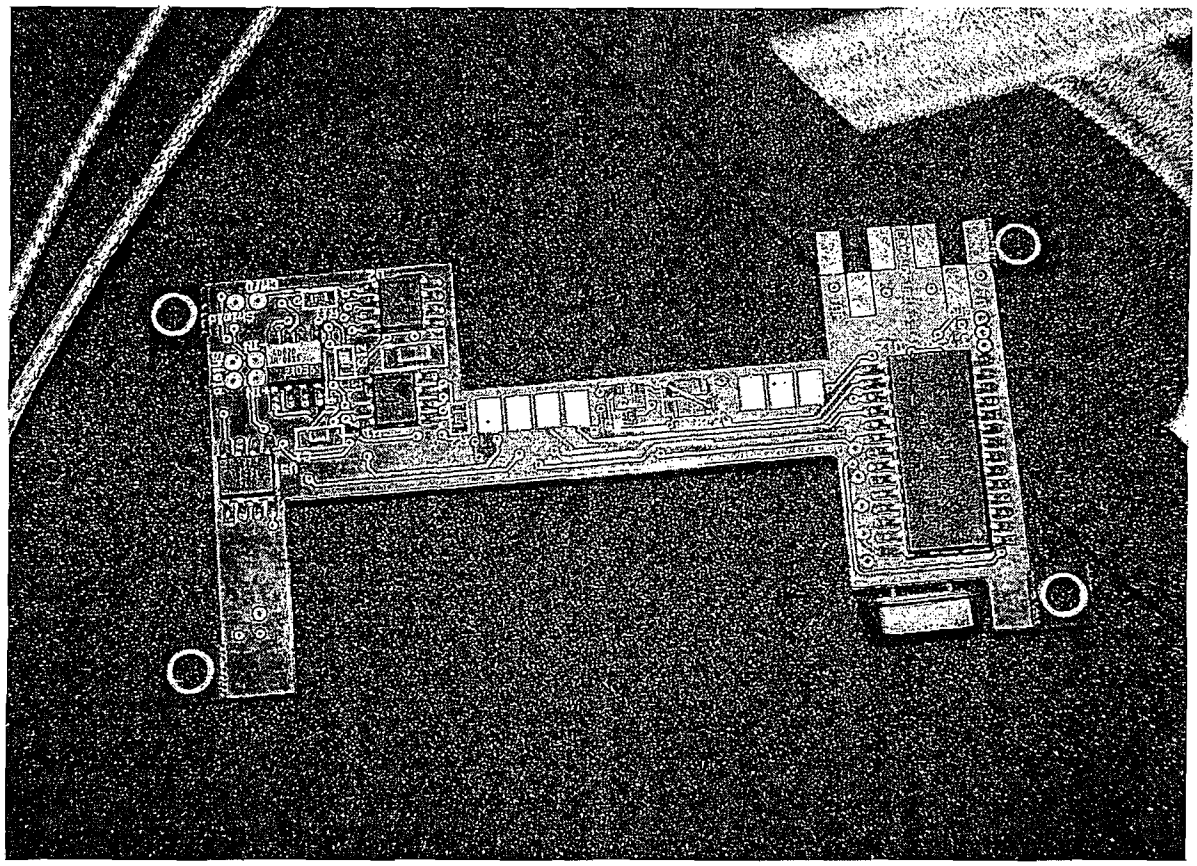


Figure 81: Close-Up Picture of Bare ECG and Heart Rate Monitor as Developed During this Research (RF Transmitter & Receiver not Included)

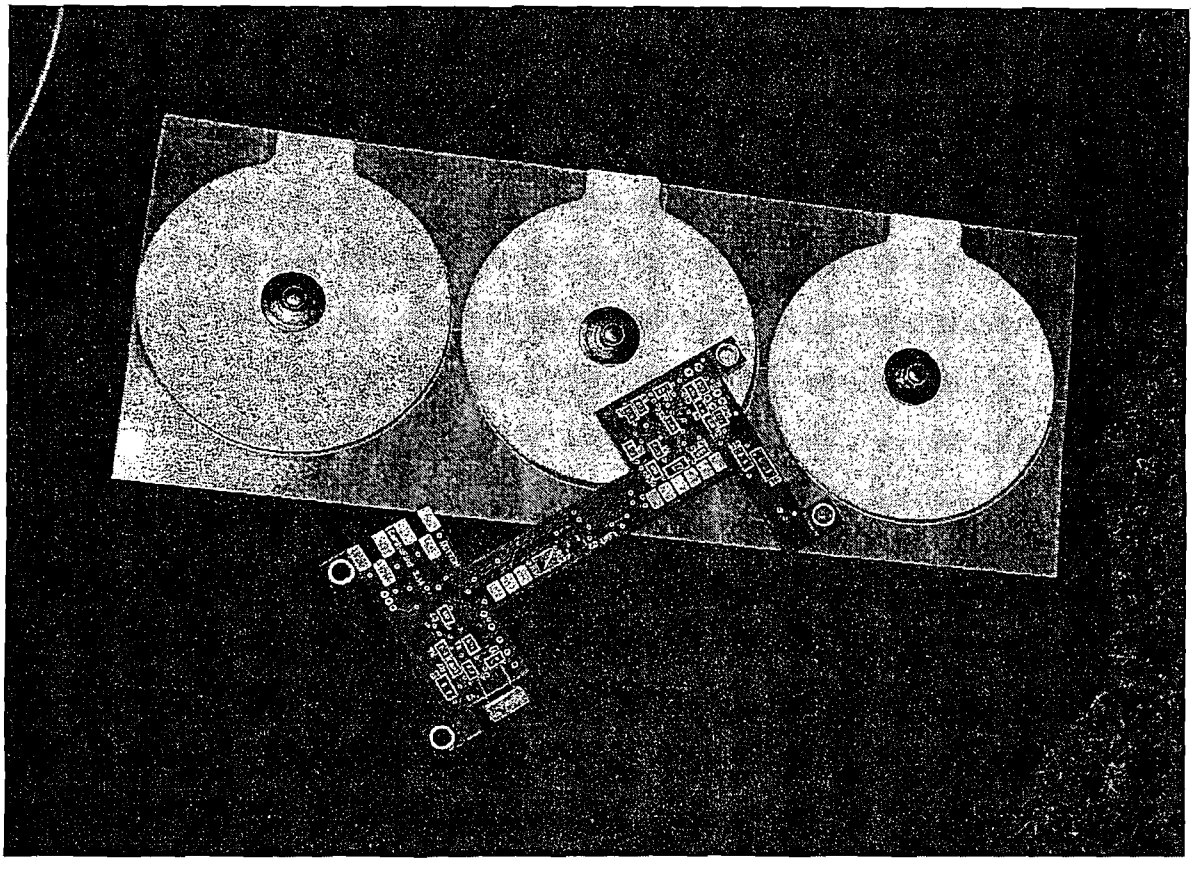


Figure 82: Close-Up Picture of The Bare ECG and Heart Rate Monitor Including the Specially Developed Foam ECG Electrodes

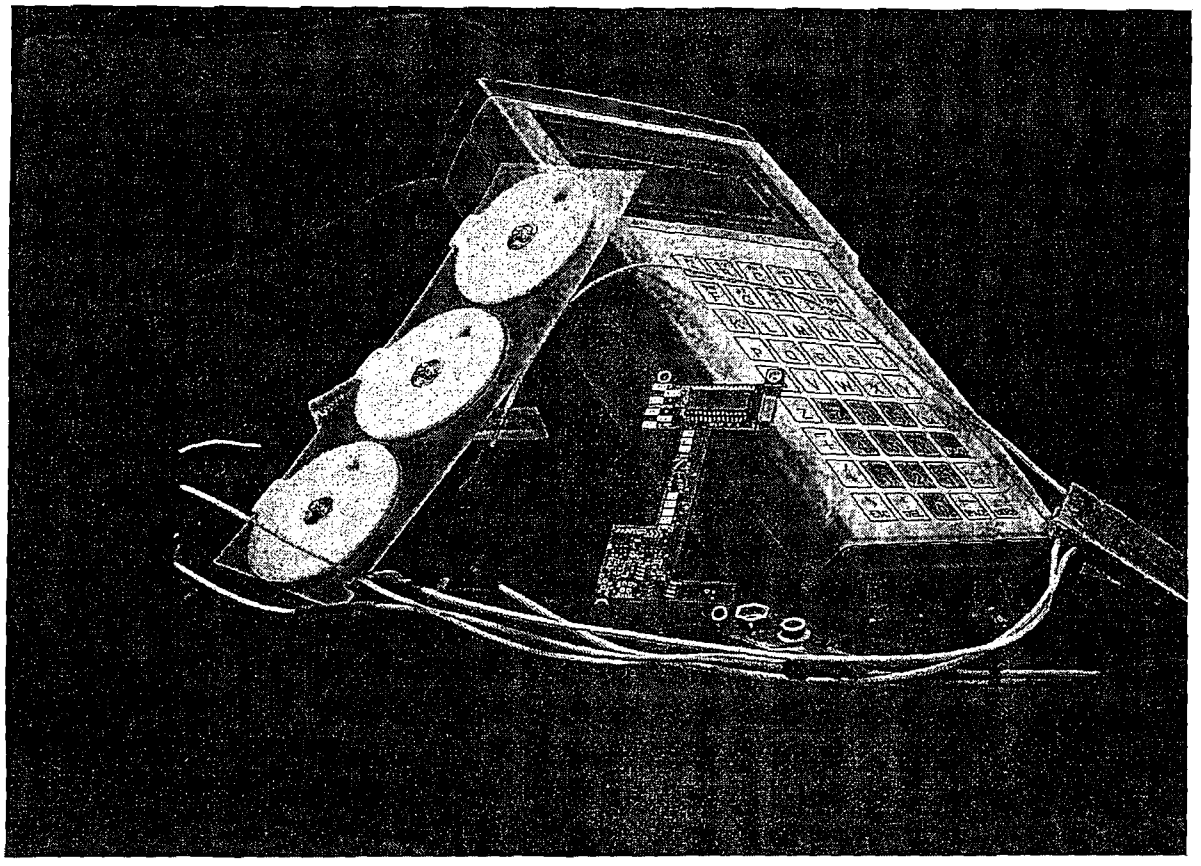


Figure 83: Combination Picture of all the Units Developed. (Excluding the RF Data Relay Units.)

*Please note: For a visual representation of the RF Data Relay Units, please refer to the DVD at the end of this appendix.

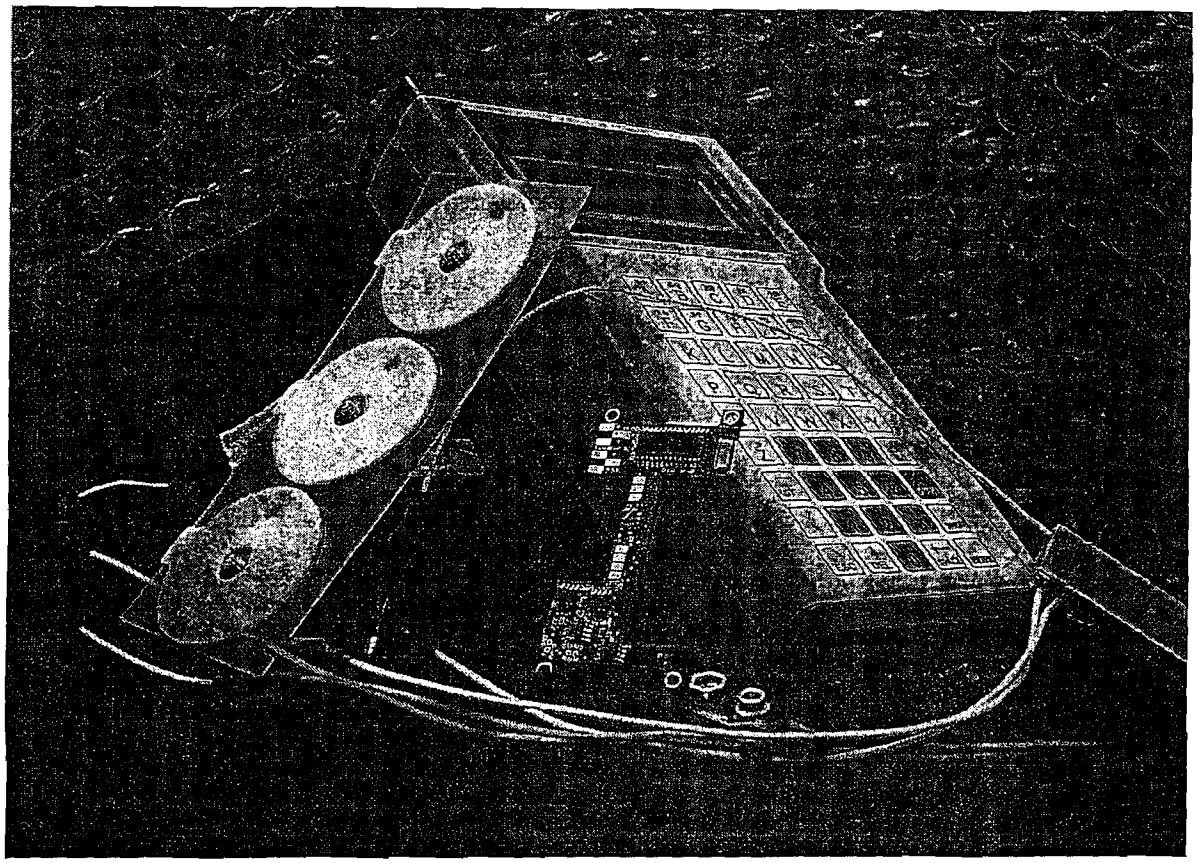


Figure 84: Combination Picture of all the Units Developed. (Excluding the RF Data Relay Units.)

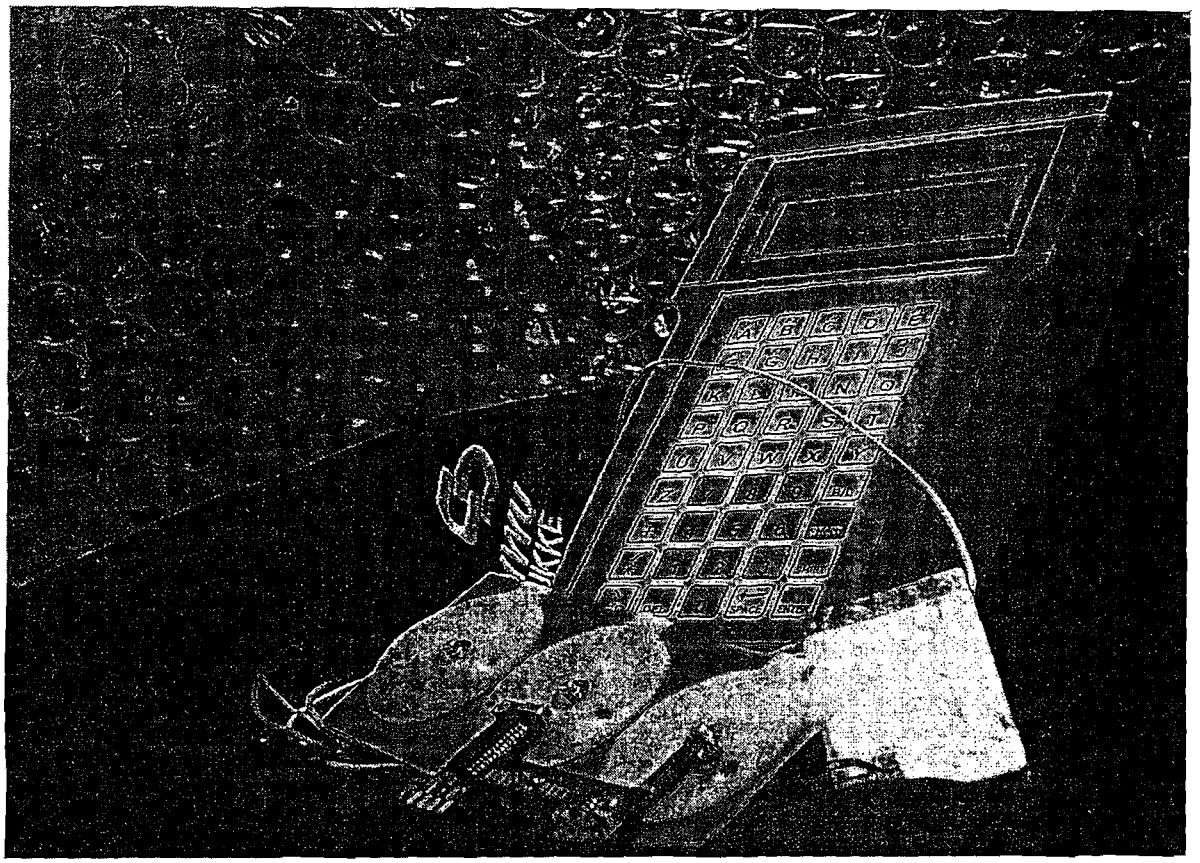


Figure 85: Combination Picture of all the Units Developed. (Excluding the RF Data Relay Units.)

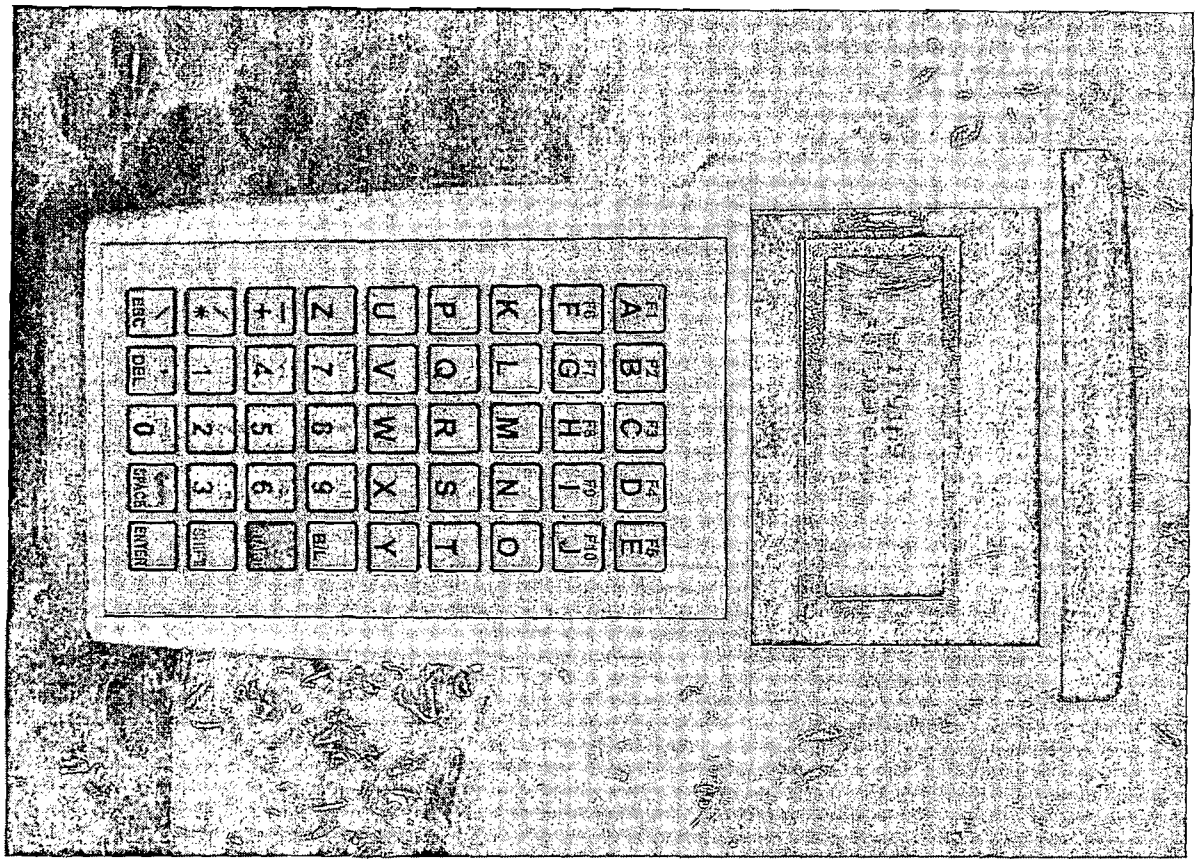


Figure 86: Close-Up Picture of the Operating Hand-Held Computing Unit