A high precision driver for an eddy current displacement sensor

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DECLARATION

I hereby declare that all the material incorporated in this thesis is my own original unaided work, except where specific reference is made by name or in the form of a numbered reference. The work herein has not been submitted for a degree at another university.

Signed: _____

Hester E. Niemann

Summary

This dissertation presents the design and development of a high precision driver for an eddy current displacement sensor. The project was initiated to supplement the development of a low-cost PCB eddy current displacement sensor for active magnetic bearings (AMBs). The sensor driver will be implemented in AMB systems that will be used in various high-speed applications.

The sensor driver is required to drive an eddy current PCB sensor, condition the output signals from the sensor, and send the conditioned position signals to an embedded digital controller. Circuit board design and development therefore constitute the main focus of this project.

Research on the defining concepts of the project was imperative in gaining the necessary understanding of the project. AMB systems and the sensors used in these systems were investigated first. The eddy-current type sensor used in this project, as well as the PCB sensor technology used were also researched. As analogue design constituted a main aspect of this project, the concepts of signal conditioning and sensor characteristics had to be comprehended.

The sensor driver consists of several sub-systems, including a sensor excitation circuit to drive the sensor, a signal conditioning circuit to condition the output signals of the sensor, and a digital processing circuit for further processing of the position signals. A conceptual design was performed for each of these sub-systems, followed by a detail design, in which the conceptual designs of the sub-systems were realized. All the sub-systems were then integrated, and lastly evaluated.

The evaluation of the sensor driver system included verification and validation of the system. The sensor driver design was verified, while the final sensor driver board was validated with regards to its specifications. Additional circuit characteristics such as signal-to-noise-ratio, sensitivity and resolution were also determined in order to characterize the sensor driver system.

The overall outcome of the sensor driver project was successful, with all the characteristics of the sensor adhering to the requirements. It was determined that the sensor driver has a signal to noise ratio of 54 dB, a linearity of 9 %, a sensitivity of 26 .4 V/mm, and a resolution of 792.5 nm.

Recommendations are made with regards to the sensor cables, heat distribution, and the low-pass filter on the field programmable gate array (FPGA). Future work will mainly focus on implementation of the sensor driver on a test bench and implementation of the linearization algorithm. Additional future work includes a study on EMC effects on the system and especially the cables, and further firmware enhancements of the sensor driver. These include input signal testing and temperature compensation. An investigation on the required excitation current for optimal sensor operation should also be done.

Foreword

I would like to thank my wonderful husband André for all his love, support and guidance, without you I would never have made it this far. To my family, your love, encouragement and understanding means the world to me.

I want to thank my supervisor Prof. George van Schoor for his guidance and support, and for giving me the opportunity to further myself not only academically, but also as a human being. A big thank you to M-Tech Industrial, who made this project available and for their funding through THRIP.

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Lastly, I would like to thank and give praise to the Lord my Shepherd, to whom I will always be grateful for all His endless blessings. Without Him nothing would be possible.

“Die Here is my herder, ek kom niks kort nie. Hy laat my rus in groen weivelde. Hy bring my by waters waar daar vrede is. Hy gee my nuwe krag.”

Psalm 23:1 -3

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List of abbreviations

AC	Alternating Current
ADC	Analogue-to-Digital Converter
ADES	Active magnetic bearing and Driver Electronics System
AMB	Active Magnetic Bearing
BPF	Band-Pass Filter
BPI	Byte Peripheral Interface
CLB	Configurable Logic Blocks
DAC	Digital-to-Analogue Converter
DCM	Digital Clock Management
DDS	Direct Digital Synthesis
DNL	Differential Non-Linearity
DPR	Dual-Port Ram
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
FPU	Floating-Point Unit

FSO	Full Scale Output
FSR	Full Signal Range
IC	Integrated Circuit
JTAG	Joint Test Action Group
LDO	Low Drop-Out
LPF	Low-Pass Filter
NCO	Numerically Controlled Oscillator
PBMR	Pebble Bed Modular Reactor
PCB	Printed Circuit Board
PROM	Programmable Read-Only Memory
PWG	Programmable Waveform Generator
RAM	Random Access Memory
RMS	Root Mean Square
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TSP	Twisted Shielded Pair
UART	Universal Asynchronous Receiver / Transmitter
USB	Universal Serial Bus
VHDL	Very high speed integrated circuit Hardware Description Language

List of symbols

E_o	Output error offset
A	Gain (dB)
E	Electrical field
S	Sensitivity
Z	Impedance
I	Current
L	Inductance
R	Resistance
V	Voltage
X	Reactance
f	Frequency
t	Time
λ	Wavelength
τ	Time constant
v	Signal velocity

Chapter 1

Introduction

This chapter provides the background information on the area of application for the sensor driver project, namely active magnetic bearings (AMBs) as well as the sensors used in AMB systems. The problem statement is presented, followed by the issues to be addressed and research methodology. This first chapter is concluded with a chapter summary for the rest of this dissertation.

1.1 Preface

The aim of this project is to design and develop a high precision driver for an eddy current displacement sensor. The sensor used in this project is a PCB eddy current sensor [7], developed as part of a low-cost sensor system. The sensor driver is necessary in order to complete the sensor system as a whole. The completed sensor system will be used in active magnetic bearing (AMB) systems within the faculty for research purposes, as well as for possible industrial implementation. This chapter will commence with a discussion on AMB systems and the types of sensors used in AMB systems.

1.1.1 Active magnetic bearings

Bearings are normally used to support or restrain a rotating or moving mechanical part. This inherently means that friction plays a large role in the performance of a bearing. In the effort to reduce friction and improve bearing performance, lubricants such as oil are required. In environments like nuclear power stations, however, bearing lubricants can become radio-active. Since the bearings have to be replaced relatively frequently due to wear and tear, these contaminated bearings pose a major health- and environmental risk. The need for magnetic bearings stemmed forth from these and other critical shortcomings posed by traditional roller bearings. Research into the field of AMBs has increased tremendously in the past decade. This is largely due to the development of the pebble bed modular reactor (PBMR), originating from

the increasing need for cleaner, safer and more effective power stations [1]. AMBs are based on the central physical concept of electromagnetism; suspending a rotor or other ferromagnetic body by actively controlling the electromagnetic forces acting on it. This not only implies contact-free suspension, but also other advantages like increased reliability, low maintenance and losses, increased speeds in extreme environments, and no lubrication required [2].

The main elements of an AMB are the electromagnets, the sensor system, the controller system, the power amplifiers and the rotor. The AMB system is a classic example of an unstable system due to the fact that the electromagnet position relative to the rotor must continually be corrected as forces are exerted on the rotor. This also indirectly implies that the AMB system is a closed loop system. Rotor deviation is sensed by the sensor system and the information is sent to the control system. The control system in turn uses the input from the sensor system to calculate an output according to the observed deviation from the reference point. This output is then sent to the power amplifiers, which control the power of the electromagnets, which in turn exert the required mechanical forces on the rotor to ensure rotor levitation at the required reference position. Figure 1-1 illustrates a radial AMB system with control in one axis.

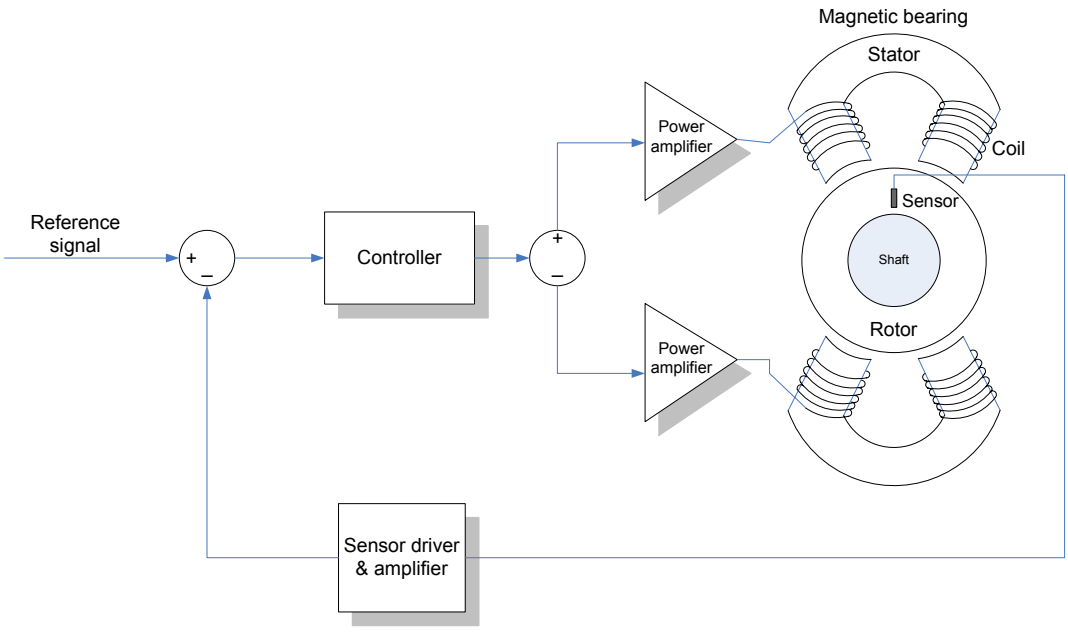


Figure 1-1 Active magnetic bearing system

The efficiency of a magnetic bearing is greatly dependent on the efficiency of the position sensors used in the system [3]. To measure the displacement of a moving rotor, contactless

sensors able of measuring a rotating surface must be used. The choice of displacement sensor will depend on the application of the magnetic bearing, the measuring range of the sensor, the required sensor linearity, sensitivity and resolution, as well as the frequency range of the bearing.

Various contactless displacement sensors are used in AMB systems. The most common are:

- **Inductive position sensors**:
  These sensors are based on the changing inductance in an air-gap when a ferromagnetic object moves nearer. The sensor consists of a coil that is excited by a high frequency oscillation. As the rotor position varies, the inductance of the coil changes according to the distance between the rotor and the sensor [3].

- **Capacitive position sensors**:
  Since the capacitance of a plate capacitor changes according to the change in clearance between the two plates, displacement can be measured by placing the one plate in a fixed position (sensor probe) and connecting the other plate to the object to be measured (target). The output of the sensor is proportional to the distance between the plates, since the plate size and dielectric stays constant [3].

- **Optical position sensors**:
  These sensors are based on the principle of light intensity. It consists of a light source and a light sensitive sensor. As the object position varies, it moves in front of the light source, obscuring the light from the sensor. The resulting difference in light intensity is converted into an electrical signal and serves as the measurement for the position of the object. Position can also be sensed by reflecting light onto the object to be measured. The fraction of light received by the sensor then varies according to the movement of the object [3].

- **Eddy current position sensors**:
  This sensor is based on the occurrence of eddy currents in a conducting object when placed in a magnetic field. It consists of an aircoil excited by a high-frequency alternating current. As the electromagnetic coil of the magnetic bearing induces eddy currents in the conducting object, energy from the oscillating circuit is absorbed. This results in a change in the amplitude of the oscillation, providing a voltage proportional to the distance between the sensor and the object [3]. This type of sensor is also the main focus of this project.

1.2 Problem statement

The motivation for this project stems forth from an AMB industrialization exercise done by the McTronX research group. Industrialization inherently requires cost reduction of the end product, which in turn involves cost reduction of all components in the system. With the sensor system being one of the more expensive components of the AMB system, the need for cost reduction of this system in particular became apparent. This consequently led to the development of a low-cost printed circuit board eddy current displacement sensor. The main motivation for the sensor driver project is therefore to supplement the development of that low-cost sensor. The sensor driver project is also part of the larger ADES (AMB and Drive Electronics System) project, which aims to develop an electronic packet for a high speed AMB system.

This project entails the design and development of a high precision sensor driver for a PCB eddy current displacement sensor. The driver comprises a sensor excitation circuit, signal conditioning circuit and a digital signal processor. Circuit board design and firmware development therefore constitute the main aspects of this project.

The excitation of the sensor coils need to be accurate and stable. Any variation in the excitation signal will result in a variation of the sensor output signal, causing erroneous position readings and faulty control of the AMB. The signal conditioning circuit is responsible for demodulating the analogue sensor output signal by filtering, rectifying, scaling and amplifying the signal. This ensures that the signal reaching the digital controller will have the correct range for the analogue-to-digital converter, ensuring maximum resolution. The digital controller in turn performs position extraction and linearization on the received signals. After the signal processing have been completed, the position values are sent to a main controller via a communications bus. The digital controller is therefore responsible for the intelligence of the sensor system. Figure 1-2 illustrates the proposed concept for the sensor driver.

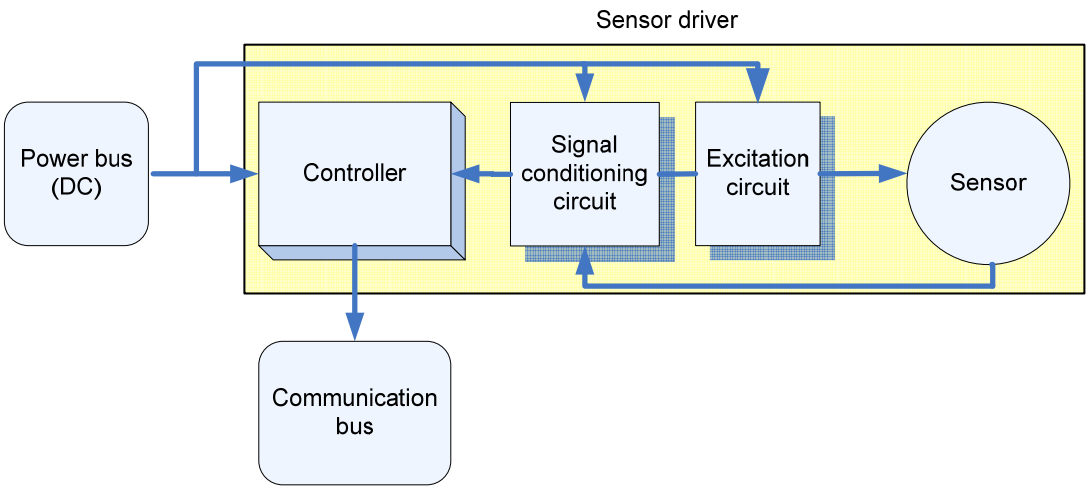


Figure 1-2 Proposed design for sensor driver

1.3 Issues to be addressed

1.3.1 Sensor driver specification

A complete sensor driver specification must be derived. This entails specifying the inputs and outputs required for each sub-system for both correct operation and for the sensor driver as a whole to adhere to this set of specifications.

1.3.2 Conceptual design

A conceptual design must be developed for the sensor driver system, as well as for all its sub-systems. The conceptual design will form the basis of the detail design to be performed, and will consist of analysis and evaluation of all considered designs to be able to choose the most suitable design for the detail design process. The conceptual design for each of the sub-systems is given.

1.3.2.1 Excitation circuit

The excitation of an eddy current sensor plays a crucial role in the accuracy of its output. If the excitation is not highly accurate and completely stable, the output will vary with every fluctuation of the excitation signal. The PCB eddy current sensor used in this project requires a 2 MHz sinusoidal excitation signal. After evaluating various means of excitation, the most suitable option can be chosen.

1.3.2.2 Signal conditioning circuit

The PCB eddy current sensor used in this project provides an analogue amplitude modulated sinusoidal voltage output. To obtain the position measurement from the sensor output, an analogue circuit is required to demodulate, filter and amplify the sensor output signal. After evaluating different signal compensation circuit designs, the best one can be chosen for implementation.

1.3.2.3 Digital controller

As discussed earlier, a digital controller is responsible for the “intelligent” part of the sensor driver. The digital controller to be implemented must have ample processing power and memory to perform the tasks necessary for the sensor driver to function according to its specifications. Firmware has to be designed and developed for implementation on the digital controller. This will be done in combination with the hardware development of the project. The implementation of the firmware on the controller will be simplified through good firmware design. This will also result in more efficient controller implementation.

1.3.3 Detail design

After the conceptual design phase has been completed, the detail design phase will commence. It will entail the circuit layout and construction of each sub-system design as decided upon during the conceptual design, together with the implementation of the firmware.

1.3.4 System integration

To complete the sensor system, all the sub-systems have to be successfully integrated. This includes the excitation circuit, PCB sensor, signal conditioning circuits, and digital controller. All sub-systems will, where possible, first be simulated separately and then combined with other sub-systems. The system integration will also consist of the critical components first being tested and evaluated for further implementation. The next integration step will consist of designing and evaluating a test circuit containing the first detail design prototype, and the last integration phase will consist of the final sensor driver board containing all sub-systems on a single multi-layered PCB.

1.3.5 System evaluation

The sensor driver has to be tested and evaluated in terms of its performance. Precision will form the main criteria for system evaluation. The results obtained will be used to characterize and verify the sensor system. Verification of each sub-system design will be performed throughout the design phase of the sensor driver, but the verification of the sensor driver design concept will be done with the sensor driver test circuit. Validation of the sensor driver will take place with the final sensor driver board, thereby validating the sensor system as a whole. Lastly, recommendation for further work and conclusions will be derived.

1.4 Research methodology

1.4.1 Sensor driver specification

The basis of the sensor driver specification will be derived by first doing research on the specifications of commercially available eddy current sensors. This research is necessary to derive a specification that will ensure a viable low-cost alternative sensor system. In order for the specification to be a practical guide for the design process, a thorough literature study needs to be performed, summarizing the most important research components of the project in chapter 2 of the dissertation.

1.4.2 Conceptual design

The conceptual design will be performed by obtaining various designs for each sub-system from studying the literature. Each of these designs will then be considered through either analytical means, or through the use of a simulation package like Orcad®. This consideration process will enable the most suitable design to be chosen for the detail design. An appropriate digital controller will also be selected. The methodology for each sub-system will now be given.

1.4.2.1 Excitation circuit

The main elements of the excitation circuit are the oscillator and the voltage-to-current converter. Each of these elements must be thoroughly investigated, and all possible designs must be evaluated through analytical means or through simulation, and then physically tested. Temperature, frequency and amplitude stability are the main design requirements. Cost must also be considered during design, as one of the requirements for the sensor driver system is to be low-cost.

1.4.2.2 Signal conditioning circuit

In order to extract the measured position signal from the sensor, the output signal of the sensor must first be demodulated and low-pass filtered to obtain a direct current (dc) signal value. This signal will then be filtered further to remove as much noise and interference as possible. The signal must then be scaled and amplified to utilize the entire range of the analogue-to-digital converters (ADCs) of the controller to achieve maximum signal resolution. As with the excitation circuit, temperature stability, high accuracy and low-cost are the main requirements of the signal compensation circuit.

1.4.2.3 Digital signal processor

Research will be done on DSPs, microcontrollers and FPGAs in order to decide on a suitable device for this project. Depending on the complexity of controller implementation, the PCB layout and integration of the digital controller will either be done in house, or sub-contracted to an external company. The firmware will consist of low-pass filters, position extraction algorithms and linearization algorithms, together with the communication architecture and protocol required to communicate with the external main controller or host. After the algorithms have been designed, it must be coded onto the digital controller using an appropriate language and compiler, and then tested and modified until satisfactory results are obtained.

1.4.3 Detail design

The analogue electronics require careful circuit design and PCB layout in order to minimize noise and external interference within the circuit. The circuit design and PCB layout will therefore constitute one of the main aspects of this project. After the circuit designs and layout have been completed, the circuit needs to be manufactured on a PCB. This will be sub-contracted to an external company which will be decided on after a quote comparison has been completed. In the meantime, the firmware design for the sensor driver will be done. After the manufacturing and populating of the PCB have been done, the firmware will be coded onto the digital controller using an appropriate language and compiler that will be determined by the device used.

1.4.4 System integration

After all the sub-systems have been designed and tested individually, they will be integrated with the system as a whole. This will be done by first simulating each sub-system separately and modifying the design until the correct results are obtained. Thereafter the individual sub-systems will be integrated, and the system as a whole simulated and tested. When satisfactory results are obtained, a sensor driver test circuit will be designed in order to implement the design concept on a single PCB. The last integration phase will consist of the final sensor driver board containing all sub-systems on a single multi-layered PCB. This entire integration process will also constitute one of the main aspects of the project.

1.4.5 System evaluation

The sensor system will be evaluated by taking measurements during testing and using the results to verify the system response with regards to the system specifications. The results obtained will also be used to verify, characterize and validate the system. Verification in the context of this project entails confirmation of the designed functional operation of the unit or circuit to be tested. Validation in the context of this project entails evaluating the circuit or system with regards to set specifications determined beforehand or with regards to common conditions or concepts applicable to the circuit or system to be tested. Both analogue and digital measurements will be evaluated. Recommendations for possible further work and conclusions will lastly be derived.

1.5 Dissertation overview

- **Chapter 2: Literature study**

  A detailed background study on the defining concepts of this project is provided in this chapter. An overview of sensor characteristics and signal conditioning will be given, along with a discussion on eddy current position sensors, PCB sensors and the concept of intelligence as applicable to sensor systems. The requirements of the sensor driver system will also be discussed, as well as an overview of electro-magnetic compatibility (EMC). Information on the types of digital controllers considered for implementation in this project will also be provided.

- **Chapter 3: Driver operation and specification**

The requirements of the sensor driver system as a whole is obtained through research on existing eddy current sensors. Affine arithmetic is also used to perform a functional analysis and allocation of the sensor driver system in order to obtain a final system requirement specification

- **Chapter 4: Sensor driver analogue design**

Chapter 4 presents the design of the analogue circuits of the sensor driver system. As each functional unit must adhere to the specifications set in the previous chapter, various designs are considered for each functional unit. The design of each functional unit consists of the conceptual design, detail design and specification of all the performance parameters. Two test circuits are also designed and built in order to verify the concept of the sensor driver.

- **Chapter 5: Sensor driver digital design**

This chapter presents the design of the digital processing circuit, along with the design of the firmware. The digital processing circuit consists of various elements, and each will be discussed. The design of the firmware is given in the form of a detailed description of the algorithm used along with all the interfaces in the design.

- **Chapter 6: Final sensor driver design**

In this chapter the final implementation of the sensor driver is discussed, along with the requirements for the final sensor system. The alterations made to the analogue design after evaluation of the sensor driver test circuit are discussed, as well as the process of integrating the analogue and digital designs to form the final sensor driver design. The conceptual and final PCB layout designs, together with all the issues surrounding it, are also described in detail.

- **Chapter 7: Evaluation**

In this chapter the results obtained from all the circuits of the sensor driver that were constructed and tested are provided and discussed. This includes the measurements taken from the oscillator test circuit, the sensor driver test circuit and the final sensor driver circuit. These measurements are used to verify the design of the different circuits with regards to its set specifications. The measurements of the final sensor driver in particular will be used to validate the sensor driver system.

- **Chapter 8: Conclusion and recommendations**

This chapter concludes the dissertation and presents an overall discussion on the results obtained in chapter 7. Problems experienced regarding the implementation of the project and recommendations for future work will also be given.

Chapter 2

Literature study

This chapter presents a detailed background study on the defining concepts of the project, starting with a discussion on sensors and signal conditioning, followed by a discussion on eddy current position sensors and PCB sensors. An overview of the sensor driver system is also given, and the concept of intelligence as applicable to sensor systems is discussed. The important considerations regarding electromagnetic compatibility are also discussed, followed by a discussion on the type of digital controller to be considered for implementation in the design. The chapter is concluded with a critical overview of the literature presented on all the topics contained within the chapter.

2.1 Background

Since sensor characteristics form the basis of the sensor specification, these characteristics must be thoroughly defined and understood in order to compile an appropriate specification. Both the static and dynamic sensor characteristics will be discussed. The purpose of signal conditioning in general is explained, and the main components needed to perform the signal conditioning for the sensor driver are discussed.

The focus is then shifted from sensors in general to the new kind of sensor used in this project, namely a printed circuit board (PCB) eddy current sensor. This sensor is compared to commercially available eddy current sensors by first presenting a brief background on eddy current sensors, then describing the PCB sensor followed by the advantages of this sensor above the standard sensors.

After all the necessary background information regarding the project components have been presented, the main focus of the project will be discussed, namely the requirements for the sensor driver. An overview of the sensor driver will firstly be given, followed by a discussion of

each of its sub-systems. The concept of intelligence will also be defined, and the incorporation thereof into the sensor driver will be described. The last section presents a few electromagnetic compatibility (EMC) considerations that must be implemented in the sensor driver system.

2.2 Sensor characteristics and signal conditioning

In order to correctly implement a sensor, its characteristics must first be understood. These sensor characteristics also form the basis of the sensor specification, as the specifications are defined in terms of the characteristics. Since the output of any physical sensor alone is seldom sufficient to adhere to industry specifications, signal conditioning becomes necessary in order to achieve these requirements. There are two types of sensor characteristics, namely static and dynamic. Both types of characteristics will be discussed, along with signal conditioning in general.

2.2.1 Static sensor characteristics

In many systems, the quantity to be measured changes slowly over time. It is therefore essential to know the static characteristics of the sensor. These characteristics, however, also influence the dynamic behaviour of the sensor, making them just as important in systems with high-speed changes in measured quantity. The following static characteristics will be discussed: accuracy, precision, repeatability, reproducibility, sensitivity, linearity, and resolution.

2.2.1.1 Accuracy

The accuracy of a sensor can be defined as the quality that describes the ability of the sensor to give results close to the true value of the measured quantity. Sensor accuracy is established by performing static calibration. This is done by keeping all sensor inputs constant, except the one to be studied, and changing this input very slowly. The difference between the measured value and the true value is called the absolute error, and is mostly expressed as a percentage of the full-scale output (FSO).
Therefore,

$$\text{Absolute error} = \text{Result} - \text{True value} \qquad (2.1)$$

The accuracy of the sensor can also be expressed as a quotient between the absolute error and the true value, called the relative error.

$$\text{Relative error} = \frac{\text{Absolute error}}{\text{True value}} \tag{2.2}$$

Relative errors are usually given in two parts: one as a percentage of the reading, and another that is a constant, usually a percentage of the FSO [4].

2.2.1.2 Precision

Precision is the quality that describes the ability of a sensor to provide the same reading when repetitively measuring the same quantity under the same conditions. The difference between the result and the true value is ignored, and only the difference between successive readings of the same quantity is used. Precision is therefore a necessary but not sufficient condition for accuracy [4].

2.2.1.3 Repeatability

The repeatability of a sensor is the conformity between successive results obtained using the same method under identical conditions and in a short time interval [4].

2.2.1.4 Reproducibility

The reproducibility is also a measure of the conformity between successive results, but over a much longer time and under different conditions [4].

2.2.1.5 Sensitivity

The sensitivity of a sensor is defined as the slope of the calibration curve, whether it is constant or not along the measurement range [4]. The sensitivity of a position sensor is given by the ratio of the output signal over the total displacement of the target. If an output signal x is related to an input signal y by the equation $y = f(x)$, the sensitivity at a point x_1 is given by (2.3) as

$$S(x_1) = \left.\frac{dy}{dx}\right|_{x=x_1} \tag{2.3}$$

Sensors must preferably have a high and constant sensitivity. For an eddy current position sensor, the sensitivity of the sensor is generally given in V/m [4].

2.2.1.6 Linearity

The linearity of a sensor is a specification of how closely the sensor calibration curve fits a specified straight line. By keeping the sensitivity of the sensor constant, the linearity of the sensor is increased. The linearity of a sensor can also be improved by incorporating a digital processor and implementing a linearization function to provide the input values corresponding to the measured values. Linearity is usually given as a percentage of the FSO [4].

2.2.1.7 Resolution

Resolution is described as the minimum change in sensor input necessary to produce a change in the sensor output. With a rapid changing input signal, the resolution of a sensor is mostly determined by the noise floor of the sensor. The resolution of a sensor is therefore the minimum change in input that can be detected by the sensor above the noise floor. It can not be improved by amplification or modulation by the detector electronics. The resolution of a sensor is given as a percentage of the FSO, or as a distance [4].

2.2.2 Dynamic sensor characteristics

The response of a sensor to a changing input signal is different to the response of the sensor when the input signal is constant. This is due to the presence of energy-storing elements in the system. Dynamic sensor characteristics include the dynamic error and speed of response. These characteristics describe the behaviour of the sensor with a changing input signal applied, and will each be discussed. The dynamic characteristics of the sensor are determined by applying a variable signal to its input, usually a transient, periodic or random signal like white noise. In a linear system, only one response is necessary to fully characterize the system.

2.2.2.1 Dynamic error

The dynamic error of a sensor is the difference between the measured value and the true value for the measured quantity when the static error is zero. The dynamic error is therefore an indication of the difference in the sensor's response to the same input magnitude [4].

2.2.2.2 Speed of response

The speed of response is an indication of how fast the sensor reacts to changes in the input signal. The delay between the applied input and the corresponding output must be kept as small as possible, due to the fact that the sensor system is to be implemented as part of the control system of an AMB. A large delay may result in oscillation of the rotor [4].

2.2.3 Signal conditioning

Sensor signal conditioning can be described as processing the form of a sensor's signal to make it comprehensible to or compatible with a device [1]. Due to the typical small output values of sensors, most sensor signals require some form of preparation before they can be digitized. All these preparation technologies are forms of signal conditioning. The most common types of signal conditioning are: amplification, attenuation, isolation, multiplexing, filtering, excitation, linearization, demodulation, cold-junction compensation and simultaneous sampling.

For a sensor such as an eddy current sensor, the main types of signal conditioning are: sensor excitation, sensor output filtering, signal amplification, signal demodulation, and signal scaling. Each of these types of signal conditioning will now be briefly discussed.

2.2.3.1 Sensor excitation

In order for a sensor such as an eddy current sensor to work correctly, it must be excited by an alternating voltage or current. This excitation signal produces a magnetic field around the target object (e.g. rotor), inducing eddy currents within the target material. These eddy currents then absorb energy from the oscillating circuit, changing the coil's inductance and providing information regarding the displacement of the target [3]. The excitation of the sensor needs to be extremely stable and accurate for correct position measurement.

2.2.3.2 Sensor output filtering

Since sensor systems are typically very sensitive and susceptible to noise, the output of the sensor needs to be filtered to eliminate as much noise as possible within the system. The signal is typically band-pass filtered at the sensor's operating frequency, since the target's displacement information is provided by the variation in the amplitude of the output signal.

2.2.3.3 Signal amplification

Since the output of most sensors are typically in the range of tens of millivolts, a gain stage is required to obtain a signal that is large enough for further processing. This can be achieved by implementing an operational-amplifier gain circuit. It is also desirable for the gain to be variable in order to perform fine-tuning on the sensor's signal conditioned output span [13].

2.2.3.4 Signal demodulation

Additional processing of the signal requires that it must be a direct current (dc) signal. Since the sensor's output is an alternating current (ac), it must be amplitude demodulated. Demodulation is the act of removing the modulation from an analogue signal to get the original baseband signal back. This entails rectifying the signal so that the entire signal is now positive. The signal is then low-pass filtered so that only the peak amplitude values of the signal remain, producing a dc signal. Figure 2-1 illustrates amplitude demodulation, with the blue line representing the dc signal obtained.

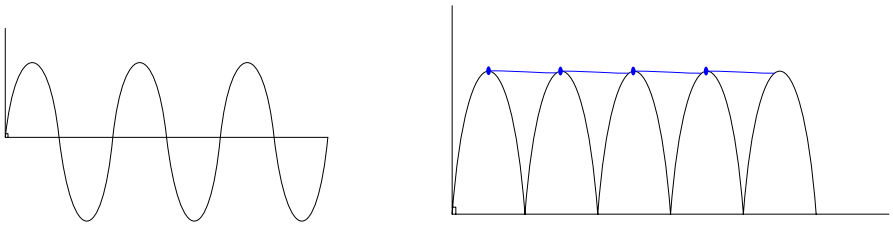


Figure 2-1 Amplitude demodulation

2.2.3.5 Signal scaling

If the intended application requires an analogue-to-digital converter (ADC), the sensor output must be direct current (dc) and within a specified amplitude range. This entails that the sensor's output dynamic range must be positioned within the high and low input reference voltage range of the ADC. This can be accomplished by creating a positive or negative dc level shift of the signal. A dc level shift, together with a gain adjustment, can also be used to utilize the full output range of the operational amplifier and ADC [13].

2.3 PCB eddy current sensors

2.3.1 Eddy current sensors

2.3.1.1 The eddy current phenomenon

The electrical phenomenon of eddy currents is caused when a conductor intersects a changing magnetic field, or vice-versa. This relative motion causes a circulating flow of current within the conductor, called eddies of current. These eddies create electromagnets with magnetic fields

opposite to that of the applied magnetic field, in accordance with Lenz's law. The magnitude of the opposing magnetic field is directly proportional to the relative velocity of motion, as well as to the electrical conductivity of the conductor [4]. This phenomenon is what forms the basis of the eddy current sensor. Since it is a non-contact sensor, it is ideal for use in magnetic levitation systems, especially AMB systems. These sensors are also not susceptible to dirt or water, and can be operated at high temperatures [4]. In addition, the target to be measured (e.g. rotor) does not need to be of magnetic material in order for the eddy current sensors to work.

2.3.1.2 Standard eddy current position sensors

Eddy current position sensors have been in use for more than thirty years [4]. Most commercially available eddy current sensors consist of a single coil together with an excitation circuit and some form of signal conditioning and linearization. A change in target displacement will result in a change in the coil's inductance and thus changes the oscillating frequency. The position output is then provided by this change in oscillating frequency [7]. In order for a radial eddy current or inductive sensor to function, the axis of the sensor coil must always be perpendicular to the surface of the rotor, as shown in Figure 2-2.

With conventional eddy current sensors this means that provision has to be made for installation space for both the sensor and its mountings. For radial displacement measuring, both the x- and y-axis need to be measured, requiring at least two sensors to be placed around the rotor. This not only limits the size of the magnetic bearing, but also increases the cost [8].

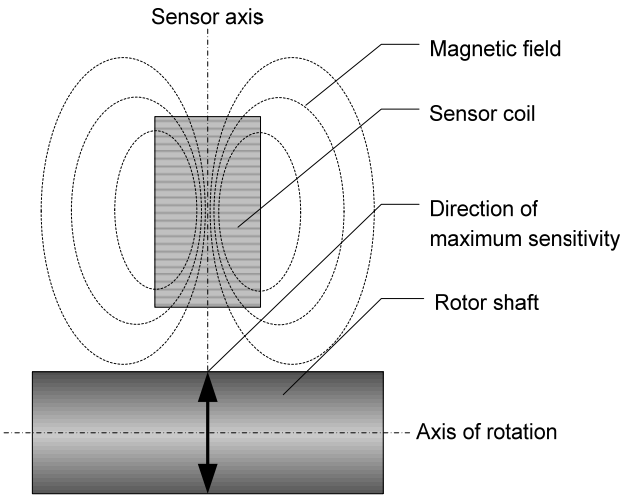
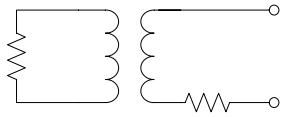


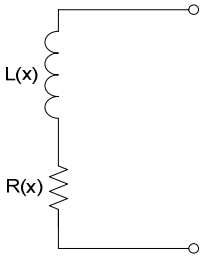
Figure 2-2 Standard sensing principle [8]

2.3.1.3 Sensor operation

The eddy current sensor can generally be modelled by an air-core transformer, with the target and sensor coil constituting the primary and secondary of the transformer, as shown in Figure 2-3 a). This model can further be simplified to an inductor and resistor network that depends on the distance between the primary and secondary of the transformer (standoff), as shown in Figure 2-3 b) [5].



a) Transformer model



b) Simplified model

Figure 2-3 An eddy current sensor modelled as a transformer [5]

The sensor coil is excited by a constant, high frequency oscillating signal, typically a 0.5 - 2 MHz sine wave. This oscillation creates a surrounding electromagnetic field. When the target position varies, the electrically conductive material of the target close to the sensor coil carries the induced eddy currents. These eddy currents create an opposing electromagnetic field, which in turn changes the impedance of the sensor coil and provides information regarding the coil distance from the target [6].

2.3.2 PCB sensors

PCB eddy current sensors have only recently been successfully developed. Previous PCB sensor designs consisted of a single annular coil implemented on a PCB, and performed both excitation and detection with the same coil. This design was however not suitable for a radial displacement sensor, due to its low lateral sensitivity. A new PCB design was then developed,

specifically for a radial displacement sensor. An overview of this new PCB sensor is firstly presented, followed by a discussion on the development of this sensor from a single annular coil PCB sensor, to its current multi-coil form.

The PCB eddy current sensor used in this project is based on the patented design of Philipp Bühler [8], and is shown in Figure 2-4. It consists of an excitation coil wound around the rotor, and four detection coils arranged at 90° angles. Position measurement is done differentially, subtracting the output of opposite detector coils to obtain the true rotor position. Position measurement is therefore done in both the x- and y-axis simultaneously by one sensor, improving on the conventional eddy current sensors [7].

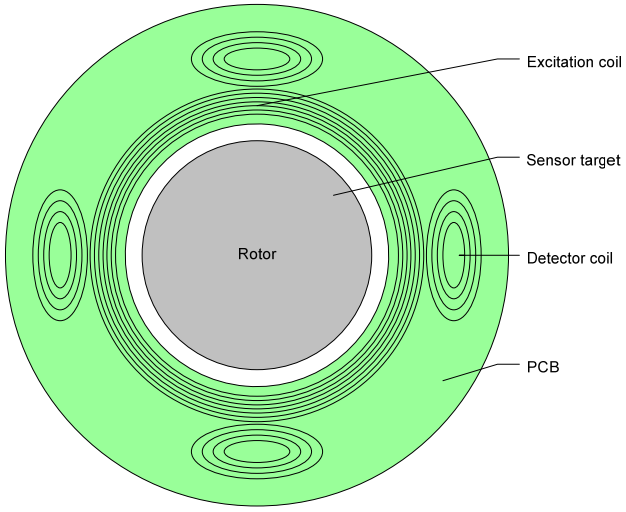
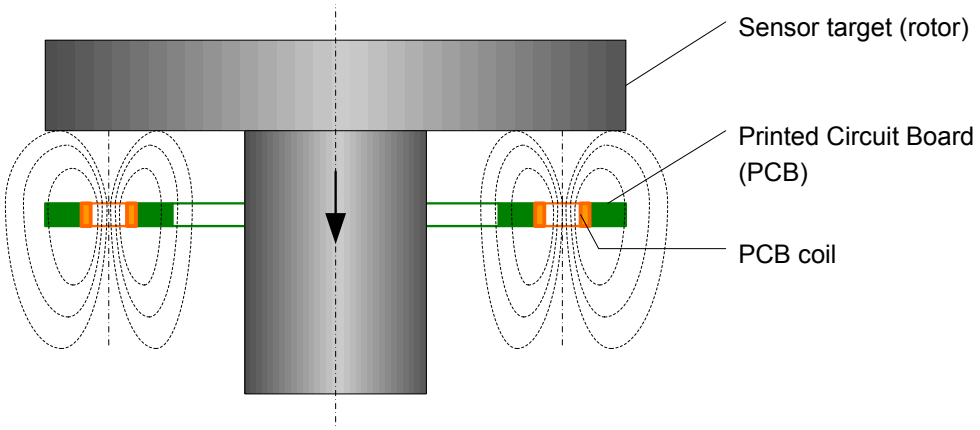


Figure 2-4 New PCB radial sensor [8]

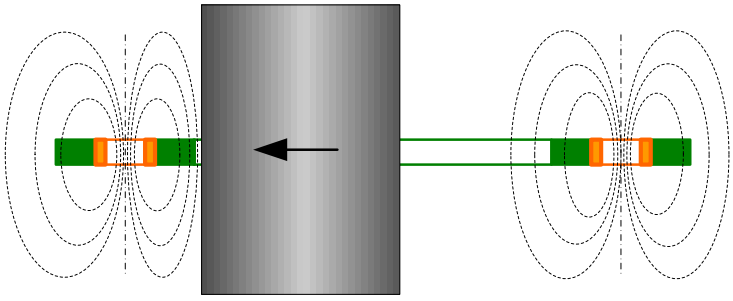
When only a single annular coil is used for both excitation and measuring, as with conventional eddy current sensors, high displacement sensitivity is achieved only perpendicular to the sensor coil plane. For a flat PCB sensor, this means that axial displacement is accurately measured, but lateral position measurement is very difficult to achieve. Figure 2-5 illustrates the sensitivities of this kind of PCB sensor in both the axial and radial directions.

The reason for the increased axial sensitivity is due to the fact that the sensor coil's axis will always be parallel to the axis of rotation, and perpendicular to the axial direction of the rotor. When a lateral displacement occurs, the rotor will only have a minor field distortion effect on the

magnetic field of the sensor. In the coil's centre, where the actual measurement occurs, the field strength is therefore virtually unchanged [8].



a) High axial sensitivity



b) Low radial sensitivity

Figure 2-5 Single coil directional sensitivities [8]

To achieve high lateral sensitivity, all the necessary coils have to be combined into one common and interdependent electromagnetic field circuit. This means that the individual coils become electromagnetically coupled, which results in a higher sensitivity. Furthermore, separate coils are used for magnetic field generation, or excitation, and field measurement, or detection [8].

The increased lateral sensitivity of the PCB eddy current sensor used in this project is illustrated in Figure 2-6. The coil arrangement of this sensor results in sufficiently large inductances, even with a low number of windings per coil and a small detector coil diameter. This is due to the

large induction of the excitation coil, and the mutual coupling between all the coils. The PCB sensor is also highly interference proof to lower frequency electromagnetic fields typically found in magnetic bearing systems [8].

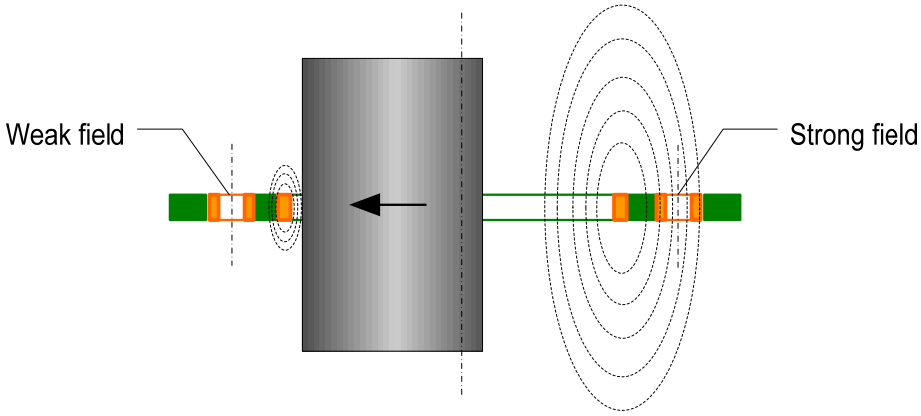


Figure 2-6 Lateral sensitivity of the new PCB sensor [8]

2.3.3 Advantages

According to [8], the main advantages of this new radial PCB eddy current sensor over conventional AMB sensors are:

- High cost-efficiency
- High level of reproducibility and accuracy
- High sensitivity
- Ultra compact design
- No extra components on PCB
- Highly interference proof to external magnetic fields from AMBs

Other advantages include:

- Axial movement and rotational speed measuring capability [7]
- Differential position measurement
- Separate excitation and detection coils

2.4 Sensor driver requirements

The sensor driver will be the main focus of this project, since the project aim is to design and develop a high precision driver for an eddy current displacement sensor. An overview of the sensor driver is given, followed by a discussion of each of its sub-systems.

2.4.1 Overview

The sensor driver will be responsible for four main function. First it must supply the excitation coil of the sensor with the correct input signal. Next, it must perform the signal conditioning on the output of the sensor and then perform differential position extraction on the position signals. Lastly, it must compensate the position signal in order to linearization the position output values in order to improve the accuracy of the sensor.

The sensor driver will consist of several sub-systems, including a sensor excitation circuit, the PCB sensor, a signal conditioning circuit, and the digital controller. This proposed design is illustrated in Figure 2-7. Analogue design will form the main study field for this project, as the design and implementation of the electronic circuits will be crucial in determining the success of the sensor driver. Firmware design and implementation will constitute the secondary study field of the project.

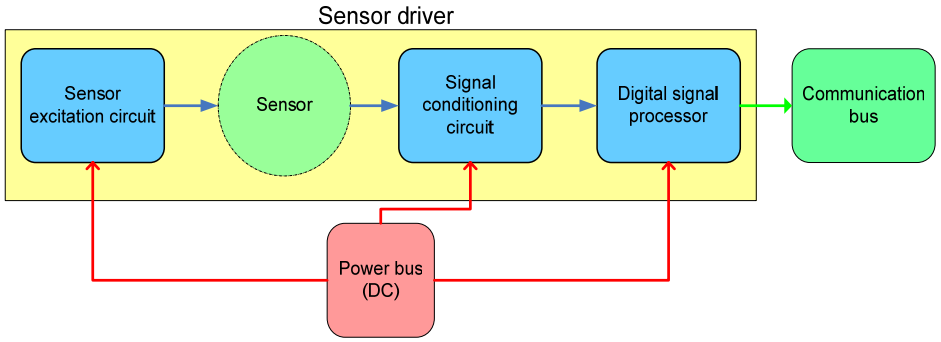


Figure 2-7 Proposed design for the sensor driver

The proposed operation of the sensor driver is shown in Figure 2-8. The excitation circuit provides the input signal to the excitation coil of the sensor. This results in four output signals from the detector coils. These signals are then fed to the signal conditioning circuit, where it is filtered, demodulated, and scaled to the correct values for the analogue-to-digital converters

(ADCs) of the digital controller. After the signals are converted to digital values, they are tested to determine whether or not they are in a permitted range. Next follows the differential position extraction, linearization and temperature compensation. Lastly, the position values are placed on the digital communications bus and sent to the main controller.

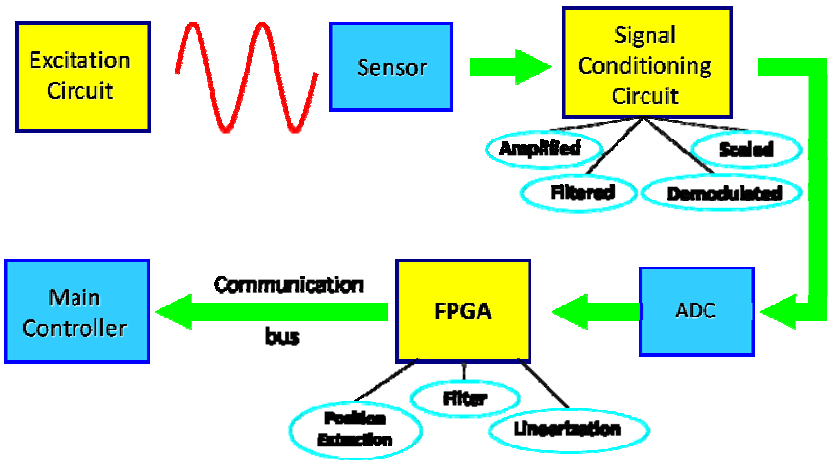


Figure 2-8 Operational diagram for the sensor driver

All of the sub-systems of the sensor driver are crucial for correct operation of both the sensor and the sensor driver. Each sub-system will now be discussed.

2.4.2 Sensor excitation circuit

The first sub-system is the sensor excitation circuit. The main requirements for this input signal are: extreme amplitude stability, frequency stability, and temperature stability. Amplitude stability is necessary due to the fact that any variation on the input signal will result in a variation on the output signal, producing false readings. Frequency stability is required, since the electrical conductivity characteristic of a material varies with frequency, influencing the response of the sensor and affecting its output. Temperature stability is necessary to minimize sensor drift due to increasing temperature. An input signal that varies with temperature would once again result in a variation of the output signal, impairing the performance of the sensor.

The sensor coil is excited by a 2 MHz sine-wave with 100 mA rms magnitude. In order to produce this signal, the following three components are needed:

- Power supply
- Oscillation circuit
- Voltage-to-current converter

Each of these components will now be discussed.

2.4.2.1 Power supply

The power supply to the sensor driver will be the same as that of commercial eddy current sensors that are currently used for research purposes. This is done so that it will be possible to replace the sensor unit with a standard commercial eddy current sensor, either for testing purposes or for use in existing systems where mechanical constraints prevent implementation of the PCB sensor. The power supply will therefore be between 12.5 V and 30 V, according to the Micro-Epsilon NCDT 3700 sensor datasheet. The power supply to the sensor excitation circuit will be obtained from the sensor driver power supply and converted to the necessary level as required by the chosen circuit design.

2.4.2.2 Oscillator circuit

Different oscillator designs will be evaluated to determine the most suitable one for this application, as the performance of the oscillator circuit will directly influence the performance of the sensor. Amplitude stability is the most critical factor to be considered, followed by temperature stability, and frequency stability.

2.4.2.3 Amplitude stability

With an invariable rotor position, the output of the sensor is directly proportional to the input of the sensor. This means that any deviation on the input of the signal will result in a deviation on the output of the sensor. Since the rotor position will always vary during operation, the deviation on the input of the sensor will result in incorrect position measurement, and can lead to unstable operation. The amplitude stability of the oscillation circuit must therefore be as high as possible.

2.4.2.4 Temperature stability

Temperature stability entails minimal output change with increasing (or decreasing) temperature. If the sensor input varies with temperature, the sensor output will contain a temperature drift component, once again resulting in incorrect position measurement. The temperature stability of the oscillator circuit must therefore also be as high as possible.

2.4.2.5 Frequency stability

A varying frequency will result in varying electrical conductivity characteristics of the material to be measured. This means that the rotor material will respond differently to the excitation field of the sensor, resulting in an inaccurate position measurement. Although frequency stability has the least effect on position measurement, it must still be as high as possible.

2.4.2.6 V/I converter

The sinusoidal voltage signal from the oscillator circuit must be amplified and converted to an sinusoidal current signal for sensor excitation. This can be achieved by using either a transistor-based voltage-to-current converter circuit, a voltage-to-current converter IC, or a high-speed power-amplifier capable of delivering 100 mA_{rms} current output at 2 MHz. The latter will be used in the sensor excitation circuit.

2.4.3 Signal conditioning circuit

2.4.3.1 Sensor output filtering

The output of the sensor must be filtered to pass through only the operating frequency of the sensor, eliminating high frequency and switching noise. If the input frequency of the sensor is 2 MHz, the output signal will be band-pass filtered at 2 MHz. Since the rotor displacement information is given by the variation of the amplitude of the output signal and not by frequency variation, filtering the frequency will not influence the position measurement negatively. It will instead increase the ability of the sensor electronics to detect the deviation by lowering the noise floor, and increasing the signal-to-noise ratio (SNR). The SNR of the signal is the ratio of the power of the signal to the power of the noise corrupting the signal, while the noise floor is the sum of all the noise sources and unwanted signals in the system.

2.4.3.2 Signal demodulation

The filtered signal must be demodulated for additional processing by first rectifying the signal, then passing it through a low-pass filter. This converts the sensed voltage signal to a direct voltage signal, as already discussed in 2.2.3. During the demodulation process, the operating frequency of the sensor is removed from the signal so that only the measured displacement bandwidth remains. The signal demodulation will be performed by a demodulator IC and a low-pass filter circuit.

2.4.3.3 Amplification and scaling

The signal must be amplified and scaled to the full input range of the ADC (e.g. 0-3 V). In order to further minimize noise, the signal must lastly be passed through another low-pass filter. The output signal of the sensor is now ready to be digitized by the ADC of the digital controller for further processing.

2.4.4 Digital controller

2.4.4.1 Controller interface

The controller interface will consist of ADCs for all the analogue inputs to the controller. The inputs to the controller will consist of the four position signals from the sensor. These signals must be in the correct voltage range of the ADC to utilize the entire ADC input range and maximize the measuring range and resolution. Depending on the choice of controller and resolution requirements, either external or internal ADCs will be used. Over-sampling techniques will also be implemented to increase the resolution of the position signal.

2.4.4.2 Realizing intelligence

It is a commonly accepted fact that no sensor will deliver accurate information all of the time [9]. A measure of fault tolerance therefore has to be incorporated into sensor systems, especially in measurement critical applications such as AMBs. This is the reason why intelligent sensors have become more popular recently in applications where extreme accuracy and reliability are required. The need for accuracy and reliability is therefore also the reason that the sensor driver must incorporate a level of intelligence. Intelligent sensors in general will first be discussed, followed by a discussion on the incorporation of intelligence in the sensor driver system.

2.4.4.3 Intelligent sensors

An intelligent sensor can be defined as a sensor which adjusts its internal behaviour to optimize the data it obtained from the physical world, and then communicate it in a responsive manner to a host system. An intelligent sensor is used to integrate a standard sensing element with electronic circuits to perform calibration and compensation of the sensor, and to communicate the sensor output together with sensor health to an external host system [10]. The availability of internal computing and digital communication capability provides the “intelligent” functions of the sensor. The main features of intelligent sensors are:

- **Self-calibration:** Performing a confidence test to decide whether a new calibration is needed.
- **Self-compensation:** Implementing compensation methods to achieve high accuracy.
- **Self-validation:** Fault monitoring of the sensor performed by the sensor itself.
- **Data fusion:** Manipulation of the data.
- **Comprehensive communication:** Communicating the data via a digital communication link to an external host.

2.4.4.4 An intelligent sensor driver

The intelligence of the sensor driver will be realized by the embedded controller. The level of intelligence required will be realized by incorporating the features of intelligent sensors in the sensor driver. This will be done as follows:

- **Self-calibration** will be done by determining if the signal values are within their permitted range. If not, the sensor must be re-calibrated.
- **Self-compensation** will include performing signal linearization and temperature compensation on the position signals.
- **Self-validation** will be done by fault monitoring by the sensor itself. This means that the sensor will be able to communicate possible internal faults to the external host before a complete sensor malfunction occurs.
- **Data fusion** will be done by performing the differential position extraction of the position signals.
- **Comprehensive communication** will be realized by a communications bus between the sensor and the main controller.

These features will provide for economical maintenance, since highly skilled personnel are not required to perform sensor maintenance. It will also significantly enhance the safety of the applied system, as they will result in fewer accidents and unscheduled shutdowns [10].

2.4.4.5 Communication

The sensor driver will communicate to the main controller via a communications bus. The digital controller will convert the position values to a form that is easily transmitted to and read by the main controller. This form will typically consist of header bytes being added to the position values for identification purposes (e.g. [($x1$)(value)]). A high transmission rate between the sensor driver and the main controller is required by the ADES, typically in the range of 20 kHz. The communication protocol that will be used is RS-485, due to its uncomplicated implementation and high transmission speeds over relatively long distances. Further specifications for the communication of the sensor driver to the main controller will be determined by the requirements of the ADES.

2.5 Electromagnetic compatibility (EMC)

2.5.1 Definition

In order to fully describe electromagnetic compatibility, electromagnetic interference (EMI) must first be defined. Electromagnetic interference is defined as: "*any electromagnetic disturbance, phenomenon, signal, or emission that causes, or is capable of causing, undesired responses or degradation of performance in electrical or electronic equipment*" [14]. Electromagnetic compatibility is therefore the ability of electrical or electronic systems to function adequately in the intended operating environment without causing or experiencing performance degradation due to EMI [14].

The causes of EMI are unwanted radiated electromagnetic fields or conducted voltages and currents. The interference is produced by a source emitter and is detected by a susceptible victim by means of a coupling path.

The following coupling mechanisms may be involved [10]:

- **Conduction:** by means of electric current between components through interconnecting wires.
- **Radiation:** by means of an electromagnetic field.
- **Capacitive coupling:** by means of an electric field due to a voltage difference between conductors.
- **Inductive coupling:** by means of a magnetic field caused by current flowing in conductors.

The aim of electromagnetic compatibility is to minimize the effect of electrical noise. EMC is achieved when the EMI source minus the coupling mechanism path losses results in an emission level that is more than a predetermined safety margin less than the susceptible recipient's threshold. If electronic equipment are not properly designed to minimize the effects of interference, they can become totally inoperable or even cause other equipment to malfunction [14].

2.5.2 EMC design considerations

Good PCB design practices can help prevent EMI and EMC problems. To design for adequate EMC, the flow of the interference into and out of the circuit must be controlled [15]. The physical layout of the PCB and its metallic components require special consideration, as it is more efficient to deal with electromagnetic problems as close to the source or susceptible victim as possible. Some general EMC guidelines for PCB design are presented, followed by PCB layout considerations, decoupling, bypassing and filtering advice, followed by a discussion on good grounding practices, and lastly two EMC standards that will be implemented in the sensor driver project are presented [14].

2.5.2.1 General

Electromagnetic compatibility should be considered throughout the entire circuit design, but especially at points where high signal transitions frequently occur, and at EMI sensitive and susceptible circuit components [15].

The following general EMC guidelines applicable to the sensor driver project are given [14]

- EMI should first be controlled at the circuit and box levels before addressing it at the interconnected and system levels.
- Digital circuits are usually the source of emissions, since they handle periodic waveforms and fast switching rates, while analogue circuits are more likely to be the susceptible victims due to their high gain functions.
- An active component can produce EMI problems by transferring the emissions through its output, or by providing the path of susceptibility through its input.
- Common mode currents, although small compared to differential mode currents, can be the main cause of radiated emissions.
- By using multi-layer PC boards, with power planes, instead of single layer, free wired PC boards, emissions and susceptibility of the circuit can be greatly improved.
- In a multi-layer PC board, a trace should ideally be spaced one dielectric layer from its return path, while power and ground planes should be spaced as close as possible.
- Advantages of multi-layer PC board design with power planes include:
    - An image plane effect being produced when properly designed power planes are used. The signal and return currents in the power planes are equal and opposite in polarity, causing their electromagnetic fields to cancel.

- The overall ground impedance, as well as high frequency ground bounce being reduced through the incorporation of a ground plane. Power bus ringing at high frequencies is also reduced by the lowered impedance between the ground and power planes.

- The placement of decoupling capacitors at an IC's power pins, as well as proper power plane design in the area of the IC can improve IC outputs and help meet quick output transition needs.

2.5.2.2 PCB layout

The EMC performance of a circuit is greatly influenced by the way in which the PCB is designed. The following considerations for electromagnetically compatible PCB layout, which will be incorporated in the sensor driver design, are given [14]

- Whenever possible, a multi-layer PC board design should be used rather than single-layer PC boards. When only a single layer board can be used, incorporate a ground plane to help reduce radiation.
- In multi-layer PC boards, radiation can be reduced by at least 10 dB through the use of top and bottom ground planes.
- It is advisable that power and return paths be located on opposite sides of a multi-layer PC board. This will reduce the level of any transients that may develop on the power planes, and lower common mode EMI.
- The connection of high frequency IC power pins to the power planes should be kept as close to the IC pins as possible.
- Analogue and digital circuits will be at risk of interacting with each other when they are placed in close proximity. It is preferable that they be placed on different layers of the PCB, or at least separated with proper isolation layout.
- High frequency traces, such as used by oscillators and clocks, should be contained by two ground planes to provide maximum isolation.
- Clock and oscillator traces should use guard traces grounded to the ground plane at several locations, and these components may also need shielding with foil or metallic enclosures to provide additional EMI preventative measures.
- When the clock rate is doubled, the overall circuit cross-talk is also increased by a factor of two. This can be reduced by minimizing the PCB trace height above the ground plane.

- When traces are located too close to the board edge, PCB edge radiation may occur. This can be prevented by placing traces at a distance of at least 3 times the board thickness away from the board's edge.
- PCB trace stacking should be avoided, or at least limited to one trace height in order to reduce radiation, cross-talk and impedance mismatches.
- Parallel traces should be separated by at least 2 trace widths in order to minimize cross-talk.

2.5.2.3 Decoupling, bypassing and filtering

Power and ground connections will always introduce an impedance which will create switching noise [15]. Decoupling is therefore necessary to maintain a low dynamic impedance from the individual component supply voltages to ground. The following advice regarding decoupling, bypassing and EMI filtering is provided [14]:

- EMI filters can either be implemented as a shunt element to divert electrical currents from a trace or conductor, or as a series element to block a trace or conductor current, or as a combination of these functions.
- A low pass filter can be used to reduce high frequency EMI problems.
- When used within their high frequency performance characteristics, capacitors may be used for signal filtering and power source decoupling. Their lead and trace lengths should be kept as short as possible to prevent additional inductive reactance at high frequencies.
- PCB bypass capacitors used at high frequencies greater than 100 MHz should implement surface mount technology with vias close enough to the mounting pad to minimize or eliminate the traces. The holes of the vias should be larger than 0.9 mm in diameter and the PCB less than 7.62 mm thick to bring the power and ground planes near the body of the capacitor. This can lower the overall effective inductance of the capacitors, and greatly reduce the power and ground circuit noise.

2.5.2.4 Grounding

The purpose of grounding is to provide a reference for external connections to the system. A ground can be defined as "*an equipotential point or plane which serves as a reference for a circuit or system"* [15], although ground currents can be induced by environmental magnetic or electric fields which can result in a shift in the ground potential. The most important EMC function of a ground system is therefore to minimize interference voltages at critical points

compared to the desired signal by lowering the impedance path at these critical points [15]. The following good grounding practices are given [14]:

- Ground planes should be used instead of vectorial traces.
- Ground traces should be made as short and thick as possible.
- Signal and RF circuit grounds must be decoupled.

2.5.2.5 EMC standards

The EMC standards to be implemented in the sensor driver project are for both EMI emission and immunity for industrial environments. Although the EMC standards that commercially available sensors specify are European standards, the international (IEC) and local (SANS) equivalents were obtained and will be used for this project. The local and international standards are identical.

- **SANS61000-6-4 / IEC 61000-6-4:2006 (same as EN50081-2)**

Electromagnetic compatibility (EMC) Part 6-4: Generic standards - Emission standard for industrial environments.

This standard aims to define the emission test requirements for electronic equipment with regards to continuous and transient, conducted and radiated disturbances. It specifies the EMC emission requirements applicable to electrical and electronic equipment to be used in industrial environments. It applies to any device that is intended to be connected to a power network supplied from a high or medium voltage transformer, and also to battery operated devices intended to operate in or in proximity to industrial locations [16].

- **SANS61000-6-2 / IEC 61000-6-2:2005 (same as EN61000-6-2)**

Electromagnetic compatibility (EMC) Part 6-2: Generic standards - Immunity for industrial environments

The object of this standard is to define the immunity test requirements for electric and electronic equipment with regards to continuous and transient, conducted and radiated disturbances, including electrostatic discharges. This standard is applicable to electrical and electronic equipment that is to be used in industrial environments. It applies to any device that is intended to be connected to a power network supplied from a high or medium voltage transformer, and also to battery operated devices intended to operate in or in proximity to industrial locations, both indoors and outdoors [17].

2.6 Digital controller

The sensor driver system is required to drive and condition the signals of all the sensors used in a complete AMB system with five degrees of freedom. This entails that two radial PCB sensors and one axial PCB sensor are required for the AMB system. To allow for the possibility of being able to drive, condition and linearize an entire AMB system's sensors with one sensor driver board, the sensor driver must be able to operate up to three sensors. Since each radial sensor returns four outputs, and an axial sensor will return two outputs, the sensor driver board must be able to handle ten position signals. For this project, however, only two radial sensors will be used. The total number of position signals therefore equals eight. As the digital controller will be required to filter, perform position extraction, and linearize all the position outputs within a 50 µs time-frame, the use of a single DSP controller becomes impractical, and the use of multiple DSP controllers will be unfeasible cost-wise. In order to perform all the digital functions on all the position signals within the specified time-frame, a controller capable of parallel processing is required. This is the reason why the search for a digital controller shifted towards FPGA controllers.

FPGAs are especially suitable for use in DSP applications for the following reasons [18]:

- Very high computational workload handling ability
- Allows for customization of the architecture in order to suit your algorithm
- It reduces system costs, as the FPGA allows integration of other components needed in the system, therefore reducing the number of external components needed to perform the same tasks
- Power efficiency by delivering the lowest power for a high sample rate

Figure 2-9 illustrates a comparison between a conventional DSP processor, which performs serial processing, and an FPGA processor, which performs parallel processing.

FPGAs are Field Programmable Gate Arrays that are programmable semiconductor devices based around a matrix of configurable logic blocks (CLBs) which are connected through programmable interconnects. FPGAs differ from Application Specific Integrated Circuits (ASICs) in the sense that where ASICs are custom built for the specific design, FPGAs are programmed to the meet the specific application's requirements with regards to functionality. Most FPGAs are also SRAM based which allows it to be reprogrammable.

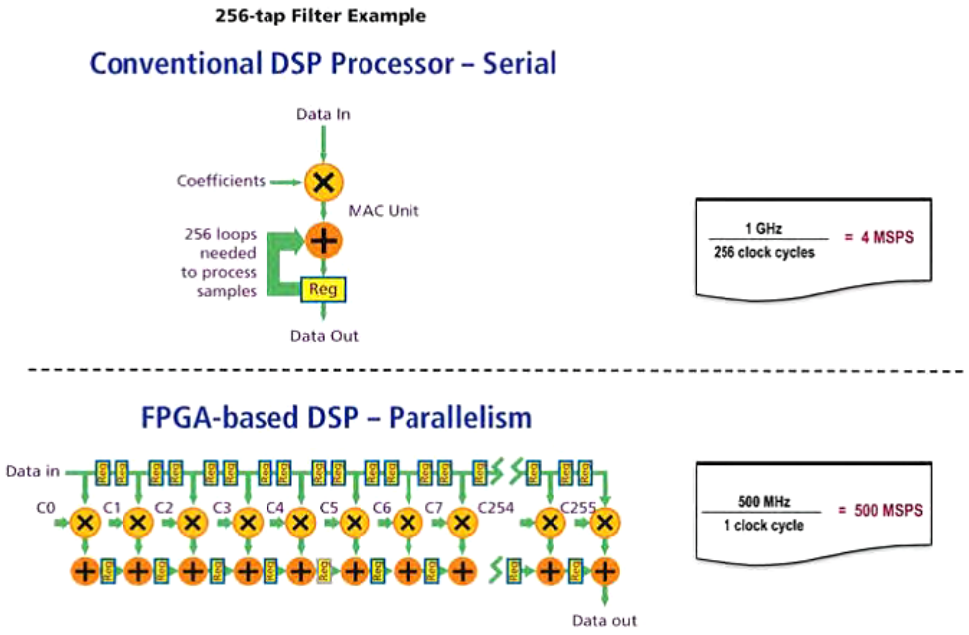


Figure 2-9 Comparison between a conventional DSP and an FPGA processor [18]

The I/O channels of the FPGA are grouped in banks, with each bank able to independently support different I/O standards. This allows for more flexible I/O support. The Digital Clock Management (DCM) is provided by most FPGAs, and has almost eliminated skew and other timing synchronization issues.

Common features of FPGAs are the following:

- Configurable Logic Blocks (CLBs). Every CLB consists of a configurable switch matrix which takes 4 or 6 inputs, selection circuitry and flip-flops.
- Interconnect. This is the physical signal routing that takes place between CLBs and I/Os.
- SelectIO (IOBs). These are the I/O banks that are capable of each supporting different I/O standars.
- Memory. Most FPGAs have embedded block RAM memory available, allowing for on-chip memory.
- Complete Clock Management. Xilinx FPGAs provide both digital clock management and phase-loop locking which provide precision clock synthesis combined with jitter reduction and filtering.

2.7 Critical overview

This chapter presented a detailed background study on the defining concepts of the project. These included sensor characteristics, signal conditioning, eddy current sensors, PCB sensors, EMC and the digital controller. The inclusion of literature on these subjects is motivated in this section, which provides a critical overview of all the literature discussed in this chapter.

- **Sensor characteristics**

In order to meaningfully obtain requirement specifications for a sensor, the sensor's characteristics must first be understood. Knowledge on sensor characteristics is also essential for correct and successful implementation of the sensor. The characteristics of a sensor are divided into two categories, namely static sensor characteristics, and dynamic sensor characteristics. These characteristics are all essential in the validation of the sensor system, which is the final outcome of the sensor driver project.

- **Signal conditioning**

The process of signal conditioning is one of the main components of the sensor driver project. This is due to the fact that the amplitude of the signal obtained from the sensor is too small and its frequency too high to be able to directly convert it into a digital signal for further processing using an ADC. Analogue signal conditioning methods are therefore necessary to obtain a meaningful signal from the sensor. These include signal amplification, filtering, demodulation and scaling. The output of the signal conditioning circuit is then suitable for an ADC to convert into digital values.

- **Eddy current sensors**

The sensor used in this project is an eddy current sensor. Knowledge on eddy current sensors are therefore necessary to understand the operation of the sensor in order to design a successful sensor driver for it. A study of commercially available eddy current sensors was also required in order for the sensor system of the sensor driver to be compared the commercially available sensors with regards to performance.

- **PCB sensors**

The type of eddy current sensor used in this project is a PCB eddy current sensor. It was therefore necessary that the principle of operation be understood in order to design an effective and successful sensor driver for the sensor. Since the PCB sensor will form part of the sensor system of the sensor driver, knowledge regarding the design of the sensor is also required.

- **EMC**

Familiarity with EMC will facilitate the design of an electromagnetically compatible sensor driver and sensor system. The causes of EMI must therefore be understood, and ways to manage it must be implemented. This meant that EMC design consideration regarding PCB layout, decoupling, bypassing, filtering, grounding and EMC in general formed an important part of the design process of the sensor driver.

- **Digital controller**

The sensor driver system requires a digital controller for digital processing of the output signals of the signal conditioning circuits. This digital processing consists of filtering, differential position extraction, and linearization of the signal. The processed signals are then communicated to an external main controller. The choice of digital controller plays an important part in the success of the sensor driver project. It was decided to consider an FPGA controller for various reasons, but most importantly for its parallel processing capabilities. It is therefore important to at least know what FPGAs are and what their main features are. This knowledge will help in deciding on a specific FPGA to implement in the sensor driver design.

Chapter

3

Driver operation and specification

In this chapter existing eddy current sensors are researched in order to obtain the requirements for the sensor driver system as a whole. A functional analysis and allocation of the sensor driver system is also done in order to obtain a final system requirement specification using affine arithmetic.

3.1. Existing eddy current sensors

In order to know what one must do, one must know what others have done. Research therefore forms an integral part in any design process. Since PCB eddy current sensors have thus far mainly been used for research purposes, information regarding sensor drivers for these sensors is very scarce. In order to acquire a meaningful requirement specification for the PCB sensor driver system, the specifications of other conventional eddy current sensors are used.

Since the objective of the PCB eddy current sensor driver is to create a cost-effective alternative to the current industrial eddy current sensors without sacrificing performance, the specification for the PCB sensor driver system will be put together using the specifications of conventional eddy current sensors currently used within the research group. Two different manufacturers' eddy current sensors are currently used in the McTronX group for research purposes, namely Micro-Epsilon's eddyNCDT 3700 (model DT3701-U1-A-C3) [19], and SKF's CMSS 65 [20]. Their main specifications are listed in Table 3-1.

From these specifications, the specifications of the PCB sensor system can be derived. It is important to note, however, that the specifications given by the products' manufacturers were obtained using a flat target object, and not a round target as is the case in an AMB system. After sensor calibration was performed on two Micro-Epsilon sensors during the design of the PCB sensor [7] their linearity was determined as 17.5% and 21.8% respectively. This varies greatly from the stated 6% given in the product datasheet.

Table 3-1 Existing sensor specifications

Specification	Micro-Epsilon eddyNCDT 3700	SKF CMSS 65
Measuring Range	1 mm	2 mm
Linearity	±6 % FSO	±1.25 %
Resolution (static)	0.2 nm (<0.000033 % FSO)	Not specified
Resolution (dynamic)	1.3 nm (0.00016 % FSO)	Not specified
Bandwidth	10 kHz	10 kHz
Temperature stability: Controller Sensor	 0.025 % FSO 0.05 % FSO	Not specified
Sensitivity	Not specified	200 mV/mil = 8 V/mm

The system specifications for the PCB sensor are therefore selected as follows:

- Linearity = ±17.5 % FSO [19]
- Sensitivity = 8 V/mm [20]
- Temperature stability (sensor) = 0.05 % FSO /°C [19]
- Temperature stability (sensor controller) = 0.025 % FSO /°C [19]
- Bandwidth = 10 kHz

Now that the goal has been set for the PCB sensor system, its operation and functionality must be determined.

3.2. Sensor driver concept selection

In order to decide on a concept for the sensor driver, its main functions must first be determined. The main functions of the sensor driver are as follows:

- Excite the PCB sensor
- Condition the sensor signals
- Generate position values to be sent to the main controller

According to [7], the PCB sensor is excited using a 2 MHz sine wave. Conditioning of the sensor signals includes amplification, filtering and linearization of the sensor signals. The position signals must also be sent to a main controller. Two main sensor driver concepts were

considered, namely 1) analogue demodulation and digital linearization, and 2) digital demodulation and linearization. Each of these concepts will now be discussed.

1. Analogue demodulation and digital linearization

In this concept, the sensor signals are conditioned by means of analogue demodulation methods, and are digitally linearized and then communicated to the main controller. Analogue demodulation converts the 2 MHz sine wave into a DC signal, which is then converted to a digital signal by means of an analogue-to-digital-converter (ADC).

Advantages:

- No complex digital processing required
- Extended optional digital filtering capabilities
- Utilize full-range of ADCs without increasing noise level

Disadvantages:

- Noise susceptibility of demodulated signals
- Specialized low-noise, high-frequency components required, which may be costly

2. Digital demodulation and linearization

In this concept, the 2 MHz sensor signals are first amplified and then converted into digital signals by means of an ADC. Signal demodulation is performed digitally, as well as the linearization of the signals. The position values are then communicated to the main controller.

Advantages:

- Less electronic components required
- Decreased noise susceptibility due to digital signals being used

Disadvantages:

- Requires an extremely high-speed ADC, at least 5 MSPS.
- Loss of position resolution due to ADC's resolution
- Requires very high throughput rate
- Complex digital processing required
- Noise level increased in order to utilize full-range of ADCs

After considering each concept, the analogue demodulation and digital linearization concept was chosen. The main reason behind this choice was the unavailability of adequate ADCs for the digital demodulation and linearization concept, as well as the fact that the second concept carries more risk than the first concept at the operating frequency of 2 MHz.

3.3. Sensor driver operation and functional analysis

Now that a concept for the sensor driver has been selected, the functional analysis can commence. A functional analysis is the process of identifying all the required functions to be performed by the system. By describing the sensor driver operation, the functions that must be performed are identified more easily.

- The sensor driver receives an external 24 V DC voltage. This supplied voltage must be converted into all the voltage supplies required by the sensor driver system.
- The excitation coil of the PCB sensor must be excited by a 2 MHz sine wave.
- The output signal of the PCB sensor detector coils must be amplified, passed through a band-pass filter, demodulated, and scaled to the correct range for the ADCs.
- The analogue signals must be converted into digital signals.
- The digital signals must be tested, filtered, linearized and the position differentially extracted and communicated to the main controller.

By reviewing the sensor driver operation and main functional analysis, the following main functional units or circuits can be identified: These functional units are shown in the system functional flow diagram of Figure 3-1.

1. Power supply circuit
2. Excitation circuit
3. PCB sensor
4. Signal conditioning circuit
5. Analogue to digital conversion circuit
6. Digital processing circuit

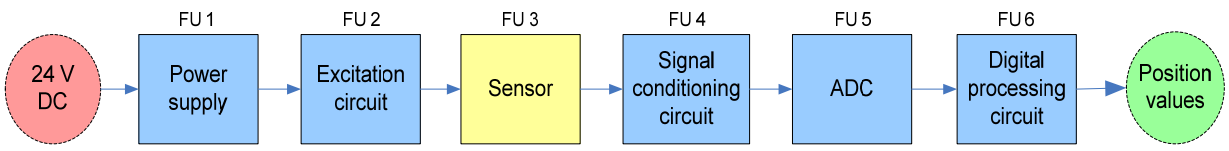


Figure 3-1 Main functional units of the sensor driver

The power supply circuit receives its input voltage from the 24 V DC power bus and supplies the rest of the sensor driver circuit with its required power. The excitation circuit generates an output signal for the excitation coils of the sensor, which in turn results in output signals from the sensing coils of the sensor. These sensor output signals are the input signals to the signal conditioning circuit, which amplifies, filters, demodulates and scales the signals before sending it to the ADC for digitization. The digital output of the ADCs are sent to the digital processing circuit, where the values are filtered, differential position extraction performed, and the position output linearized. These position values are then communicated to the main controller via a communications bus.

3.4. Sensor driver functional allocation

All of the functions identified in the functional analysis are now allocated to their corresponding functional units and sub-units. Figures 3-2 to 3-7 show the functional allocation of each main functional unit.

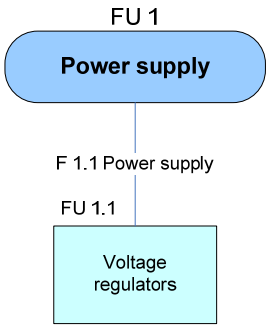


Figure 3-2 Functional allocation for the power supply unit

Figure 3-2 illustrates the functional allocation for the power supply unit. The power supply circuit (FU 1) supplies the necessary power (F 1.1) to the rest of the analogue circuit by means of voltage regulators (FU 1.1). Figure 3-3 shows the functional allocation for the sensor excitation circuit. The sensor excitation circuit (FU 2) performs the sensor excitation (F 2.1) by first generating a sine wave (F 2.1.1) by means of an oscillator circuit (FU 2.1), and then converting the voltage signal to a current signal (F 2.1.2) by means of a voltage-to-current converter (FU 2.2).

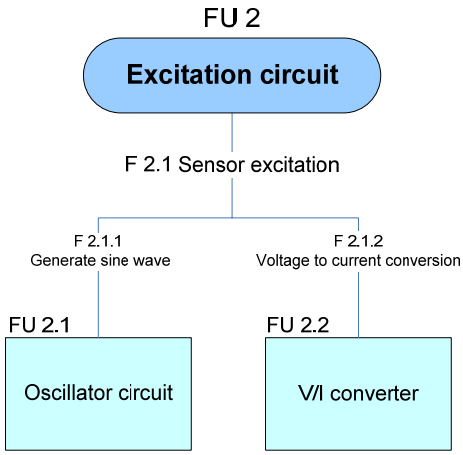


Figure 3-3 Functional allocation for the excitation circuit

Figure 3-4 presents the functional allocation for the signal conditioning circuit. The signal conditioning circuit (FU 4) performs the conditioning of the sensor output signal (F 4.1). This is accomplished by first amplifying the output from the sensor (F 4.1.1) by means of a signal amplifier (FU 4.1), then passing it through a band-pass filter (FU 4.2) in order to remove as much noise from the signal as possible (F 4.1.2). The alternating signal is then demodulated (F 4.1.3) by the amplitude demodulator (FU 4.3), and amplified and scaled (F 4.1.4) to the full input voltage range of the ADCs by another amplification circuit (FU 4.4).

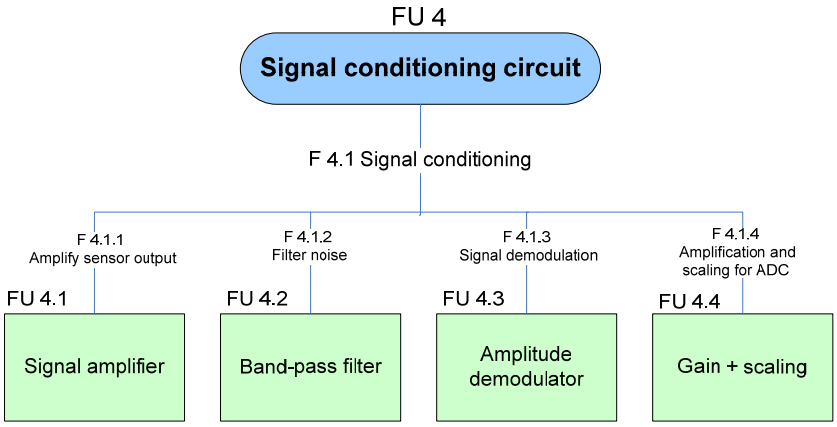


Figure 3-4 Functional allocation for the signal conditioning circuit

Figure 3-5 illustrates the functional allocation for the ADC. The ADC (FU 5) interfaces between the analogue circuit and the digital processing circuit (F 5.1) by digitizing the analogue values

through an analogue-to-digital converter (FU 5.1). The digital values are then sent to the digital processing circuit for further processing.

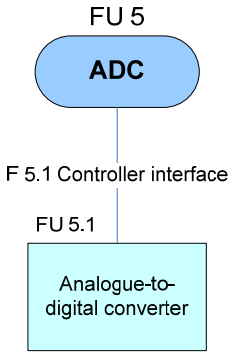


Figure 3-5 Functional allocation for the ADC

Figure 3-6 shows the functional allocation for the digital processing unit. The digital processing unit is not divided into any user-defined functional units, as all its sub-units function together as a single unit. Only the functions performed by the digital processing unit are therefore specified and illustrated in Figure 3-6, as each function will be performed by a different firmware algorithm.

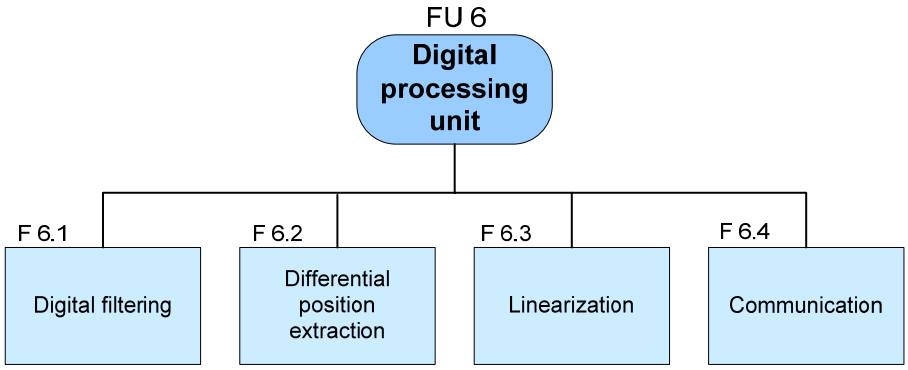


Figure 3-6 DSP functional allocation

The digital values obtained from the ADC are first tested (F 6.1) to detect possible sensor faults such as coil failure or electronics malfunction. If all the values pass the input tests, the values are passed through a digital filter to further eliminate as much noise as possible. The position values are then differentially extracted (F 6.2) by subtracting opposite coil output values (e.g.

$x=x_2-x_1$). After the position values are obtained, they are linearized (F 6.3), and then lastly sent to the main controller (F 6.4) by means of a communications bus.

3.5. Sensor driver requirement specification

3.5.1 System specifications

By knowing the functional units the sensor driver system consists of, and what the specification for the system as a whole is, a specification can be derived for every functional unit. These specifications form the requirement specification for the sensor driver. In order to derive a specification for each functional unit, a numerical analysis of the system must first be performed. The system specifications for the sensor driver system, as given in 3.1, are again given:

- Linearity = ±17.5 % FSO [19]
- Sensitivity = 8 V/mm [20]
- Temperature stability (sensor) = 0.05 % FSO /°C [19]
- Temperature stability (sensor controller) = 0.025 % FSO /°C [19]
- Bandwidth = 10 kHz

The main requirement specifications consist of linearity, sensitivity, and temperature stability. The average linearity of the PCB sensor was determined as 11.14% [7], and this figure will be used in the system analysis and performance estimation of the sensor driver system.

3.5.1.1 System analysis

In order to analyse the sensor driver system, the impact of different uncertainties such as static variations of operating conditions, dynamic variations of operating conditions, and physical effects in analogue circuits have to be considered. The effects of such uncertainties can be expressed through the use of affine arithmetic [21]. Affine arithmetic is a kind of interval arithmetic that can be used to compute the influence of independent sources of uncertainty to a variable. The influence of the sources of uncertainty i to a variable $\hat{x}$ with a central value x_0 can be represented by a symbolic sum of terms $x_i\epsilon_i$, with ϵ_i representing an arbitrary noise symbol [21].

$$\hat{x} = x_0 + \sum_{i=1}^{n} x_i\epsilon_i \qquad \epsilon_i \in [-1,1] \qquad (3.1)$$

The summation of different variables is defined by [21] as

$$\hat{x} \pm \hat{y} \pm \hat{z} = (x_0 \pm y_0 \pm z_0) + \sum_{i=1}^{n}(x_i \pm y_i \pm z_i)\epsilon_i \qquad \epsilon_i \in [-1,1] \qquad (3.2)$$

and multiplication with a gain factor is defined by [21] as

$$c\hat{x} = cx_0 + \sum_{i=1}^{n} cx_i\epsilon_i \qquad \epsilon_i \in [-1,1] \qquad (3.3)$$

To analyse the sensor driver system using affine arithmetic, let the variables be defined as follows:

$\hat{x}$ = Linearity (% FSO)

$\hat{y}$ = Sensitivity (V/mm)

$\hat{z}$ = Temperature stability (%FSO /°C)

The total performance of the sensor driver P_{tot} can therefore be defined as

$$P_{tot} = \hat{x} + \hat{y} + \hat{z} = (x_0 + y_0 + z_0) + \sum_{i=1}^{n}(x_i + y_i + z_i)\epsilon_i \qquad \epsilon_i \in [-1,1] \qquad (3.4)$$

Each variable can in turn be expanded to include the main functional units, as well as sub-units.

3.5.1.2 Linearity

The linearity of the system can be expressed as follows:

$$\hat{x} = x_0 + x_1\epsilon_1 + x_2\epsilon_2 + x_3\epsilon_3 + x_4\epsilon_4 + x_5\epsilon_5, \qquad \epsilon_{1,}\epsilon_{2,} \dots, \epsilon_5 \in [-1,1],$$

$$= x_0 + x_1\epsilon_1 + (x_{2.1} + x_{2.2})\epsilon_2 + x_3\epsilon_3 + (x_{4.1} + x_{4.2} + x_{4.3} + x_{4.4} + x_{4.5})\epsilon_4 + x_5\epsilon_5 \qquad (3.5)$$

where

x_0= 0

x_1: Power supply linearity

x_2: Excitation circuit linearity

$x_{2.1}$: Oscillator circuit linearity

$x_{2.2}$: V/I amplifier linearity

x_3: Sensor linearity

x_4: Signal conditioning circuit linearity

$x_{4.1}$: Signal amplifier linearity

$x_{4.2}$: Band-pass filter linearity

$x_{4.3}$: Amplitude demodulator linearity

$x_{4.4}$: Low-pass filter linearity

$x_{4.5}$: Gain and scaling amplifier linearity

x_5: ADC linearity

3.5.1.3 Sensitivity

Since the sensitivity of the system is given as V/mm and not as a percentage value, it cannot be expressed in terms of summation. It is instead given as the product of the sensor's sensitivity with the gain factor of the signal conditioning circuit.

$$\begin{aligned} \hat{y} &= c_4 y_3 \\ &= (c_{4.1} \times c_{4.2} \times c_{4.4} \times c_{4.5}) y_3 \end{aligned} \tag{3.6}$$

where

c_4: Signal conditioning circuit gain

$c_{4.1}$: Signal amplifier gain

$c_{4.2}$: Band-pass filter gain

$c_{4.4}$: Low-pass filter gain

$c_{4.5}$: Gain and scaling amplifier gain

y_3: Sensor sensitivity

3.5.1.4 Temperature stability

The temperature stability of the system ($\hat{z}$) can again be expressed as the summation of terms, due to the fact that it is given as a percentage value increase per degree Celsius. It is therefore expressed as

$$\hat{z} = z_0 + z_1\epsilon_1 + z_2\epsilon_2 + z_3\epsilon_3 + z_4\epsilon_4 + z_5\epsilon_5 \qquad \epsilon_{1,}\epsilon_{2,} \dots, \epsilon_5 \in [-1,1] \tag{3.7}$$

Since the temperature stability of the sensor and sensor controller are separately specified, they can also be expressed separately and independently as follows:

$$\begin{aligned} \hat{z}_s &= z_0 + z_1\epsilon_1 + z_2\epsilon_2 + z_3\epsilon_3 \\ &= z_0 + z_1\epsilon_1 + (z_{2.1} + z_{2.2})\epsilon_2 + z_3\epsilon_3 \end{aligned} \tag{3.8}$$

$$\begin{aligned} \hat{z}_c &= z_0 + z_4\epsilon_4 + z_5\epsilon_5 \\ &= z_0 + (z_{4.1} + z_{4.2} + z_{4.3} + z_{4.4} + z_{4.5})\epsilon_4 + z_5\epsilon_5 \end{aligned} \tag{3.9}$$

where

$\hat{z}_s$: Temperature stability for sensor unit

$\hat{z}_c$: Temperature stability for sensor controller unit

z_0: 0

z_1: Power supply temperature stability

z_2: Excitation circuit temperature stability

- $z_{2.1}$: Oscillator circuit temperature stability
- $z_{2.2}$: V/I amplifier temperature stability

z_3: Sensor temperature stability

z_4: Signal conditioning circuit temperature stability

- $z_{4.1}$: Signal amplifier temperature stability
- $z_{4.2}$: Band-pass filter temperature stability
- $z_{4.3}$: Amplitude demodulator temperature stability
- $z_{4.4}$: Low-pass filter temperature stability

$z_{4.5}$: Gain and scaling amplifier temperature stability

z_5: ADC temperature stability

3.5.2 Specification estimates

Since affine arithmetic is used in this instance to perform a semi-symbolic simulation of the system, an estimate for specification values can be obtained by letting $\epsilon_{1,}\epsilon_{2,}\ldots,\epsilon_5$ represent integer values in the range $[-1,1]$, therefore $\epsilon_1 = \epsilon_2 = \epsilon_3 = \epsilon_4 = \epsilon_5 = \pm 1$. By assigning integer values to the noise symbols, the system analysis corresponds to one simulation run. By combining the affine arithmetic expressions with the specifications set for the sensor driver, a general specification for each main functional unit can be obtained.

3.5.2.1 Linearity estimate

A general functional unit specification for linearity is obtained as follows:

$$\hat{x} = x_1\epsilon_1 + x_2\epsilon_2 + x_3\epsilon_3 + x_4\epsilon_4 + x_5\epsilon_5 \tag{3.10}$$

$$\hat{x} = \pm x_1 \pm x_2 \pm x_3 \pm x_4 \pm x_5 = \pm 17.5\%\ \text{FSO}$$

$$\therefore \hat{x} = \pm 1.5\% \pm 1.5\% \pm 11.14\% \pm 1.5\% \pm 1.5\% < \pm 17.5\%\ \text{FSO}$$

The linearity of the functional units are equally divided as ±1.5 %. The linearity of the system will however be improved through linearization by the digital processing unit. This will ensure that the system linearity will be much less than the specified $\pm 17.5\ \%$ FSO,therefore meeting the system's linearity requirement specification.

3.5.2.2 Sensitivity estimate

The sensitivity of the sensor driver system is determined by the measuring range of the sensor and the voltage input range of the ADCs.

$$\hat{y} = c_4 y_3 \geq 8\ \text{V/mm}$$

3.5.2.3 Temperature stability estimate

During testing of the PCB sensor, measuring problems such as oscillator amplitude and frequency drift meant that the temperature stability of the sensor could not be determined [7]. A general functional unit specification for temperature stability is obtained for both the sensor and sensor controller as follows:

$$\hat{z}_s = z_1\epsilon_1 + z_2\epsilon_2 + z_3\epsilon_3 \tag{3.11}$$

$$\hat{z}_s = \pm z_1 \pm z_2 \pm z_3 = 0.05\ \%\ \text{FSO/℃} = 500\ \text{ppm/℃}$$

$$\therefore \hat{z}_s = \pm 100\ \text{ppm/℃} \pm 250\ \text{ppm/℃} \pm z_3 = 500\ \text{ppm/℃}$$

The general functional unit temperature stability specification for the sensor controller is obtained as follows:

$$\hat{z}_c = z_4\epsilon_4 + z_5\epsilon_5 \tag{3.12}$$

$$\hat{z}_c = \pm z_4 \pm z_5 = 0.025\ \%\ \text{FSO/℃} = 250\ \text{ppm/℃}$$

$$\therefore \hat{z}_c = \pm 200\ \text{ppm/℃} \pm 50\ \text{ppm/℃} = 250\ \text{ppm/℃}$$

3.5.2.4 Sensor driver requirement specification

- **Power supply**
  - Linearity: $\pm 1.5\ \%$
  - Temperature stability: ± 100 ppm/°C
- **Excitation circuit**
  - Linearity: $\pm 1.5\ \%$
  - Temperature stability: ± 250 ppm/°C
- **Signal conditioning circuit**
  - Linearity: $\pm 1.5\ \%$
  - Temperature stability: ± 200 ppm/°C
- **ADC**
  - Linearity: $\pm 1.5\ \%$
  - Temperature stability: ± 50 ppm/°C

3.6. Conclusion

This chapter researched existing eddy current sensors to acquire requirement specifications for the sensor driver system as a whole. In order to obtain the final requirement specifications, a functional analysis and allocation of the sensor driver system was done. These were then used together with affine arithmetic to determine the specification estimates for the performance parameters of all the sub-systems of the sensor driver system.

Chapter 4

Sensor driver analogue design

This chapter presents the design of the analogue circuits of the sensor driver system. Each functional unit must adhere to the specifications set in chapter 3, and various designs are considered for each functional unit. The design of each functional unit is given, which consists of the conceptual design, detail design and specifications of all the performance parameters. In order to verify the concept of the sensor driver, two test circuits were designed and built, and will also be discussed.

4.1 Functional units

As discussed in chapter 3, the sensor driver system consists of six main functional units, each with its own set of sub-units. These are:

1. Power supply circuit
2. Excitation circuit
    a. Oscillator circuit
    b. Voltage-to-current converter
3. PCB sensor (transmission lines)
4. Signal conditioning circuit
    a. Signal amplifier
    b. Band-pass filter
    c. Amplitude demodulator
    d. Low-pass filter
    e. Gain and scaling amplifier
5. Analogue to digital converters
6. Digital processing circuit

As the PCB sensor has already been designed and constructed [7], the only sensor design aspect of importance to the sensor driver system is the transmission line design. The detail design of all these main- and sub-units will now be discussed.

4.2 Power supply

The power supply circuit is responsible for converting the isolated +24 V DC received from the power bus into the different voltages required by the sensor driver circuit. Since the power supply circuit is responsible for supplying power to all the sensor driver components, it is included in the sensor driver performance parameters' specifications.

4.2.1 Power supply requirement specifications

The power supply circuit is required to provide the following voltages to the different parts of the sensor driver circuit:

- ±15 V output voltage (analogue)
- ±5 V output voltage (analogue)
- +5 V output voltage (digital)
- +24 V input voltage
- Balanced output
- Regulated output
- ±1.5% output accuracy
- >1 A output current
- ±0.015%/°C temperature stability

4.2.2 Power supply circuit design

4.2.2.1 Conceptual design for power supply circuit

The design of the power supply circuit for the sensor driver test circuit consists of a series of linear voltage regulators and an inverting DC-to-DC converter. The first linear voltage regulator receives the supplied voltage of 24 V DC as input, and generates a regulated +15 V. This forms the positive supply to all devices requiring a ±15 V dual supply. This regulated voltage also forms the input to two linear +5 V voltage regulators, one supplying the analogue positive supply to devices requiring ±5 V dual supply, and the other supplying the digital input voltage to all digital devices in the sensor driver circuit. The analogue +5 V voltage is also supplied as input voltage to an inverting DC-to-DC converter which converts its positive input voltage into a negative -15 V output voltage. This output voltage in turn forms the negative supply to all devices requiring a ±15 V dual supply. The negative output voltage is then lastly regulated by a -5 V linear voltage regulator to supply the negative supply to devices requiring ±5 V dual supply.

Figure 4-1 shows the functional diagram for the power supply circuit. Since each regulator consists of an internal closed loop, the performance parameters of each dual supply consists of only the performance parameters of the positive and negative supply which make up that specific dual supply. Each supply is therefore only responsible for its own performance, and does not influence the supplies preceding or succeeding it.

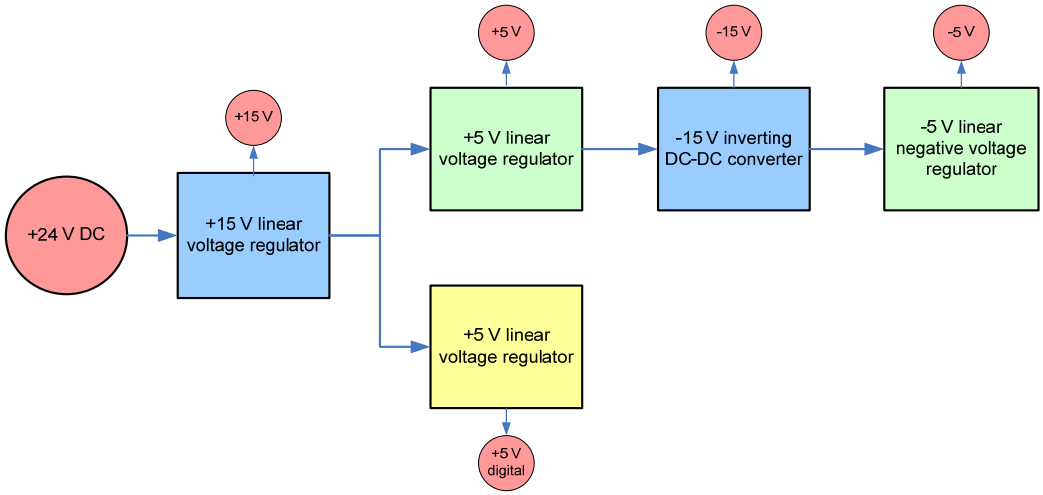


Figure 4-1 Power supply functional diagram

4.2.2.2 Detail design for power supply circuit

The following components were chosen for the design:

- **+15 V linear low drop-out (LDO) regulator:**
  - **LT1085**: Adjustable 3 A Low-Dropout Positive Adjustable Regulator [23]
- **+5 V linear LDO regulator:**
  - **TL750M05** Low-Dropout Voltage Regulator [24]
- **-15 V inverting DC/DC converter:**
  - **LT1931:** 1.2MHz/2.2MHz Inverting DC/DC Converter in ThinSOT [25]
- **-5 V linear LDO regulator:**
  - **UCC284-5** Low-Dropout 0.5 A Negative Linear Regulator [26]

The component selection was based on the power dissipation capabilities and output stability of each regulator. An estimate of the power dissipation of the sensor driver circuit was determined by summing the power dissipation of each IC in the circuit together with the power dissipation of the sensor excitation coil.

The power dissipation of the operational amplifiers is given by the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs [22]. The quiescent power is given by the voltage between the supply pins times the quiescent current. The drive power of the device is given by the difference between the total drive power and the load power. Equation (4.1) gives the calculation of the power dissipated in the operational amplifier package.

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L} \quad (4.1)$$

P_D is the power dissipated in the package, V_S the total supply voltage, I_S the supply (quiescent) current, and V_{OUT} the output voltage.

After simplifying (4.1), (4.2) can be derived.

$$P_D = (V_S \times I_S) + I_O \left(\frac{V_S}{2} - V_{OUT}\right) \quad (4.2)$$

The estimated maximum total power dissipation of the sensor driver circuit is determined using the specifications of each device, the maximum output current, and the output voltage of each device.

$$P_{D(TOTAL)} = P_{D(LM7171)} + P_{D(LM7372)} + P_{D(AD637)} \times 2 + P_{D(AD8099_1)} + P_{D(AD8099_2)} \times 2 + P_{D(LT1568)} \times 2 + P_{D(AD8099_3)} \times 2 + P_{D(PIC16F876A)} + P_{D(AD9833)} + P_{D(coil)} \quad (4.3)$$

$$= \left[(6.5\ \text{mA} \times 30\ \text{V}) + \left(100\ \text{mA} \times \left(15\ \text{V} - 12\ \text{V}\right)\right)\right] + \left[(6.5\ \text{mA} \times 30\ \text{V}) + \left(150\ \text{mA} \times 15\ \text{V} - 12\ \text{V} + 108\ \text{mW} \times 2 + 14.5\ \text{mA} \times 10\ \text{V}\right) + 80\ \text{mA} \times 5\ \text{V} - 1.2\ \text{V} + 14.5\ \text{mA} \times 10\ \text{V} + 80\ \text{mA} \times 5\ \text{V} - 3.8\ \text{V} \times 2 + 10\ \text{mA} \times 10\ \text{V} + 100\ \text{mA} \times 5\ \text{V} - 4.75\ \text{V} \times 2 + 14.5\ \text{mA} \times 10\ \text{V} + 80\ \text{mA} \times 5\ \text{V} - 3.8\ \text{V} \times 2 + 4\ \text{mA} \times 5\ \text{V} + 25\ \text{mA} \times 5\ \text{V} - 4.9\ \text{V} + 20\ \text{mW} + [113.2\ \text{mA} \times 12\ \text{V}]$$

$$= 495\ \text{mW} + 645\ \text{mW} + 108\ \text{mW} \times 2 + 450\ \text{mW} + 241\ \text{mW} \times 2 + 125\ \text{mW} \times 2 + 241\ \text{mW} \times 2 + 22.5\ \text{mW} + 20\ \text{mW} + 1.36\ \text{W}$$

$$= 4.4225\ \text{W}$$

Due to the fact that the power supply consists of a series of regulators, all following the first +15 V regulator, the entire circuit's power is drawn from that regulator. It is therefore necessary to

determine what the maximum junction temperature of the regulator will be at the maximum power of the circuit. The junction temperature of the regulator is given by (4.4)

$$T_J = T_A + P_D\theta_{JA} \tag{4.4}$$

$$= 25° \text{ C} + 4.4225 \text{ W} \times 30 ° \text{C/W}$$

$$= 157.68 ° \text{C}$$

The maximum junction temperature of the LT1085 is 150 °C. As can be seen from (4.3) the junction temperature is relatively close to the maximum junction temperature. Since the power dissipation of the sensor driver circuit was determined using the maximum output current of each device, the calculated power dissipation will in practice not be realised. This means that the calculated junction temperature of the LT1085 will also in practice not be reached. The type of +15 V voltage regulator was chosen based on how close the different devices' junction temperatures came to the maximum junction temperatures using (4.4). The LT1085 came the closest and was therefore chosen for implementation in the sensor driver.

4.2.2.3 Circuit schematic of power supply

The circuit schematic for this design is shown in Figure 4-2. The +5 V digital voltage supply is separated from the other power supplies by means of an EMI filter. This prevents any high-speed switching noise of the digital circuit from leaking into the power supply signals of the analogue circuit.

4.2.2.4 Performance parameter specifications

- ***Power supply linearity***

The linearity of this design is mainly determined by the output accuracy of the components. The voltage output of both the regulators and the inverting DC/DC converter are determined by either a resistor value, or a voltage divider network. Since the voltage level accuracy is not the main concern in this instance, the tolerances of the resistors can be ignored with regards to the linearity of the circuit. The circuit linearity is therefore only determined by the output accuracy of the voltage regulator and inverting DC/DC converter.

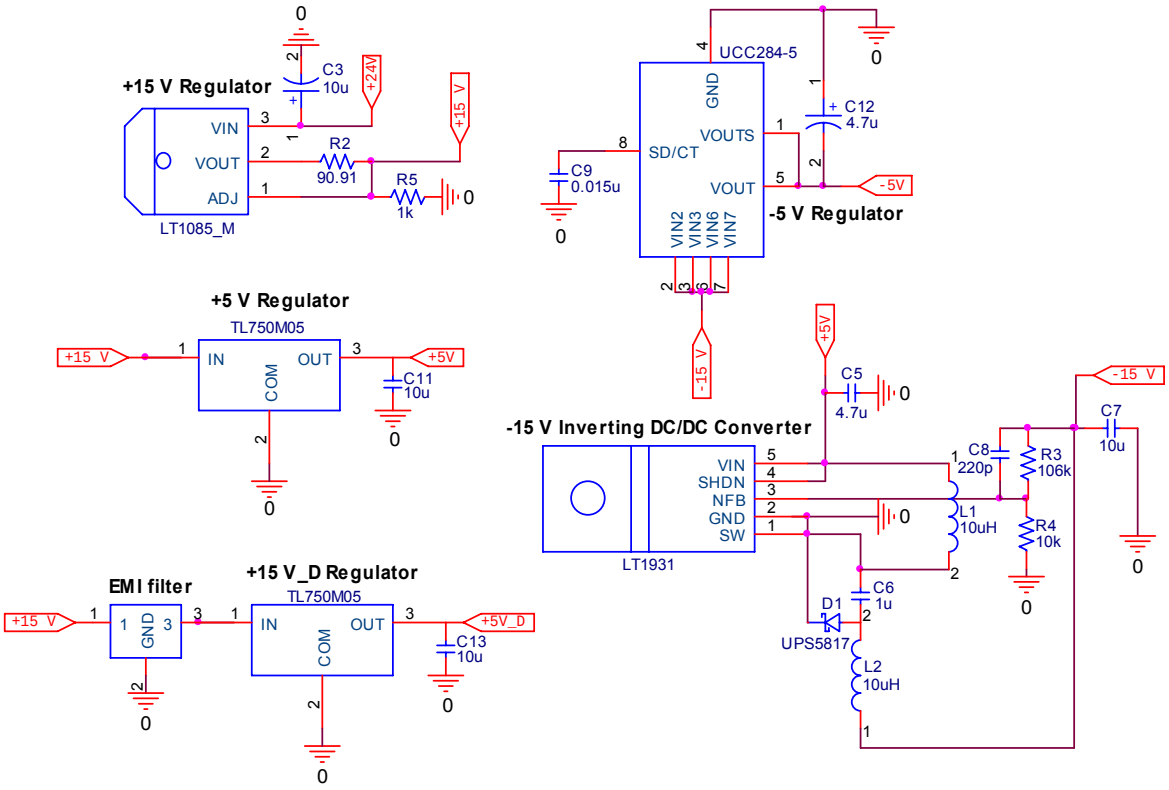


Figure 4-2 Power supply design circuit schematic

The linearity of the positive and negative supplies of the two dual and one single supply is given separately as follows:

- **±15 V supply:**
  - **+15 V supply**: LT1085 linear LDO regulator
    - Output accuracy: ±1 % @ 25°C [23]
  - **-15 V supply**: LT1931 inverting DC/DC converter
    - Output accuracy: ±1.6 % @ 25°C [25]

∴ **Total output accuracy ±15 V supply: ±1.3 %**

- **±5 V supply:**
  - **+5 V supply:** TL750M05 linear LDO regulator
    - Output accuracy: ±1 % @ 25°C [24]
  - **-5 V supply:** UCC284-5
    - Output accuracy: ±1.5 % @ 25°C [26]

∴ **Total output accuracy ±5 V supply: ±1.25 %**

- **+5 V supply:**
  - **+5 V supply**: TL750M05 linear LDO regulator
    - Output accuracy: ±1 % @ 25°C [24]

∴ Total output accuracy +5 V supply: ±1 %

➢ *Power supply temperature stability*

The temperature stability of the circuit is given by the output accuracy of the regulators and inverting DC/DC converter measured over their entire operating temperature range.

- **±15 V supply:**
  - **+15 V supply:** LT1085 linear LDO regulator [23]
    - Output accuracy: ±1.6 % over entire temperature range
    - Temperature range: -40°C to +125°C
    - Temperature stability = $\frac{\pm 0.6\%}{125℃-25℃} = \pm 0.006\ \%/℃$
    - Output accuracy (-40°C to +85°C) = $\pm 1\ \% + (\pm 0.006 \times 60℃)$ = ±1.36%
  - **-15 V supply:** LT1931 inverting DC/DC converter [25]
    - Output accuracy: ±2 %
    - Temperature range: -40°C to +85°C
    - Temperature stability = $\frac{\pm 1\%}{85℃-25℃} = \pm 0.0167\ \%/℃$
  - ±15 V output accuracy over -40°C to +85°C temperature range: ±1.68 %

∴ ±15 V temperature stability = $\frac{\pm \mathbf{1.68}\%-\pm \mathbf{1.3}\ \%}{\mathbf{85}℃-\mathbf{25}℃} = \mathbf{0.0063}\ \%/℃ = \mathbf{63.3\ ppm}/℃$

- **±5 V supply:**
  - +5 V supply: TL750M05 linear LDO regulator [24]
    - Output accuracy: ±2 %
    - Temperature range: -40°C to +125°C
    - Temperature stability = $\frac{\pm 1\%}{125℃-25℃} = \pm 0.01\ \%/℃$
    - Output accuracy (-40°C to +85°C) = $\pm 1\ \% + (\pm 0.01 \times 60℃)$ = ±1.6%
  - -5 V supply: UCC284-5 negative linear LDO regulator [26]
    - Output accuracy: ±2 %
    - Temperature range: -40°C to +85°C
    - Temperature stability = $\frac{\pm 1\%}{85℃-25℃} = \pm 0.0167\ \%/℃$
  - ±5 V Total output accuracy over -40°C to +85°C temperature range: ±1.8 %

∴ ±5 V Total temperature stability = $\frac{\pm \mathbf{1.8}\ \%-\pm \mathbf{1.25}\ \%}{\mathbf{85}℃-\mathbf{25}℃} = \mathbf{0.00917}\ \%/℃ = \mathbf{91.67\ ppm}/℃$

- **+5 V supply:**
  - +5 V supply: TL750M05 linear LDO regulator [24]
    - Output accuracy: ±2 %
    - Temperature range: -40°C to +125°C
    - Temperature stability = $\frac{\pm 1\%}{125℃-25℃} = \pm 0.01\ \%/℃$
    - Output accuracy (-40°C to +85°C) = $\pm 1\ \% + (\pm 0.01 \times 60℃)$ = ±1.6%
  - +5 V Total output accuracy over -40°C to +85°C temperature range: ±1.6 %

∴ **+5 V Total temperature stability =** $\frac{\pm \mathbf{1.6}\ \% - \pm \mathbf{1}\ \%}{\mathbf{85}℃-\mathbf{25}℃} = \mathbf{0.01}\ \%/℃ = \mathbf{100\ ppm}/℃$

4.2.3 Power supply performance parameters summary

Although this design requires five regulator devices, the component count is not very high and the circuit is quite simple. Each power supply's output accuracy and temperature stability of is well within the set requirements for the power supply circuit.

- **Required performance parameters:**
  - Linearity: $\pm 1.5\ \%$
  - Temperature stability: ± 100 ppm/°C

- **Estimated achievable performance parameters:**
  - Linearity:
    - ±15 V supply: **±1.3 %** < ±1.5 % required
    - ±5 V supply: **±1.25 %** < ±1.5 % required
    - +5 V supply: **±1 %** < ±1.5 % required
  - Temperature stability:
    - ±15 V supply: **63.3 ppm/°C** < 100 ppm/°C required
    - ±5 V supply: **91.67 ppm/°C** < 100 ppm/°C required
    - +5 V supply: **100 ppm/°C** ≤ 100 ppm/°C required

4.3 Excitation circuit

The excitation circuit is responsible for delivering the required 2 MHz sine wave excitation signal to the excitation coil of the sensor. As already mentioned, the excitation circuit consists of two sub-circuits, namely an oscillator circuit, and a voltage-to-current-converter circuit. The design of each will now be discussed.

4.3.1 Oscillator circuit

The oscillator circuit generates a sine wave at the required frequency of 2 MHz. The most important performance parameters of the oscillator circuit are its linearity, frequency stability, and temperature stability.

4.3.1.1 Requirement specifications of oscillator circuit

The requirement specifications for the oscillator circuit were obtained from the specifications estimate discussed in chapter 3, as well as from requirements obtained during testing of the PCB sensor. The requirement specifications for the oscillator circuit are as follows:

- Sine wave output
- Amplitude stability < 300 ppm
- Frequency stability < 100 ppm
- Temperature stability < 250 ppm/°C

4.3.1.2 Circuit design of oscillator circuit

Three different oscillator designs were evaluated for implementation in the project by designing and constructing a test board featuring all three oscillator designs and evaluating each. The chosen design consists of the AD9833 programmable waveform generator capable of producing sine, triangular, and square wave outputs. The output frequency and phase are software programmable, and no external components are necessary, apart from decoupling capacitors, a crystal oscillator, and a controller or processor with which the device is programmed. The AD9833 features a 28-bit frequency register, and can achieve a 0.1 Hz resolution with a 25 MHz clock rate. Programming entails writing to the device via a 3-wire serial interface such as SPI or I^2C at clock rates up to 40 MHz, and is compatible with DSP and microcontroller standards. The measurement results of the oscillator test circuit will be discussed in Chapter 7.

The AD9833 consists of a fully integrated direct digital synthesis (DDS) chip, which is capable of performing a wide range of simple and complex modulation schemes. Due to the fact that these modulation schemes are implemented in the digital domain, it allows for accurate and simple realization of complex modulation algorithms using DSP techniques. The internal circuitry of the AD9833 consists of a numerically controlled oscillator (NCO), frequency and phase modulators, SIN ROM, a digital-to-analogue converter (DAC) and a regulator.

4.3.1.3 Component selection for oscillator circuit

Apart from the programmable waveform generator, the oscillator circuit design requires only a microcontroller. The following components were chosen for the design:

Programmable waveform generator: AD9833 Low Power Programmable Waveform Generator from Analog Devices. [27]

Microcontroller: PIC16F876A 28-pin Enhanced Flash Microcontroller from Microchip.

The PIC16F876A microcontroller was chosen because of familiarity with the chip. In the final sensor driver design, the functions of the PIC16F876A will be performed by the digital processing circuit.

The AD9833 has an output frequency range of up to 12.5 MHz and a DAC resolution of 10 bits. It requires a 5 V supply voltage, and has a maximum output voltage of 0.65 V. Its voltage output temperature coefficient is 200 ppm/°C.

4.3.1.4 Circuit schematic of oscillator circuit

Figure 4-3 shows the circuit schematic of the oscillator circuit design. As already mentioned, the PIC16F876A microcontroller from Microchip is used in this design. The microcontroller writes to the AD9833 using SPI communication. A crystal oscillator is used to provide the AD9833 with its master clock. As can be seen from the figure, only a few external components are required for this design.

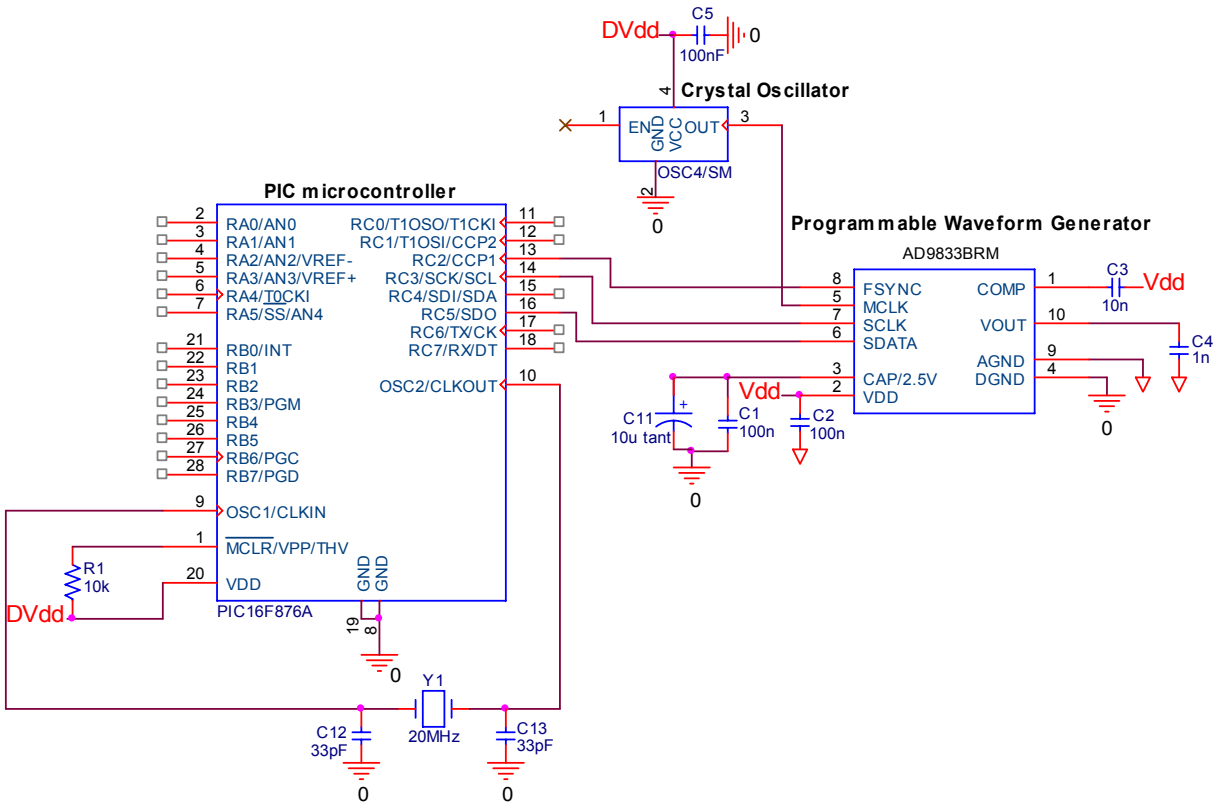


Figure 4-3 Oscillator circuit schematic

4.3.1.5 Performance parameter specifications for oscillator circuit

- **Linearity of oscillator circuit**

The linearity of the oscillator circuit is mostly determined by the conversion error and differential nonlinearity (DNL) of the DAC of the AD9833. The DAC has an update rate of 25 MSPS and a 10-bit resolution. For a sine wave of 2 MHz, the conversion error as estimated from simulation was determined to be around 0.782 %. This rather large conversion error can however be overcome by adjusting the output frequency to a factor of the sampling frequency of 25 MHz. The frequency was therefore adjusted to $2.083\dot{3}$ MHz (since $2.083\dot{3} \times 8 = 25$). This eliminated the conversion error completely, resulting in an amplitude output that is stable throughout. One of the main advantages of the AD9833 is highlighted by this issue, namely the ability to adjust the frequency for optimal response. Another advantage of the AD9833 is that its output stability is independent of power supply stability.

- **AD9833 programmable waveform generator [27]:**
  - Conversion error @ 2.0833 MHz: 0 %
  - Differential nonlinearity: ±0.5 LSB

$$= \frac{0.6}{2^{10}} \times 0.5 \times 100\ \%$$
$$= 29.3 \times 10^{-3}\ \%$$
$$= 293\ \text{ppm}$$

∴ **Total linearity of oscillator circuit: 0.0293% = ±293 ppm**

4.3.1.6 Frequency stability of oscillator circuit

The AD9833 generates sine waves by deriving the phase from the programmed frequency as follows:

$$\Delta Phase = \frac{f \cdot 2^{28}}{f_{MCLK}} \tag{4.5}$$

It then uses this digital phase information as an address to a look-up table and converts the phase information into amplitude. Due to the fact that the frequency is programmed by the user, the only variable that can influence output frequency accuracy and phase noise is the master clock or digital clock input. Therefore the frequency stability is equal to that of the crystal oscillator used.

- **Crystal oscillator:**
  - Typical frequency stability at room temperature: 50 ppm

∴ **Total frequency stability of oscillator circuit: 50 ppm**

4.3.1.7 Temperature stability of oscillator circuit

- **AD9833 [27]:**
  - V_{OUT} Temperature coefficient: 200 ppm/°C
  - Operating temperature range: -40°C to +105°C
- **Crystal:**
  - Operating temperature range: 0°C to +70°C
  - Frequency temperature coefficient: 1.43 ppm/°C

∴ **Total temperature stability of oscillator circuit:**
  - **Amplitude: 200 ppm/°C**
  - **Frequency: 1.43 ppm/°C**

4.3.2 Voltage-to-current converter

The voltage-to-current converter (V-I converter) amplifies the sine wave output signal of the oscillator circuit to the required voltage, and converts the voltage signal into the required controlled current signal for the excitation coils of the sensor. The requirements for the voltage-to-current circuit are obtained from the physical requirements of the excitation signals and are discussed next.

4.3.2.1 Requirement specifications of V-I converter

The fact that the excitation signal is at a high-frequency (2 MHz) results in certain requirements being set in order for the excitation circuit to function properly, for example a very fast slew rate and high gain bandwidth product. The requirement specifications for the voltage-to-current converter circuit are as follows:

- ±15 V supply voltage
- ±12 V output voltage
- 100 mA output current
- Slew rate ≥ 96 V/µs
- Gain bandwidth product ≥ 100 MHz
- ±0.5 % output accuracy
- ±0.01 %/°C temperature stability (100 ppm/°C)

4.3.2.2 Circuit design of V-I converter

The design of the voltage-to-current converter consists of two stages. The first stage is the voltage gain stage, and consists of a low noise, high speed operational amplifier and a high speed, high output current voltage feedback amplifier. The second stage is the voltage-to-current converting stage, and consists of a high speed, high output current operational amplifier. This design was chosen to eliminate noise caused by switching transistors in traditional power drive circuits. The first stage provides a high gain amplification of the oscillator output signal, and the second provides conversion from voltage to current. In the original sensor design, the excitation coil was driven with a ±15 V, 141 mA sine wave (10.6 V_{RMS}, 100 mA_{RMS}). Due to the unavailability of operational amplifiers capable of operating rail-to-rail at ±15 V, it was decided to use an output voltage of ±12 V. The current output level therefore must be adjusted in order to keep the inductance of the excitation coil as close as possible to the inductance calculated with the original excitation signal. As shown in (4.6), the inductance of the excitation coil is

determined by the reactance of the coil and the excitation frequency. By keeping the reactance of the coil the same, the coil inductance will also be the same.

$$L_{em} = \frac{X_{exc}}{2\pi f} \tag{4.6}$$

For the original excitation signal it was assumed that the reactance of the coil would make up 95% of the impedance, and was calculated to be 100.7 Ω. Therefore, to keep the inductance the same as for the original excitation signal using a ±12 V excitation signal, the excitation current is calculated as follows:

$$I_{RMS} = \frac{V_{RMS} \times 0.95}{X_{exc}} \tag{4.7}$$

$$= \frac{8.485\ \mathrm{V_{RMS}} \times 0.95}{100.7\ \Omega}$$

$$= 80.047\ \mathrm{mA_{RMS}}$$

$$\therefore I_{RMS} = \pm 113.2\ \mathrm{mA}$$

The voltage and current input to the sensor is therefore lowered to ±12 V (8.485 V_{RMS}) and ±113.2 mA (80.047 mA_{RMS}).

The functions of the circuit are shown in Figure 4-4. The sine wave from the oscillator circuit is amplified to the required voltage value, and then converted to a controlled current for the excitation coil of the sensor.

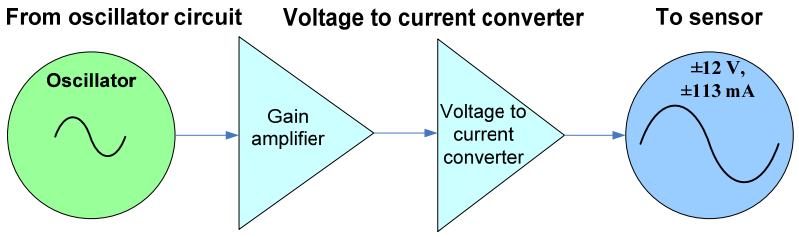


Figure 4-4 Voltage-to-current converter functional diagram

4.3.2.3 Component selection for V-I converter

The following components were chosen for the design:

- **Gain amplifiers:**
  - **AD8099** Ultralow distortion, high speed, low noise operational amplifier [22].
  - **LM7171** Very high speed, high output current, voltage feedback amplifier [28].
- **V to I converting amplifier:**
  - **LM7372** High speed, high output current, dual operational amplifier [29].
- **Gain and load resistors:**
  - Trimming potentiometers

The AD8099 was chosen due to its low voltage noise, low offset voltage and drift, very high slew rate of 1350 V/ µs and exceptionally high gain bandwidth product of 3.8 GHz. It has an input offset voltage of 0.5 mV and input voltage noise of 0.95 nV/$\sqrt{\text{Hz}}$. The device requires a supply voltage of ±5 V, and has an output voltage swing of ±3.8 V [22]. In order to achieve the required excitation voltage amplitude, an output voltage of at least ±12 V is needed. Therefore, a second operational amplifier with a supply voltage of ±15 V and output voltage swing of at least ±12 V is needed. This second gain function is performed by the LM7171 op-amp.

The LM7171 has a very high slew rate of 4100 V/µs and 200 MHz gain bandwidth product. It has an output voltage swing of ± 12.7 V and can supply 100 mA output current [28]. It was chosen due to its very high slew rate, output voltage swing and high gain bandwidth product. The LM7171 amplifies the sine wave signal from the first op-amp to the ±12 V voltage signal required. The LM7372 op-amp then converts the voltage signal to the required controlled current signal.

The LM7372 was chosen due to its high output current of 150 mA and output voltage swing of ± 13 V. It also has a slew rate of 3000 V/µs and a 120 MHz gain bandwidth product [29]. The LM7372 converts the ±12 V voltage signal into a controlled 113.2 mA current signal needed to excite the excitation coils of the sensor. The circuit schematic and circuit simulations will explain the design in more detail.

4.3.2.4 Circuit schematic and simulations for V-I converter

The circuit schematic for the design of the voltage-to-current converter is shown in Figure 4-5.

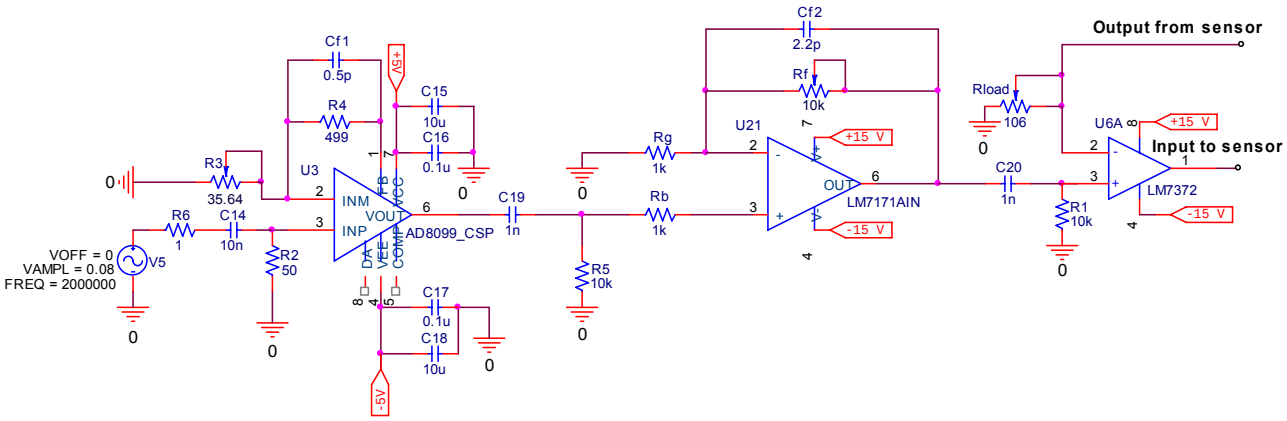


Figure 4-5 Voltage to current converter circuit schematic

R_3, Rf, and R_{load} are precision trimming potentiometers (trimpots), in order for the gain and current to be accurately fine-tuned. In the final circuit, all trimming potentiometers will be replaced with high accuracy fixed resistors. C_7, C_1, and C_6 are used to perform ac-coupling of both the input signal from the oscillator circuit, as well as the output signals of the circuit to the sensor excitation coils by acting as a high-pass filter. By implementing ac-coupling, all dc current is removed. Since the input offset voltage and current parameters for the op amp are dc parameters, they can therefore also be eliminated.

The output of the oscillator circuit was measured as 160 mV_{p-p}. This output forms the input signal to the first stage gain amplifiers of the circuit. The required gain for the first gain amplifier is determined as 15 V/V. The output of this first stage amplifier forms the input to the second gain amplifier, of which the required gain is determined as 10 V/V. The total gain for the voltage to current converter circuit is therefore 150 V/V in order to amplify the oscillator signal to the required level of ±12 V. The second stage voltage to current converting amplifier converts its input voltage into output current. The amplifier also uses a sense resistor to sense the voltage across the sensor excitation coil, and controls the output current according to the difference between the input and sensor output voltage. The amplifier thus controls the current applied to the sensor excitation coil, keeping the current amplitude constant at 113.2 mA. Figure 4-6 shows the simulated first stage and second stage outputs of the circuit.

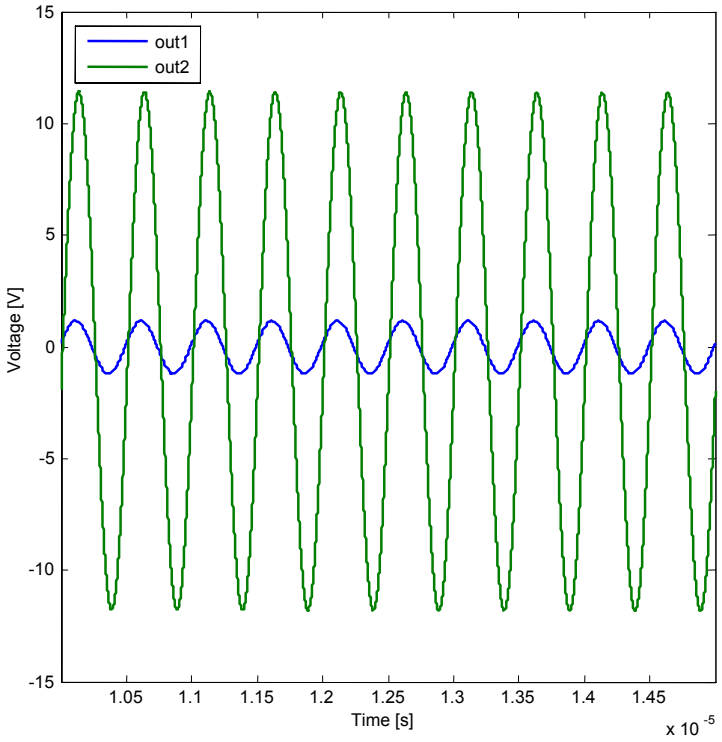


Figure 4-6 Voltage-to-current converter first stage and second stage outputs

Figure 4-7 shows the simulated controlled output current of the voltage-to-current converter.

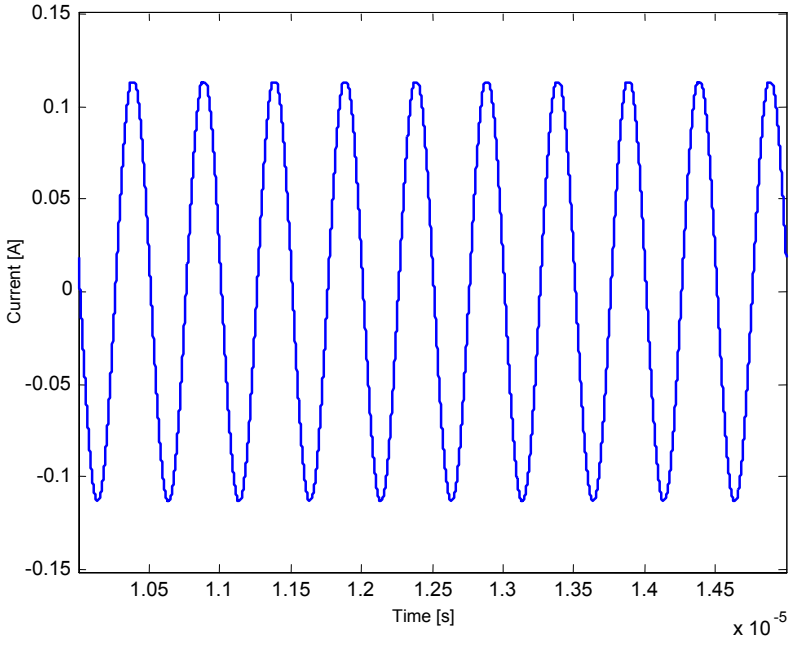


Figure 4-7 Current output of voltage-to-current converter

4.3.2.5 Performance parameter specifications for the V-I converter

- **Linearity of V-I converter**

The linearity of the voltage-to-current converter circuit is determined mainly by the differential gain error of the op amps, since the ac coupling removes the effect of the input offset voltage and drift. The differential gain for each op-amp is as follows:

- **AD8099 Op amp [22]:**
  - Differential gain: 0.025%
- **LM7171 Op-amp [28]:**
  - Differential gain: 0.01 %
- **LM7372 Op-Amp [29]:**
  - Differential gain: 0.01 %

∴ **Total linearity for V-I converter: 0.045% = 450ppm**

- **Temperature stability of V-I converter**

Due to the fact that the input offset voltage is removed by ac coupling, the temperature drift associated with that dc parameter can also be ignored. The temperature stability of the circuit is therefore given by the temperature coefficients of the resistors. The total temperature stability is determined by multiplying the maximum temperature coefficient of the components with the number of components. The temperature coefficient, number of components influencing the temperature stability of the design, and the operating temperature range of the components are as follows:

- **Resistors:**
  - Temperature coefficient: ±10 ppm/°C
  - Number of resistors: 6
  - Temperature range: -55°C to +125°C

∴ **Total temperature stability for V-I converter: ±60 ppm/°C (max)**

4.3.2.6 Summary of performance parameters for excitation circuit

In this section, the total estimated percentage of the performance parameters for the excitation circuit are calculated and compared to the set performance parameter requirements determined in chapter 3.

- **Required performance parameters:**
  - Linearity: $\pm 1.5\ \%$
  - Temperature stability: $\pm 250\ \text{ppm/°C}$
- **Estimated achievable performance parameters:**
  - Linearity: 293 ppm + 450 ppm = 737 ppm =**0.0737 %** << 1.5 % required
  - Temperature stability: 200 ppm/°C +60 ppm/°C = **260 ppm/°C** > 250 ppm/°C

The estimated achievable linearity is much better than the required linearity. The estimated achievable temperature stability is only slightly poorer than the required temperature stability, but still within a reasonable margin. As it is possible that the rest of the sensor driver's performance parameters can be less than specified, these error margins may yet be negligible. The excitation circuit design therefore adheres to its set of specification requirements .

4.4 Transmission lines

The transmission lines connect the excitation circuit with the sensor excitation coil, as well as the sensor sensing coils with the signal conditioning circuit of the sensor driver. As the signals being transmitted are high frequency and high accuracy signals, the selection of transmission lines is a very important aspect in the performance of the sensor system. The theory behind the transmission lines are briefly discussed, and two types of transmission lines are considered, namely twisted-pair cable and coaxial cable. The specifications for the sensor driver's transmission lines are then given, and two cables will be evaluated for implementation. The electrical model used to simulate the transmission lines is also presented and discussed, along with simulated results of the effect of variations in cable length.

4.4.1 Transmission line theory

A transmission line can be defined as the material medium or structure that forms all or part of a path from one place to another for directing the transmission of energy. In the case of wires connecting the components in an electronic circuit, the length of the wires can mostly be ignored. If the voltage on the wire at a given time changes in a time interval comparable to the time it takes for the signal to travel down the wire, the length of the wire becomes significant and the wire must be treated as a transmission line. A common rule of thumb for transmission lines is that when the length of the cable or wire is greater than a tenth of the wavelength of the signal travelling in the cable or wire, the cable or wire should be treated as a transmission line, and the circuit must be carefully designed using transmission line theory.

The wavelength of the signal transmitted to and from the sensor driver circuit is calculated as follows:

$$\lambda = \frac{v}{f} \tag{4.7}$$

$$= \frac{3 \times 10^8 \text{ m/s}}{2 \times 10^6 \text{ Hz}}$$

$$= 150 \text{ m}$$

where λ is the wavelength, v is the speed at which the signal is travelling, which is assumed to be at the speed of light (3×10^8 m/s), and f is the frequency of the signal (2 MHz). The length of the cables to be used in this project is 3 m, which is significantly less than the wavelength of the signal. This implies that the cables are not considered as transmission lines.

In the analysis of transmission lines, distributed constants must be used, since the time interval of voltage changes across the transmission line is comparable to the wavelength of the signal travelling on the line [31]. The analysis is done using an electrical model of the transmission line. The electrical model represents a transmission line of infinitesimal length with lumped constants assigned to it. The values of these constants are typically given per unit length. The electrical model of the transmission line is shown in Figure 4-8. This model will be used to simulate different cable types in order to select the best cable for implementation in the sensor driver.

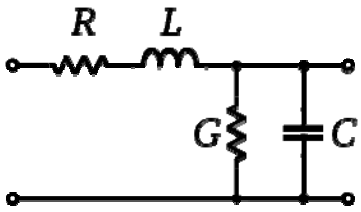


Figure 4-8 Circuit schematic representation of the elements of a transmission line

4.4.2 Cable type selection

Two types of cables are considered for possible implementation in the sensor driver. These are twisted shielded pair (TSP) cable, and coaxial cable. Each of these two types of cables will now be discussed shortly to motivate the cable type selection.

4.4.2.1 Twisted shielded pair cable

A twisted shielded pair cable is a cable in which two conductors are twisted together for the purposes of cancelling out electromagnetic interference (EMI) form external sources. The one conductor usually carries the forward signal and the other the return signal of a single circuit. TSP cables are used for transmitting low-level, low-frequency signals. This is because TSP cable provides for electromagnetic noise cancellation and shielding for both low and high frequencies. It also offers adequate bandwidth at a reasonable price. TSP cable is also flexible and easy to install. Figure 4-9 shows a 4 core twisted shielded pair cable.

Figure 4-9 Twisted shielded pair cable [30]

The twisting of the conductors in TSP cables causes cancellation of noise induced by magnetic fields by picking up the same noise signal as they pass very close to each other through the facility environment. This common mode noise signal can then be cancelled out by using

differential amplifiers. The shield around the twisted pair also provides some high-frequency noise signal attenuation.

The disadvantage of TSP is that it is not suitable for use with high-frequency systems with a bandwidth of more than 1 MHz. It is therefore not suitable for use in the sensor driver system, since the operating frequency of the system is 2 MHz.

4.4.2.2 Coaxial cable

For signal bandwidth of more than 1 MHz and distances more than 10 meters, coaxial cable must be used. The length of the run and the bandwidth of the signals to be transmitted therefore determine the type of cable to be used. In order to help eliminate noise pickup in high-frequency systems, differential data recording may be used just as it was used with TSP in low-frequency systems. To accomplish this, two cables must be run for each signal. This method is particularly effective if the gauge is designed to output a balanced signal. This method will however not work if the cable transit times are not identical to the order of a few hundred picoseconds. The cables must also be run next to each other so that they will both pick up the same common mode noise signal as they pass through the environment.

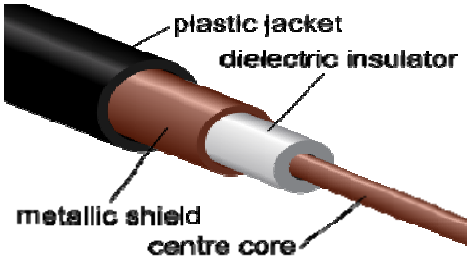


Figure 4-10 Coaxial cable [31]

Figure 4-10 shows a cutaway view of a coaxial cable. The coaxial cable is chosen as the cable type to be implemented in the sensor driver system. It will be implemented as discussed above in order to eliminate possible noise pickup. Each signal will therefore have two cables to be run very close to each other.

4.4.3 Sensor driver transmission line specifications

The specifications of the sensor driver transmission lines are as follows:

- Operating frequency: 2.083 MHz
- High resonant frequency (> 2 MHz)
- Low-loss cable
- Length: 3 m
- Low phase shift over length of cable (< 20°)

The choice of cables was narrowed down to two, namely the 1855A and 1865A single core coaxial cables from Belden. The specifications of these two cables are given in Table 4-1.

Table 4-1 Cable specifications [32],[33]

Name	AWG	*L* (µH/m)	*C* (pF/m)	*R* (Ω/km)	Shielding	Resonant Frequency (MHz)	Phase shift (degrees)
1855A	23	0.351067	53.4803	65.9481	Beldfoil	17.277	-7.0613
1865A	25	0.305133	54.1365	89.8994	Duofoil	18.418	-6.186

Each of these cables will now be discussed and compared to each other in order to select the best cable for the application.

4.4.4 Cable 1855A: Sub-miniature Coaxial Cable

The circuit schematic of the electrical model used to simulate the transmission line using cable 1855A is shown in Figure 4-11. The series resistors each represent half of the nominal conductor DC resistance as given in the cable's datasheet [32]. At the system's operating frequency of 2 MHz, the conductance of the dielectric can be neglected for coaxial cables, as $G \ll \omega \mathrm{C}$ in the following equation for determining the characteristic impedance of a transmission line [34]:

$$Z_0 = \sqrt{\frac{R+\mathrm{j}\omega \mathrm{L}}{G+\mathrm{j}\omega \mathrm{C}}} \tag{4.8}$$

The series inductors each represent half of the nominal inductance of the cable, and the parallel capacitors represent the nominal capacitance of the conductor to the shield. The values for all these components are given in the cable's datasheet [32] as a value per unit length. These

values are then converted to represent a cable length of 3 m. The transformer represents the PCB sensor, and the voltage follower op-amp represents the load of the signal conditioning circuit.

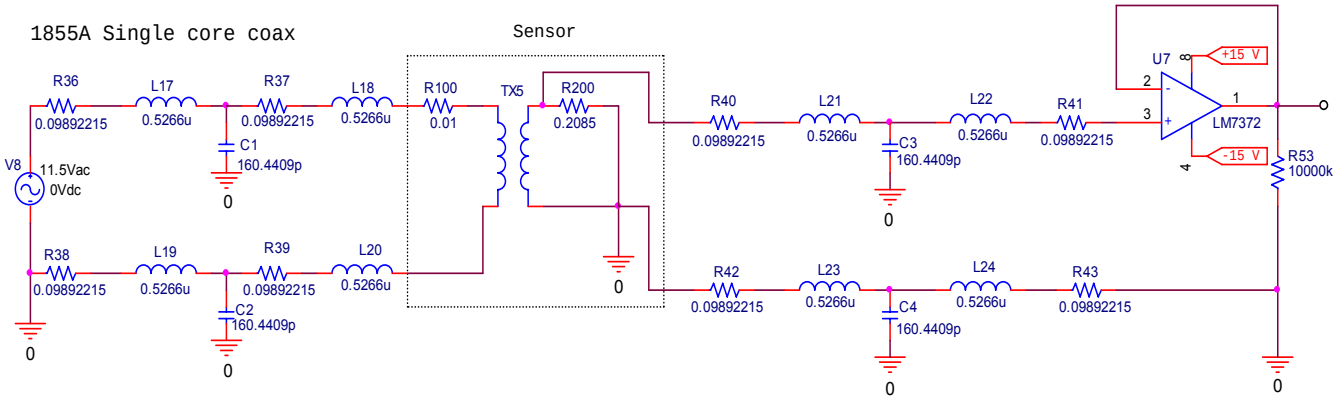


Figure 4-11 Circuit schematic of cable 1855A

The gain and phase plots for cable 1855A from Belden are shown in Figure 4-12 and 4-13 respectively. The gain plot in Figure 4-12 shows the resonant frequency of the cable at a length of 3 metres, as is used with the conventional eddy current sensors.

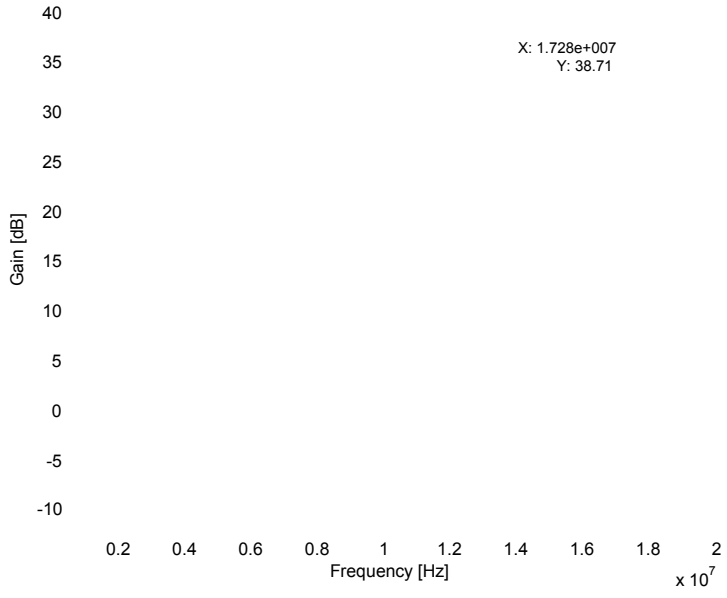


Figure 4-12 Gain plot of cable 1855A showing the resonant frequency

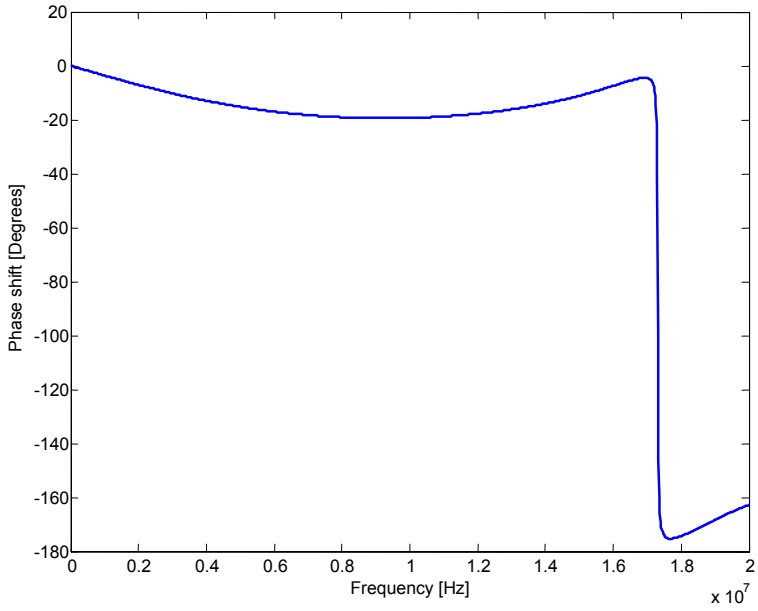


Figure 4-13 Phase plot of cable 1855A

The phase shift of cable 1855A is shown in Figure 4-13. At the operating frequency of 2.0833 MHz the phase shift is found to be -7.33°. The transmission lines for cable 1855A were also simulated using simulated input- and output signals from the sensor, and are shown in Figure 4-14.

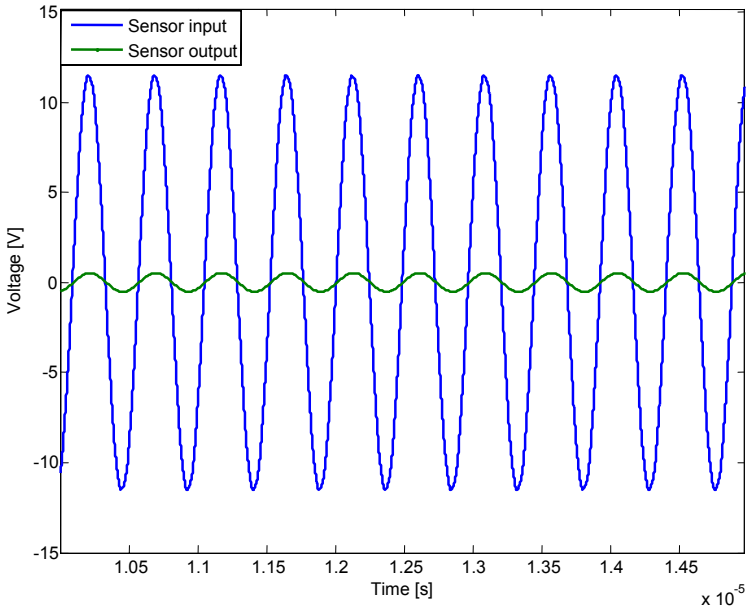


Figure 4-14 Simulated input and output of sensor with cable 1855A

4.4.5 Cable 1865A: Sub-miniature Coaxial Cable

The circuit schematic of the electrical mode used to simulate the transmission line using cable 1865A is shown in Figure 4-15. As discussed in section 4.4.4, each series resistor represents half of the nominal conductor DC resistance as given in the cable's datasheet [33]. At the operating frequency of 2 MHz, the conductance of the dielectric can again be neglected. The series inductors each represent half of the nominal inductance of the cable, and the parallel capacitors represent the nominal capacitance of the conductor to the shield.

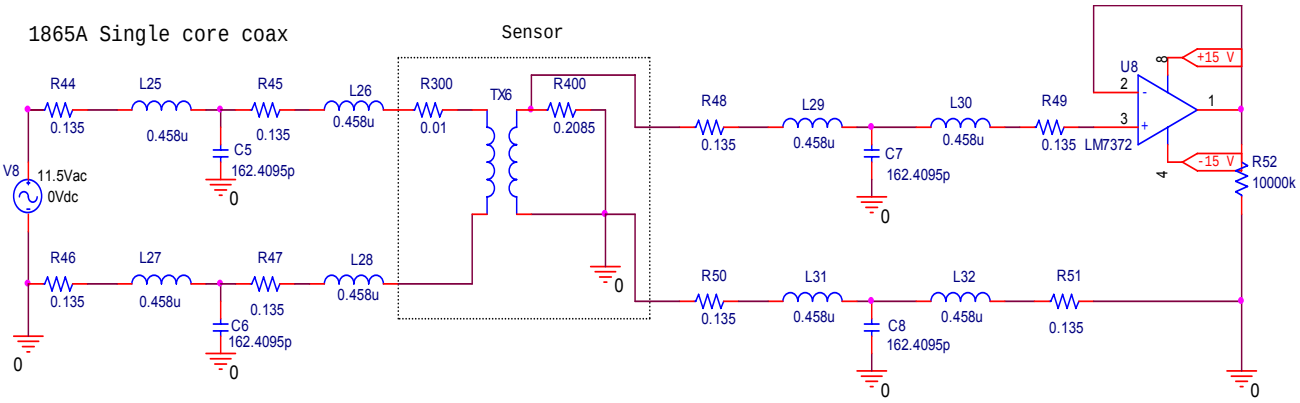


Figure 4-15 Circuit schematic of electrical model used for cable 1865A

The gain and phase plots for cable 1865A are shown in Figure 4-16 and 4-18 respectively. The gain plot shows the resonant frequency of the cable with a length of 3 metres.

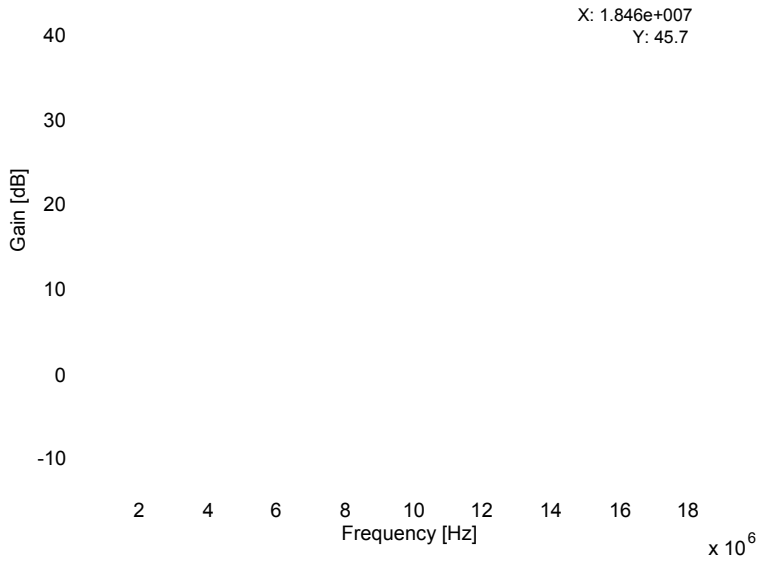


Figure 4-16 Gain plot of cable 1865A from Belden showing the resonant frequency

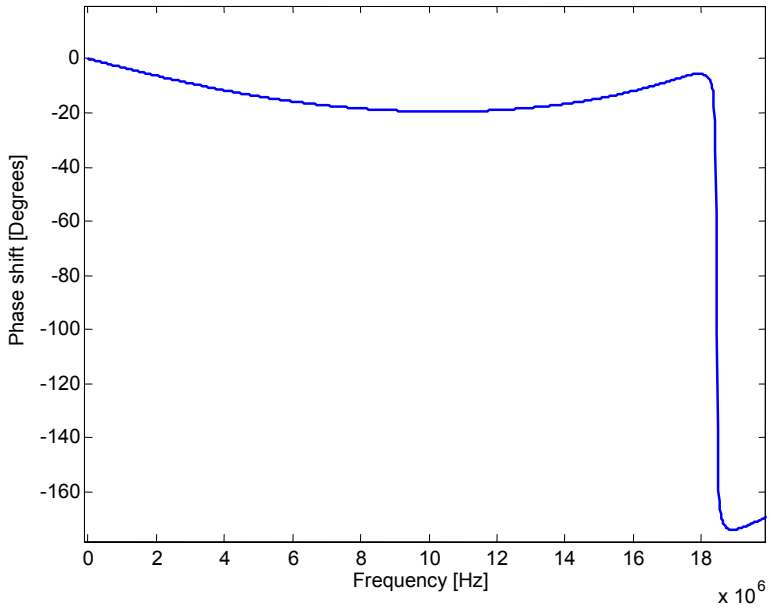


Figure 4-17 Phase plot of cable 1865A from Belden

The phase shift of cable 1865A is shown in Figure 4-17. At the working frequency of 2.0833 MHz the phase shift was measured as -6.43°. The transmission lines of cable 1865A were also simulated using the simulated input- and output signals from the sensor, and are shown in Figure 4-18.

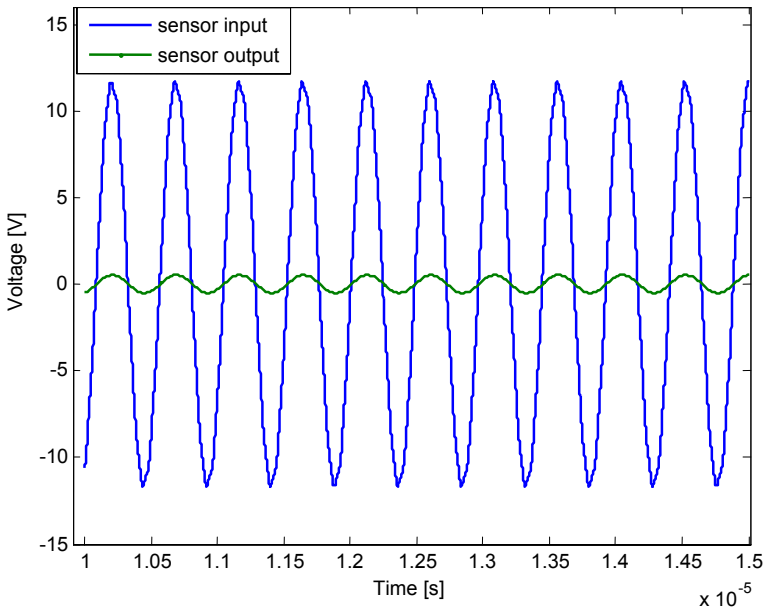


Figure 4-18 Sensor input and output signals using cable 1865A

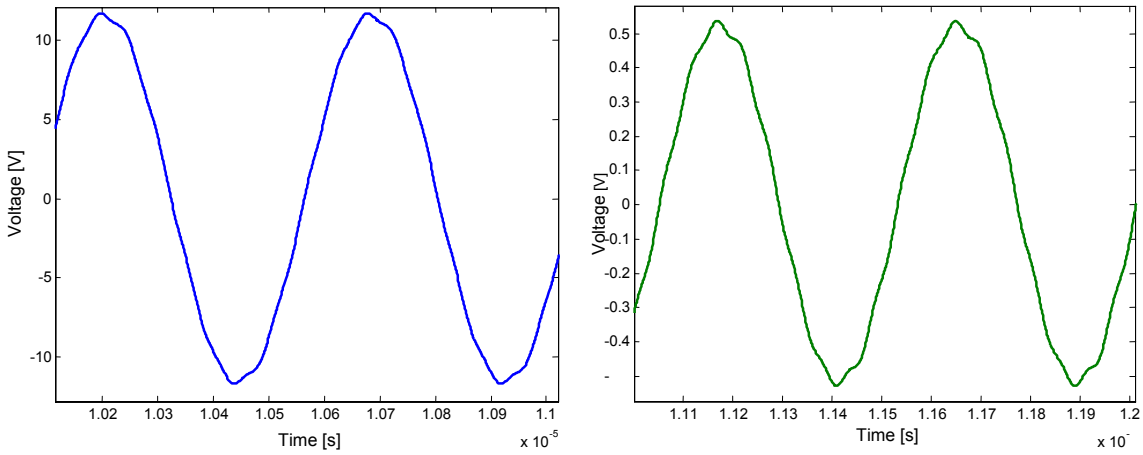


Figure 4-19 Input (left) and output (right) signals of sensor showing slight distortion

As can be seen from Figure 4-18, the 1865A cable causes some distortion in the signal, which is magnified in Figure 4-19. The 1855A cable however does not cause any distortion to the signal. The 1855A cable was therefore chosen for implementation in the sensor driver project.

If the length of the cable is increased to 10 meters, it can be seen from that the resonant frequency is still well above 2 MHz. Figure 4-21 shows the resonant frequency when the length of the cable is reduced to 1 meter.

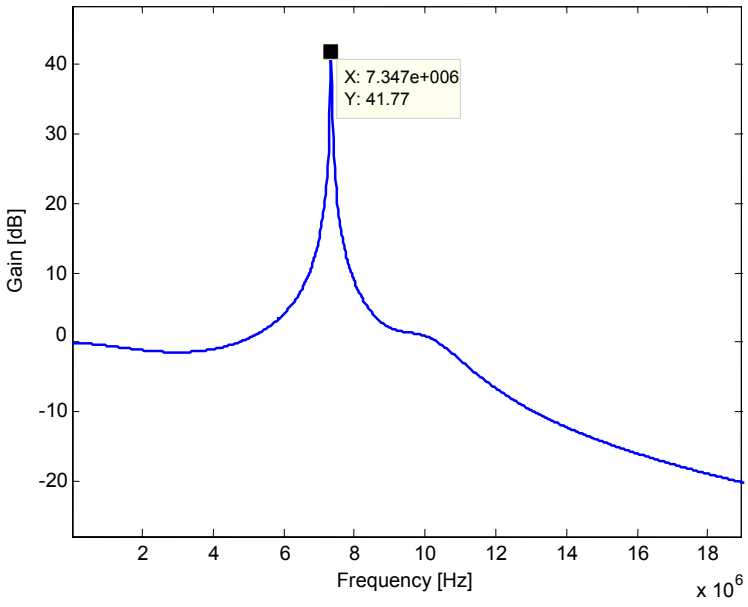


Figure 4-20 Frequency response of cable 1855A (length: 10 m)

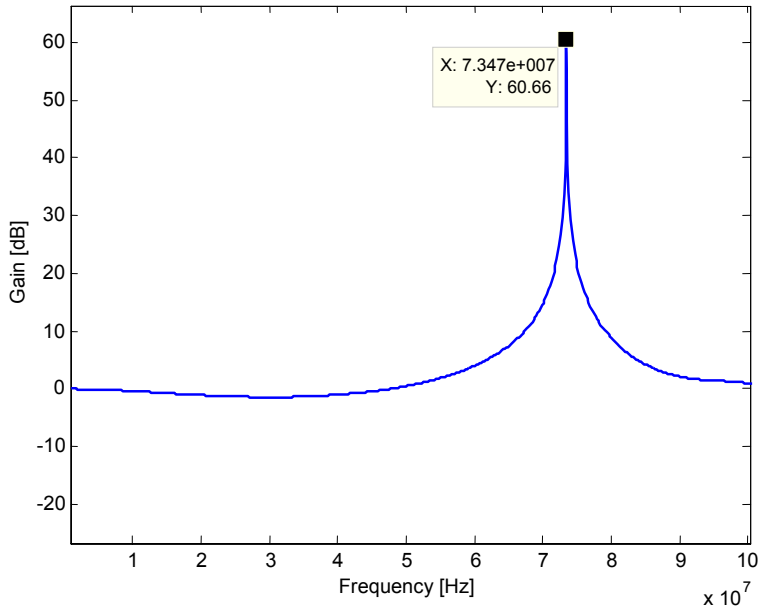


Figure 4-21 Frequency response of cable 1855A (length: 1 m)

4.5 Signal conditioning circuit

The signal conditioning circuit receives the four output signals from the sensor and conditions them for digital processing. The operational diagram of the signal conditioning circuit is shown in Figure 4-22. This circuit consists of five parts, namely:

1. a signal amplifier
2. band-pass filter
3. amplitude demodulator
4. low-pass filter, and
5. gain/scaling amplifier.

Each of these five parts will now be discussed.

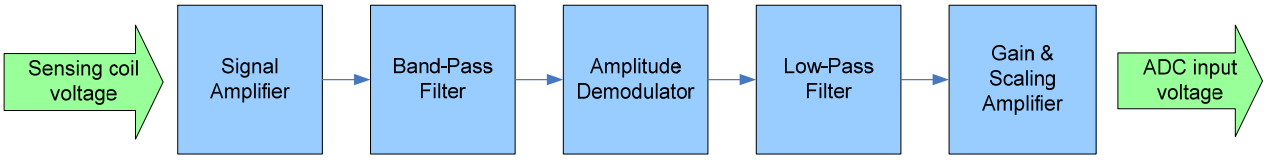


Figure 4-22 Signal conditioning circuit operational diagram

4.5.1 Signal amplifier

The function of the signal amplifier is to amplify the sensor sensing coil output voltage for further signal processing. Noise levels must be kept to a minimum, and distortion of the signal must be avoided. A low noise, high accuracy amplifier is therefore needed.

4.5.1.1 Requirement specifications of signal amplifier

The requirement specifications for the signal amplifier are as follows:

- ±5 V supply voltage
- ≥ ±0.6 V input voltage
- ≥ ±3.5 V output voltage swing
- Bandwidth ≥ 20 MHz
- Slew rate ≥ 40 V/µs
- Low input offset voltage (V_{OS} < 5 mV)
- Low input offset voltage drift (< 5 µV/°C)
- Low input voltage noise (< 3nV/$\sqrt{\text{Hz}}$)

4.5.1.2 Circuit design of signal amplifier

The design of the signal amplifier circuit consists of a single low-noise, low-distortion, high speed operational amplifier. The input to the signal amplifier is between ±0.42 V and ±0.52 V, and the output will be the maximum output swing of the chosen operational amplifier. The selection of the operational amplifier will therefore be essential to the performance of the signal amplifier circuit.

4.5.1.3 Component selection for signal amplifier

The component selection for this design entailed thorough research on available op amps adhering to the requirement specifications criteria. The list was narrowed down to the selection shown in Table 4-2, and their performance parameters compared in order to select the most suitable op amp for this design. The selected op amp is the AD8099 ultra-low distortion, high speed, low noise op amp. The AD8099 was chosen since it had the lowest input voltage noise, second lowest input offset voltage, and second lowest input offset voltage drift from all the op amps in the selection. The gain will be set using a trimming potentiometer, which will be replaced with a fixed resistor in the final circuit.

Table 4-2 Op amp selection

		Supply (V)	Output Voltage Swing (V)	GBWP (MHz)	Slew Rate (V/μs)	Min Stable Gain	Input Voltage Noise (nV/√Hz)	Input Offset Voltage (mV) @25°C	Input Offset Voltage Drift (μV/°C)
1	AD829	±5 / ±15	±3 / ±12	600 / 750	150 / 230	1	1.7	1	0.3
2	AD8099	±5	±3.8	3800	1350	2	0.95	0.5	2.3
3	ADA4899-1	±5	±3.25	600	310	1	1	0.23	5
4	LMH6622	±6	±4.6	160	85	2	1.6	1.2	-2.5
5	LMH6628	±5	±3.5	200	550	1	2	±2	5
6	LMH6702	±5	±3.5	1700	3100	1	1.83	±4.5	-13
7	MAX4105	±5	±3.7	410	1400	5	2.1	6	2.5
8	MAX4433	±5	-2.5 - +4.5	180	145	1	2.8	±5	7
9	OPA843	±5	±3.5	800	1000	5	2	±0.3	±4
10	OPA2674	±6	±4.8	220	2000	1	2	±1	±4
11	OPA4820	±5	±3.5	250	240	1	2.5	±0.25	8

As can be seen in Table 4-2, the AD8099 has a slew rate of 1350 V/μs and a gain bandwidth product of 3.8 GHz. Its input voltage noise is a mere 0.95 nV/$\sqrt{\text{Hz}}$ and has an input offset voltage of 0.5 mV and an input offset voltage drift of 2.3 μV/°C. It requires a ±5 V supply and has an output voltage swing of ±3.8 V [22].

4.5.1.4 Circuit schematic and simulations for signal amplifier

The circuit schematic for this design is shown in Figure 4-23. A signal generator is used to simulate the output from the sensor. A buffer amplifier is also included to prevent the signal conditioning circuit from loading the sensor coils unacceptably and interfering with the performance of the sensor. The AD8099 is implemented as a non-inverting amplifier.

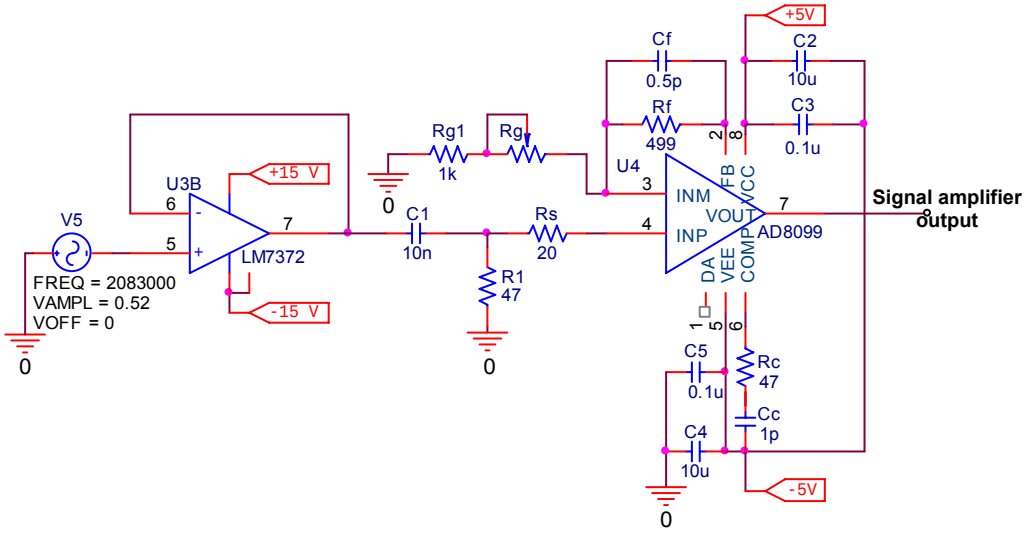


Figure 4-23 Signal amplifier circuit schematic

R_g is a precision trimming potentiometer (trimpot) in order to adjust the closed loop gain of the circuit. R_{g1} is a fixed resistor to limit the gain to 11 V/V in order to protect the circuits following the signal amplifier. The input to the signal amplifier is around ±0.52 V [7], and the output voltage swing of the op amp is around ±3.8 V. The required gain is calculated as follows:

$$A = \frac{V_{OUT}}{V_{IN}} \tag{4.4}$$

$$= \frac{3.8\ V}{0.52\ V}$$

$$= 7.3\ \text{V/V}$$

The value of R_F is recommended by the product's datasheet as 499 Ω, so the value of R_G is calculated as follows:

$$A = 1 + \frac{R_F}{R_G} \tag{4.5}$$

$$\therefore R_G = \frac{R_F}{A-1}$$

$$= \frac{499}{6.3}$$

$$= 79.2\ \Omega$$

C_1 is used to perform ac-coupling of the input signal from the sensor by acting as a high-pass filter. By implementing ac-coupling, all dc current flowing through R_f and R_g is removed. Since the input offset voltage and current parameters for the op amp are dc parameters, they can therefore also be eliminated. The values for the other components present in the circuit were obtained from the AD8099 datasheet. The circuit was simulated using Orcad Capture, and the result is shown in Figure 4-24.

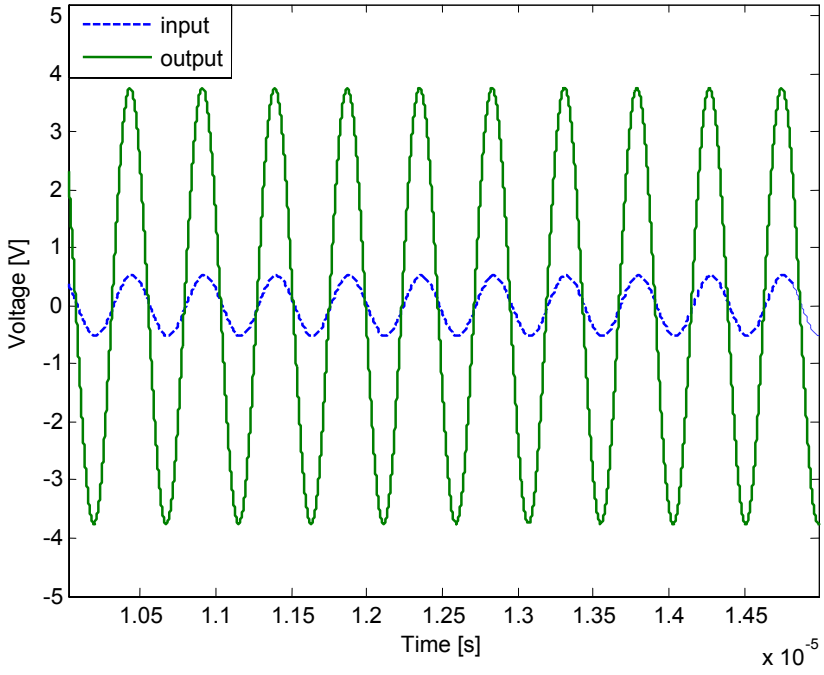


Figure 4-24 Signal amplifier input and output signals

4.5.1.5 Performance parameter specifications of signal amplifier

- **Linearity of signal amplifier**

Since the circuit performs ac amplification, ac coupling removes the effect of the input voltage offset of the op amp. The linearity of the design is therefore mostly determined by the differential gain error of the op amp.

- **AD8099 Op amp [22]:**
  - Differential gain: 0.025%

∴ Total linearity of signal amplifier: 0.025%

- **Temperature stability of signal amplifier**

Due to the fact that the input offset voltage is removed by ac coupling, the temperature drift associated with that dc parameter can also be ignored. The temperature stability of the design can therefore only be approximated using the temperature coefficients of the gain, feedback and input resistors. The temperature coefficient, number of components influencing the temperature stability of the design, and the operating temperature range of the components are as follows:

- **Resistors:**
  - Temperature coefficient: 10 ppm/°C.
  - Number of resistors: 3
  - Temperature range: -55°C to +125°C

∴ Total temperature stability of signal amplifier: 30 ppm/°C (max)

4.5.2 Band-pass filter

The function of the band-pass filter is to remove undesired high and low frequency noise present in the sensor output signal. Its effect on the modulated envelope component can be modelled as a first order low-pass filter as given by

$$LPF = G\frac{1}{s+\Delta\omega} \tag{4.6}$$

where *G* is a gain constant and *Δω* is half the pass-band of the BPF [37].

4.5.2.1 Requirement specifications for band-pass filter

The requirement specifications for the band-pass filter are as follows:

- ±5 V supply voltage
- ±3.8 V input voltage
- ≥ ±3.5 V output voltage swing
- Bandwidth ≥ 20 MHz
- Slew rate ≥ 40 V/μs
- Low input offset voltage (V_{OS} < 5 mV)
- Low input offset voltage drift (< 5 μV/°C)
- Low wideband output noise (< 15 nV/$\sqrt{\text{Hz}}$)

4.5.2.2 Circuit design for band-pass filter

The bandwidth of the band-pass filter is chosen as the maximum frequency at which the low-pass filter's phase shift is still acceptable at the system bandwidth (10 kHz), and will not result in the system becoming unstable and the attenuation unsatisfactory. For this application the maximum phase shift at 10 kHz is 10°. Taking this into consideration, a fourth order band-pass filter with a bandwidth of 200 kHz is used. The phase shift of the corresponding second order low-pass filter at 10 kHz is calculated as 7.91°, which is still below the maximum phase shift for the sensor driver. A low noise, high frequency, fourth order band-pass filter is therefore required for this design.

4.5.2.3 Component selection for band-pass filter

The fourth order band-pass filter is implemented by means of a LT1568 filter building block IC. The LT1568 is a very low noise, high frequency active RC filter building block that requires only a few external components to implement either a 2nd or 4th order low-pass or band-pass filter with centre frequency up to 10 MHz. The internal components comprising the filter building block IC are also configured to function optimally together, whereas a filter comprising external components may not be, and can cause the circuit performance parameters to be greater than required. This will in turn cause the sensor driver to not meet its set requirements and not perform as optimally and accurately as needed. The LT1568 has a slew rate of 53 V/µs and a bandwidth of 55 MHz. It requires a ±5 V supply voltage, and can deliver an output voltage swing of ±4.7 V [35].

4.5.2.4 Circuit schematic and simulations for band-pass filter

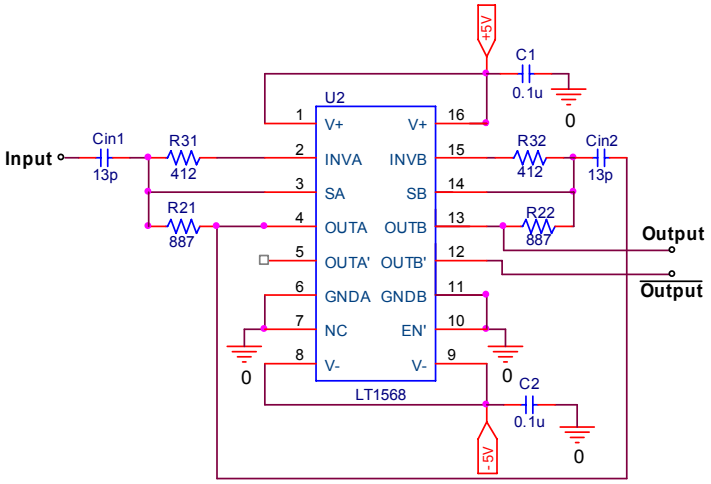


Figure 4-25 Band-pass filter circuit schematic [35]

The circuit schematic for the band-pass filter is shown in Figure 4-25. In order to refine the gain of the filter, R_{31} is chosen as a 500 Ω precision trimming potentiometer. The frequency response of the band-pass filter circuit is shown in Figure 4-26. The centre frequency of the band-pass filter is at 2 MHz with a 200 kHz 3 dB bandwidth.

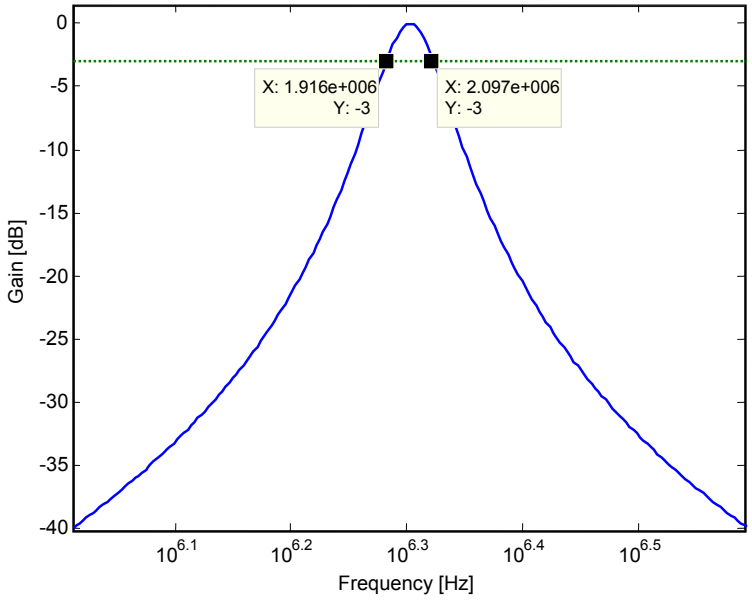


Figure 4-26 Frequency response of band-pass filter

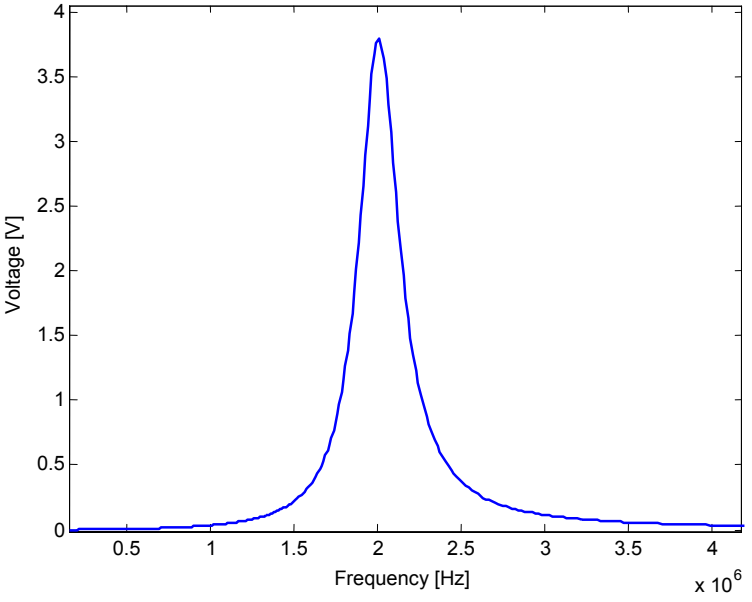


Figure 4-27 Amplitude response of band-pass filter

The amplitude response of the band-pass circuit was obtained by performing an ac-sweep with amplitude 3.8 V on the circuit, and is shown in Figure 4-27. R_{31} was adjusted to 404 Ω in order to obtain a voltage gain of 1 V/V. The output of the filter is shown in Figure 4-28, and was obtained by providing a 2 MHz sine wave with 3.8 V amplitude as input to the circuit. The circuit has a settling time after start-up of roughly 7 µs according to the simulation.

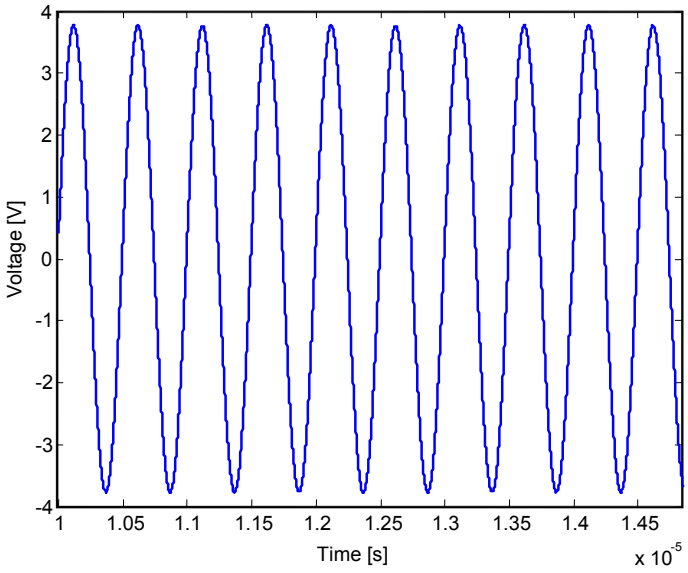


Figure 4-28 Output voltage of band-pass filter circuit

4.5.2.5 Linearity of band-pass filter

Once again, since ac amplification is performed by the circuit, the included ac coupling capacitors remove the effect of the input voltage offset of all the internal op amps. The linearity of the design is therefore mostly determined by output variations of the filter building block. These effects are however not specified in the product's datasheet, and are assumed to be no more than 1%.

4.5.2.6 Temperature stability of band-pass filter

The temperature stability of the band-pass filter design is approximated using the temperature coefficients of the resistors and capacitors that make up the external components to the filter. The temperature coefficient, number of components influencing the temperature stability of the design, and the operating temperature range of the components are specified.

- **Resistors:**
  - Temperature coefficient: +10 ppm/°C
  - Number of resistors: 4
  - Temperature range: -55°C to +125°C
- **Capacitors:**
  - Temperature coefficient: 0 ± 30 ppm/°C
  - Number of capacitors: 2
  - Operating temperature range: -55°C to +125°C

∴ Total temperature stability for band-pass filter: 100 ppm/°C (max)

4.5.3 Amplitude demodulator

In order to effectively convert the sensor output into accurate position values, the sine wave output signal must be converted to a dc value. This step is required since the position values are obtained from the peak amplitude variation of the signal. Amplitude demodulation must therefore be performed to rectify the amplified sine wave output signal in order to obtain a dc signal. This can be done using one of three methods:

- Full wave rectifier circuit followed by a low-pass filter
- Amplitude demodulator followed by a low-pass filter
- RMS-to-DC converter

After considering each method with regards to availability of components able of functioning at the required frequency (2 MHz), the RMS-to-DC converter was chosen.

4.5.3.1 Requirement specifications for amplitude demodulator

The requirement specifications for the RMS-to-DC converter are as follows:

- ±5 V / ±15 V supply voltage
- ≥ ±3.8 V input voltage
- ≥ 2.7 V_{RMS} input voltage
- ≥ +3.5 V output voltage swing
- Bandwidth ≥ 2 MHz

4.5.3.2 Circuit design of amplitude demodulator

The design consists of a single RMS-to-DC converter together with a few external components. A high precision device is required in this design to keep circuit-generated noise levels to a minimum and ensure a highly accurate design. A high bandwidth is also required in order to be able to convert the 2 MHz signal, as well as an output voltage swing greater than ±12 V. These requirements resulted in a limited amount of viable components.

4.5.3.3 Component selection for amplitude demodulator

The chosen RMS-to-DC converter is the AD637 high precision, wideband RMS-to-DC converter. Since RMS-to-DC converters are mostly used in small-signal, low frequency applications, the available selection of components were scarce. The AD637 converter was selected due to the fact that it is the only available component adhering to all the requirement specifications, specifically the bandwidth requirement of 2 MHz and the input and output voltage level requirements. It also requires only one external component to function, but optional trimming resistors and filter components may be added to improve the performance of the device. The AD637 calculates the true root mean square value of the input waveform, which can be either ac or dc, and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal because it relates directly to the power of the signal.

The AD637 has a ±3 dB bandwidth of 8 MHz, output voltage swing of 0 to 13.5 V, and requires a supply voltage of ±15 V [36]:

4.5.3.4 Circuit schematic of amplitude demodulator

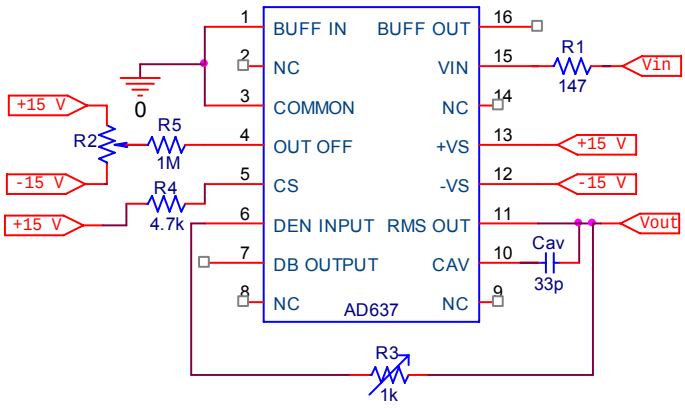


Figure 4-29 RMS-to-DC converter circuit schematic

The circuit schematic of the RMS-to-DC converter circuit is shown in Figure 4-29. C_{AV} determines the averaging time constant according to (4.7) as given in the datasheet [36]:

—— (4.7)

The AD637 uses an inverting low-pass filter stage to provide a buffered voltage output whose averaging time constant is set by its internal on-chip 25 kΩ feedback resistor and an external averaging capacitor, C_{av}. The RC_{av} time constant is chosen to be longer than the period of the lowest frequency being measured, but short enough to allow reasonable settling time and phase shift. Figure 4-30 shows a plot of the phase shift at the sensor bandwidth (10 kHz) for different values of the averaging capacitor C_{av}. In order to minimize the dc error of the converter, the input frequency must be greater than the inverse of the time constant. This means that the time constant determined by C_{av} must be larger than the period of the input signal, as expressed in (4.8).

—— (4.8)

This restricts the value of C_{av} to greater than 20 pF, meaning that the minimum phase shift obtainable at 10 kHz is around 2 °. The value of C_{av} is therefore chosen as 33 pF, which results in a phase shift of 2.97 °.

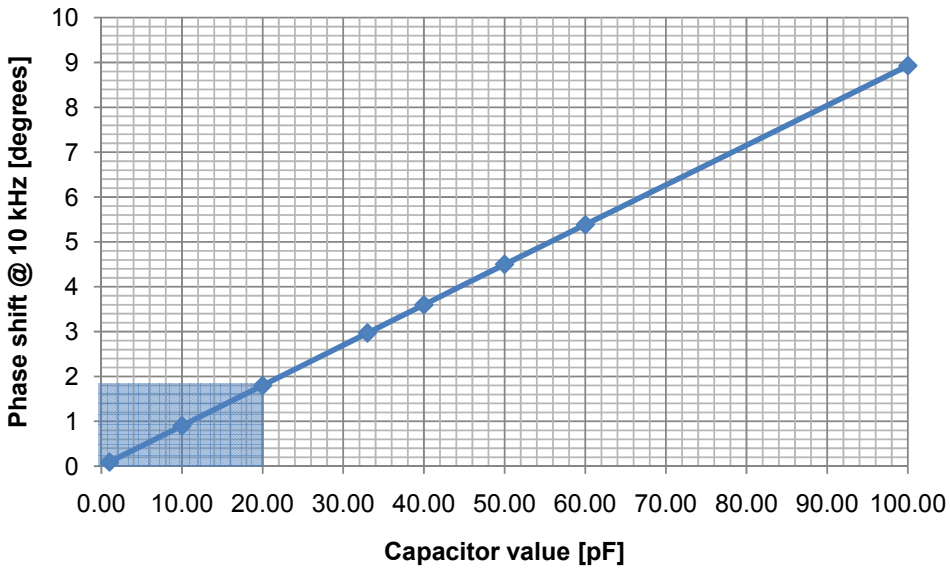


Figure 4-30 Phase shift of sensor bandwidth for different averaging capacitor values

Resistor R_2 is a 50 kΩ variable resistor that provides the offset trim for the circuit. The offset trim is done by grounding the input signal and adjusting R_2 so that the output is 0 V. Resistor R_3 is

used to trim the scale factor of the converter in order to obtain the correct rms output voltage. These two resistors are included in the circuit to trim out output offset and scale factor errors, thereby increasing the accuracy of the converter. Remaining errors are due to nonlinearity factors. The output of the circuit is the root-mean-square of its input voltage. To calculate the approximate linearity and temperature stability of the circuit, it is assumed that the input voltage is ±3.8 V, and the output rms voltage is a maximum of 2.687 V.

4.5.3.5 Linearity of amplitude demodulator

The linearity of the RMS-to-DC conversion circuit is mainly determined by the conversion accuracy of the converter, consisting of conversion irregularities as well as dc output offsets.

- **RMS-to-DC converter (AD637) [36]:**
  - Nonlinearity: 0.02 % FSR
  - Total error (with external trim): ±0.25 mV ± 0.05 % of reading

    = ±0.009 % ± 0.05 %

    = ±0.059 %

∴ Total linearity of amplitude demodulator: 0.079%

4.5.3.6 Temperature stability of amplitude demodulator

The temperature stability of the RMS-to-DC conversion circuit is given by the output offset voltage drift of the internal op-amps of the converter, and the temperature coefficient of the averaging capacitor.

- **RMS-to-DC converter (AD637) [36]:**
  - Output offset voltage drift: ±0.056 mV/°C = ±20.841 ppm/°C
  - Operating temperature range: -40°C to +85°C
- **Capacitor:**
  - Temperature coefficient: 0 ± 30 ppm/°C
  - Operating temperature range: -55°C to +125°C

∴ Total temperature stability of amplitude demodulator: ±51 ppm/°C

4.5.4 Low-pass filter

Since the output of the RMS-to-DC converter is already a dc signal, and due to the fact that the converter already implements a low-pass filter stage, an additional low-pass filter is not necessary and would only increase the phase shift of the sensor.

4.5.5 Gain and scaling amplifier

The gain and scaling amplifier is required to scale the output variation of the sensor so that the largest part possible of the input range of the ADCs is utilized. This entails subtracting a reference voltage from the amplifier input, and multiplying the signal with a gain to obtain an output of ±3.8 V, which is the output voltage range of the op-amp. The input voltage range of the ADCs is ±5 V, so the input to the ADC will be up to 76 % of its input range. The reference voltage is calculated by taking the mean of the minimum and maximum input values, which is 2.168 V and 2.684 V respectively. This allows the ADC input to correspond to the entire sensor measuring range. The reference voltage is calculated as 2.4275 V and is subtracted from the op-amp's input signal to generate a dc signal around zero.

The gain of the op-amp is calculated as follows:

$$A = \frac{|V_{OUT}|}{|V_{IN}|} \tag{4.9}$$

$$= \frac{3.8\ \mathrm{V}}{0.2595\ \mathrm{V}}$$

$$= 14.64\ \mathrm{V/V}$$

4.5.5.1 Requirement specifications of gain and scaling amplifier

The requirement specifications for the gain and scaling amplifier are as follows:

- ±5 V supply voltage
- ≥ 3 V input voltage
- ≥ ±3 V output voltage swing
- Low input offset voltage (V_{OS} < 5 mV)
- Low input offset voltage drift (< 5 µV/°C)
- Low input voltage noise (< 3 nV/$\sqrt{\mathrm{Hz}}$)

4.5.5.2 Circuit design of gain and scaling amplifier

The circuit consists of a subtracting and non-inverting operational amplifier. The circuit requires a low noise, high speed op-amp to perform the gain and scaling functions. The reference voltage subtracted from the signal is generated by either a precision voltage reference, or a precision potentiometer. In the first test design, the potentiometer will be used, but will be replaced with a precision voltage reference in the final design.

4.5.5.3 Component selection for gain and scaling amplifier

The component selection for this design was based on previous component selection decisions. The same op-amp used in the signal amplifier circuit was chosen, namely the AD8099 ultra-low distortion, high speed, low noise op amp. To adjust the gain, a trimming potentiometer is used. The relevant specifications of the AD8099 were given in 4.3.2 [22].

4.5.5.4 Circuit schematic and simulations for gain and scaling amplifier

The circuit schematic for this design is shown in Figure 4-31.

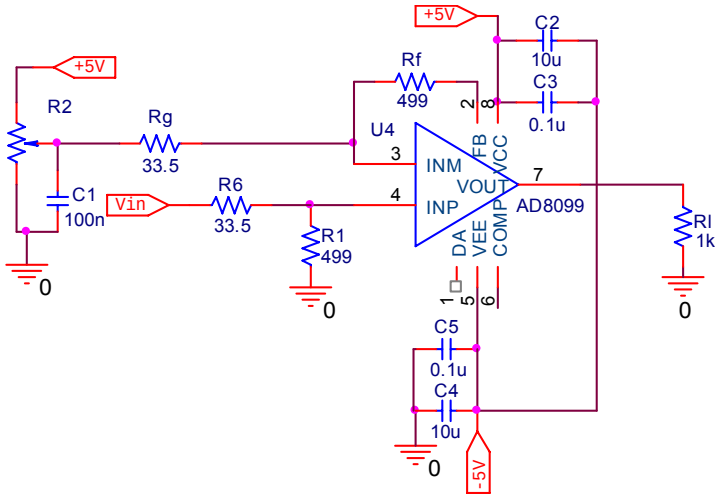


Figure 4-31 Gain and scaling amplifier circuit schematic

R_g and R_6 are precision trimming potentiometers (trimpots) in order to adjust the closed loop gain of the circuit. The voltage reference is provided by the trimming potentiometer R_2.

The gain of 14.64 V/V is achieved as follows:

$$A = 1 + \frac{R_F}{R_G} \tag{4.10}$$

$$R_G = \frac{R_F}{A-1}$$

$$= \frac{499}{13.64}$$

$$= 36.58\ \Omega$$

The circuit was simulated using Orcad Capture, and the output voltage of the amplifier over the input voltage range is shown in Figure 4-32. It can be seen that the entire range of the input voltage correlates to the full output voltage swing of the op-amp.

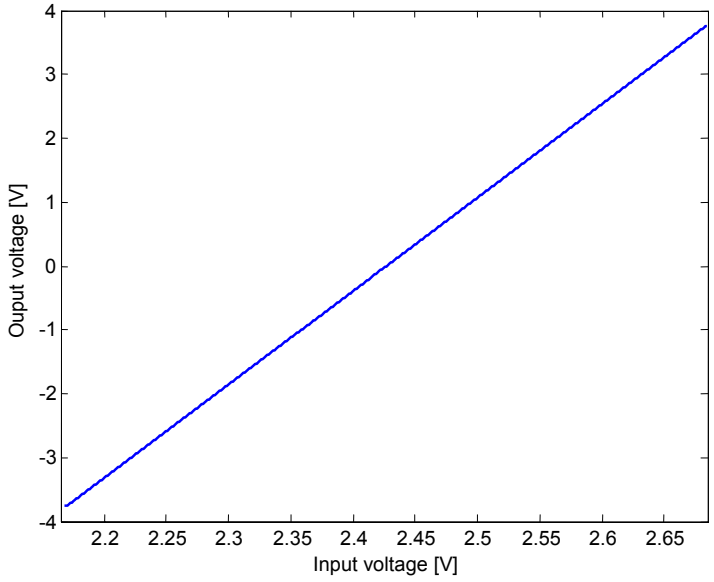


Figure 4-32 Input and output voltage of amplifier circuit

4.5.5.5 Linearity of gain and scaling amplifier

The linearity of the gain and scaling amplifier circuit is determined by its input voltage offset, differential gain error of the op amp, and the setting stability of the trimming potentiometers.

- **AD8099 Op amp [22]:**
  - Differential gain: 0.025%
  - Input offset voltage (V_{OS}): 0.5 mV

The output offset error (E_O) is then calculated as follows:

$$E_O = \left(1 + \frac{R_F}{R_G}\right) V_{OS} \tag{4.11}$$

$$= \left(1 + \frac{499}{36.58}\right) (0.5\, e^{-3})$$

$$= 7.32 \text{ mV}$$

$$= 0.096\ \%$$

∴ Total linearity of gain and scaling amplifier: 0.121%

4.5.5.6 Temperature stability of gain and scaling amplifier

The temperature stability of the design can be approximated using the temperature coefficients of the trimpots, gain-, feedback- and input resistors, as well as the input offset voltage drift of the op amp. The temperature coefficient, number of components influencing the temperature stability of the design, and the operating temperature range of the components are as follows:

- **AD8099 Op amp [22]:**
  - Input offset voltage drift: 2.3 µV/°C

  The output offset error drift is therefore

$$E_O(T) = \left(1 + \frac{R_F}{R_G}\right) V_{OS}(T) \tag{4.12}$$

$$= (14.64)(2.3e^{-6})$$

$$= 33.67\mu V/℃ \ = \ 4.43 \text{ ppm/℃}$$

  - Temperature range: -40°C to +125°C

- **Trimming potentiometer:**
  - Temperature coefficient: ±100 ppm/°C
  - Number of trimpots: 2
  - Temperature range: -55°C to +150°C

- **Resistors:**
  - Temperature coefficient: 10 ppm/°C.
  - Number of resistors: 2
  - Temperature range: -55°C to +125°C

∴ Total temperature stability of gain and scaling amplifier: 225 ppm/°C (max)

The relatively poor temperature stability of the trimming potentiometers causes the total temperature stability of the gain and scaling amplifier to be too high. The trimming potentiometer configuration as showed in Figure 4-31 will therefore only be used in the first test design and not in the final design. In the final design, the potentiometers will be replaced be a high precision resistor. The potentiometers used in the gain and scaling amplifier are 100 Ω potentiometers. The temperature stability for the parallel configuration of potentiometer R_G and its fixed resistor R_{G2} is then:

$$R_{P1} = \frac{R_G R_{G2}}{R_G + R_{G2}} \tag{4.13}$$

$$= \frac{100 \times 51}{100 + 51}$$

$$= 33.7748\ \Omega$$

$$R_{P2} = \frac{(R_G + 100\ \text{ppm})(R_{G2} + 10\ \text{ppm})}{(R_G + 100\ \text{ppm}) + (R_{G2} + 10\ \text{ppm})}$$

$$= 33.7762\ \Omega$$

$$\frac{R_{P2} - R_{P1}}{R_{P1}} = 4.03955e^{-3}\ \% = \ 40.395\ \text{ppm}$$

For the parallel configuration of the potentiometer R_2 and its fixed resistor R_{2_F}, the temperature stability is calculated as follows:

$$R_{P1} = \frac{R_2 R_{2\_F}}{R_2 + R_{2\_F}} \tag{4.13}$$

$$= \frac{1000 \times 1750}{1000 + 1750}$$

$$= 636.3636\ \Omega$$

$$R_{P2} = \frac{(R_2 + 100\ \text{ppm})(R_{2_F} + 10\ \text{ppm})}{(R_2 + 100\ \text{ppm}) + (R_{2\_F} + 10\ \text{ppm})}$$

$$= 636.4064\ \Omega$$

$$\frac{R_{P2} - R_{P1}}{R_{P1}} = 6.727e^{-3}\ \% = \ 67.27\ \text{ppm}$$

Therefore the total temperature stability of the gain and scaling amplifier is:

∴ Total temperature stability of gain and scaling amplifier: 132 ppm/°C (max)

4.5.6 Summary of performance parameters for signal conditioning circuit

In this section, the total estimated percentage of the performance parameters for the signal conditioning circuit are calculated and compared to the set performance parameter requirements determined in chapter 3.

- **Required performance parameters:**
  - Linearity: $\pm 1.5\ \%$
  - Temperature stability: ± 200 ppm/°C
- **Estimated achievable performance parameters:**
  - Linearity: 0.025 % + 1% + 0.079 % + 0.121 % = **0.225 %** << 1.5%
  - Temperature stability: 30 ppm/°C + 100 ppm/°C + 51 ppm/°C + 132 ppm/°C

= 313 ppm/°C > 200 ppm/°C

The estimated temperature stability of the signal conditioning circuit is poorer than the specification estimate. This is expected, since the signal conditioning circuit consists of a great deal of analogue components, which may not be the case with the eddy current sensor controller from Micro-Epsilon and SKF used to obtain the requirement specification estimates. Another aspect for consideration is the fact that the specifications of the Micro-Epsilon sensor is given as a percentage of the sensor system's full scale output, and not as a percentage of the components' output capability. Also, as mentioned in chapter 3, these requirement specification

estimates serve only as baseline figures, and not fixed requirements. The development of the sensor driver design will therefore continue, despite its slight variations from the estimated requirement specifications.

4.6 Analogue-to-digital converters (ADC)

The analogue-to-digital converters convert the analogue signals from the signal conditioning circuit into digital values which is then sent to the digital processing circuit for further processing.

4.6.1 Requirement specifications for ADCs

The requirement specifications for the ADCs are as follows:

- ≥ 12-bit resolution
- > 0.5 MSPS throughput rate
- SPI compatibility
- Linearity ≤ ±1.5 %
- Temperature stability ≤ ±50 ppm/°C

4.6.2 Circuit design of ADCs

Since the complete sensor driver will need to process multiple signals, it was decided that in order to reduce component count, only ADCs with 2 channels or more which perform simultaneous sampling were to be considered for implementation. The ADC samples the analogue input signal, converts it into digital values, and communicates the values by means of an SPI connection to the digital processing circuit. The SPI connection allows for a very high throughput rate.

4.6.3 Component selection for ADCs

The following component was chosen for implementation in this design:

- **AD7367** Dual 14-bit 2-channel, simultaneous sampling ADC [38]

The AD7367 ADC was chosen because of its high throughput rate of 1 MSPS, 14-bit resolution and its two channels with simultaneous sampling. It also has programmable input ranges of

±10 V, ±5 V, 0 V – 10 V, and ±12 V with a 3 V external reference. Simultaneous conversion with read process is specified to be performed in less than 1 µs, and the AD7367 has a high speed SPI compatible interface. The specifications of the AD7367 therefore adhere to all its requirements.

4.6.4 Circuit schematic for ADCs

The circuit schematic for the AD7367 ADC is shown in Figure 4-33.

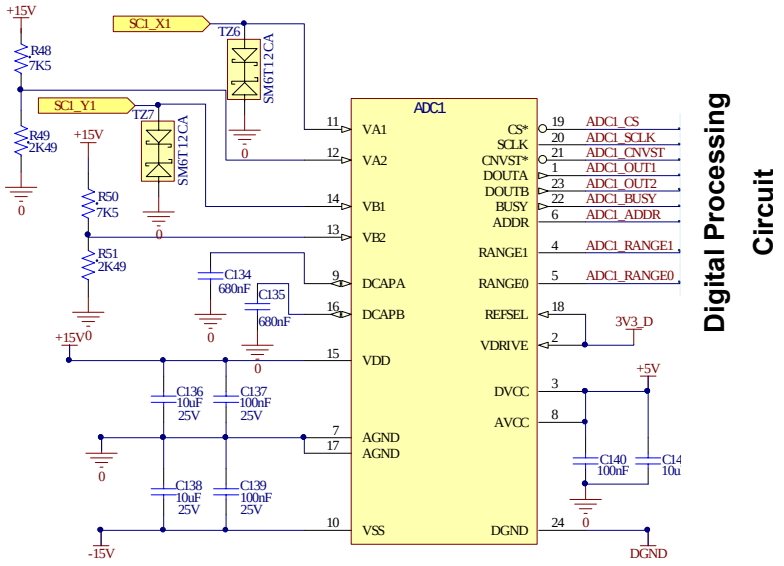


Figure 4-33 Circuit schematic of ADC AD7367

4.6.5 Linearity

The linearity of the ADC circuit is mostly determined by the differential nonlinearity of the ADC.

- **AD7367 ADC [38]:**
  - Differential nonlinearity: ±0.9 LSB

∴ Linearity: $\frac{V_{FRSR}}{2^N} \times \text{DNL} \times 100\ \%$

$$= \frac{10}{2^{14}} \times 0.9 \times 100\ \%$$

$$= 4.5 \times 10^{-12}\ \%$$

∴ **Total linearity of ADCs: 4.5×10^{-12} %**

4.6.6 Temperature stability of ADCs

- **AD7367 [38]:**
  - Reference temperature coefficient: 25 ppm/°C
  - Operating temperature range: -40°C to +85°C

∴ Total temperature stability of ADCs: 25 ppm/°C

4.6.7 Summary of performance parameters for ADCs

In this section, the total estimated percentage of the performance parameters for the analogue-to-digital converters are calculated and compared to the set performance parameter requirements determined in chapter 3.

- **Required performance parameters:**
  - Linearity: $\pm 1.5\%$
  - Temperature stability: ± 50 ppm/°C
- **Estimated achievable performance parameters:**
  - Linearity: **$4.5e^{-12}$ %** << 1.5 %
  - Temperature stability: **25 ppm/°C** < 50 ppm/°C

The estimated linearity and temperature stability of the ADCs are much better than required. The AD7367 is therefore well-suited for implementation in the sensor driver.

4.7 Sensor driver test circuit

The test circuit of the sensor driver consists of a power supply circuit, an excitation circuit and two signal conditioning circuits, all as described in this chapter, along with one PCB sensor. The aim of the test circuit is to verify the concept of the sensor driver with regards to the sensor excitation and signal conditioning. The test circuit was implemented on a six-layer PC board, with separate power and ground planes for optimal performance. Figure 4-34 illustrates the stack-up of the board. Figure 4-35 shows a diagram of the sensor driver test circuit. The measurement results of the test circuit will be discussed in chapter 7.

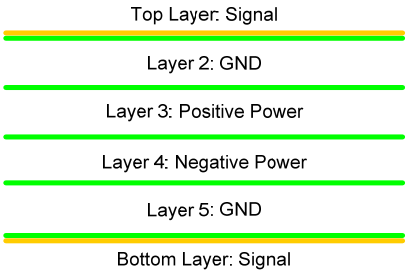


Figure 4-34 Stack-up of sensor driver test circuit board

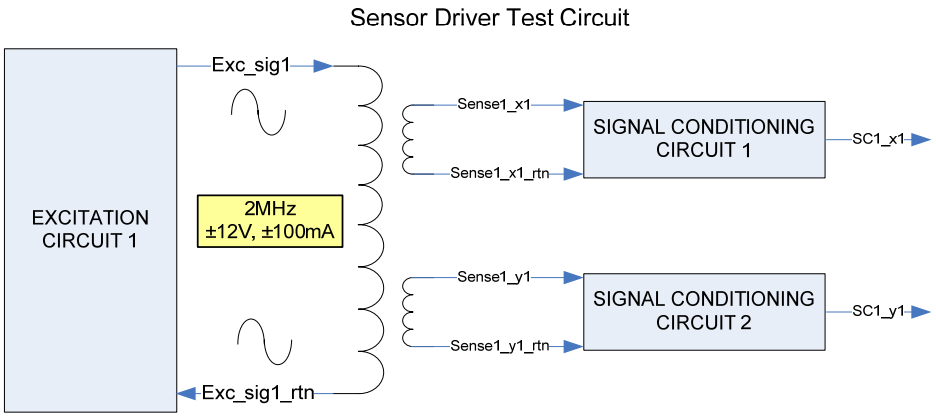


Figure 4-35 Diagram of the sensor driver test circuit

The circuit schematic of the sensor driver test circuit is provided in Appendix A.

4.8 Conclusion

The design of the analogue circuits were presented and discussed in this chapter. Various designs were considered for each functional unit in order to adhere to the specifications set in chapter 3. Each functional unit design consisted of a conceptual design, detail design and an estimate of the performance parameters achievable with that design. Two test circuits were also designed, built and tested in order to verify design concepts of the sensor driver. The results of these two test circuits are presented and discussed in chapter 7. The next chapter will discuss the design of the digital circuit of the sensor driver.

Chapter

5

Sensor driver digital design

In this chapter the design of the digital processing circuit is presented, along with the design of the firmware. The digital processing circuit consists of various elements, each of which will be discussed. The firmware design is given in the form of a detailed description of the algorithm used and all the interfaces in the design.

5.1 Digital processing circuit design

5.1.1 Digital processing circuit conceptual design

The digital controller to be implemented in the sensor driver design is an FPGA from Xilinx. An FPGA was chosen above a digital signal processor (DSP) like the TMS320 of Texas Instruments due to its parallel processing power, high number of I/O pins and very high speed processors. Since digital filters will have to be implemented for each digital signal (up to 10 signals), parallel processing and a high speed processor are essential for successful implementation of the sensor driver system. This was discussed in chapter 2. Figure 5-1 shows the functional diagram for the FPGA of the sensor driver.

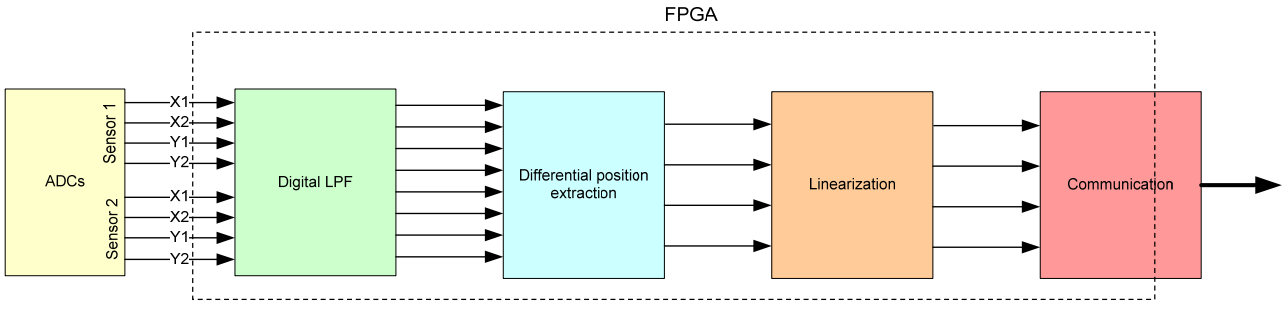


Figure 5-1 FPGA functional diagram

5.1.1.1 Input requirements

The FPGA receives its inputs from a number of ADCs by means of SPI communication. For a complete 5-axis AMB system, two radial- and one axial PCB sensor are required. With each radial sensor providing four differential position signals, and the axial sensor providing two differential position signals, the total number of signals that have to be digitally processed equals 10. Depending on the type of ADC used, up to 10 SPI pins must therefore be available, and must be able to receive data at a rate of 1 MSPS (mega-samples per second).

5.1.1.2 Processing requirements

The FPGA must be capable of digitally filtering the ten position signals simultaneously. This is done in order to remove all excess noise present. The FPGA must therefore be capable of implementing up to 10 digital filters semi-simultaneously (multiple simultaneously and multiple consecutively). After filtering the position values are differentially extracted by subtracting the digital values of opposite coils from each other. The position values are then linearized by passing it through a straight line function. Reading of all the values, processing and writing of all values must occur within a 20 kHz (50 µs) time frame.

5.1.1.3 Output requirements

The position values are communicated to a main controller via an RS-485 communications bus. The FPGA must therefore set-up the communications-driver and communicate the position values. The FPGA must be capable of writing all the position values out to an RS-485 driver and communicate the position values to a main controller within the 20 kHz (50 µs) time frame.

5.1.2 Digital processing circuit detail design

5.1.2.1 Requirement specifications

The requirement specifications for the FPGA of the digital processing circuit were obtained from the iSensor digital design [45], and are as follows:

- System gates > 1000K
- Logic cells > 25 000
- Total block RAM > 560 Kbits
- SPI capability
- Flash programming
- RS-485 communication

5.1.2.2 Circuit design

The FPGA digital processing circuit consists of the following elements:

1) FPGA processor
2) Flash programming
3) USB interface
4) Power supplies
5) Communication

Each of these elements will be discussed in detail in this section, as well as in the following sections.

1) FPGA processor

It was decided that a Xilinx FPGA would be used in this design, since the ADES main controller is based on a Xilinx architecture and a full Xilinx development environment will already be established. The Spartan-3 family was identified as a good choice for implementation in this project, as these devices are low cost while providing resources that are comparable to more expensive mid-range devices [39].

The FPGA receives its required power from the power supplies. After start-up, the FPGA reads the digital values from the ADCs through the SPI lines. These values are then passed through a differential position extraction function, filtered, and linearized before being sent to a communications-driver, which sends the processed position values to an external main controller. These position values are then used as input to the control system of an AMB.

2) Flash programming

The FPGA is programmed by loading its configuration data into reprogrammable, static CMOS configuration latches (CCLs). These jointly control all the functional elements and routing resources. The configuration data are stored on external PROMs (FLASH-based devices) or some other non-volatile medium. After power is applied to the FPGA, the configuration data is written to it by one of several means. The method that will be implemented in this design, is the Byte Peripheral Interface (BPI). This is a parallel configuration interface in which the FPGA acts as the master device, controlling the address pins and PROM signal in order to read configuration data from the FLASH-based device. In BPI mode, the FPGA configures itself from an industry-standard Parallel NOR Flash PROM. Using a Xilinx platform flash also has the benefit that the device can be programmed through the JTAG chain using the standard Xilinx Impact tool. The FPGA generates up to 24-bit address lines to access an attached parallel flash.

3) USB interface

The USB interface to the FPGA enables high speed communication between a computer and the FPGA. This is especially necessary during set-up of, amongst others, the programmable waveform generator. The USB interface will also be used in obtaining data from the sensor driver, or retrieving data saved in the SRAM.

4) Power supplies

The FPGA requires different power supplies than the analogue circuit, namely 1.2 V, 1.8 V, 3.3 V and 5 V. These voltages will be supplied by separate voltage supplies for the digital circuits.

5) Communication

As mentioned earlier, the FPGA communicates with an external main controller via an RS-485 communications bus. This is accomplished using an RS-485 communications-driver together with the FPGA. The FPGA sets up the driver to correctly convert the digital signals sent to it for RS-485 communication by adding start and stop bits, etc. The data is then sent at the required transmission rate to the external main controller.

5.1.2.3 Component selection

1) FPGA processor

The Spartan-3A DSP device XC3SD3400A-4FG676I was chosen for implementation in this design. This device was chosen due to its high number of system gates, logic cells, total block RAM, and multipliers. With 1 MSPS sample rate and processing speed in excess of 50 MHz, this device will be capable of performing a large number of multiplication operations per sample of the ADC. It would therefore be sufficient for implementation in this design. The FG676 package was chosen because of its more relaxed ball spacing (1 mm) and slightly larger package size. With a larger ball spacing, via placement becomes less critical, and a good breakout can be achieved. This will make manufacturing of the board easier and will result in a more reliable board [41]. The FPGA circuit is also designed to be pin-compatible with the "smaller" and less expensive XC3SD1800A-4FG676I Spartan-3A DSP device. This allows for more economical and cost effective future implementations of the sensor driver system.

The relevant specifications of the **XC3SD3400A** are [40]:

- System gates: 3400K
- Logic cells: 53712
- Block RAM: 2268 Kbits
- DSP slices: 126
- Multipliers: 18-bit by 18-bit
- Maximum user I/O: 469

2) Flash programming

The Spartan-3A DSP will be used in conjunction with a parallel Xilinx Platform flash device XCF16PVO48C. The XCF16PVO48C is an in-system programmable PROM used for the configuration of Xilinx FPGAs. This device was chosen because of its relatively low cost and ease of programming using the Xilinx tool chain [41].

The relevant specifications of the **XCF16PVO48C** are [41]:

- 1.8 V supply voltage
- In-system programmable PROMs
- Low-power advances CMOS NOR Flash process
- JTAG (IEEE Standard 1149.1/1532 Boundary scan)

- JTAG command initiation of standard FPGA configuration
- Cascadable for storing longer or multiple bitstreams
- Serial or parallel FPGA configuration interface (up to 33 MHz)
- Built-in data decompressor compatible with Xilinx advanced compression technology

The circuit schematic of the Flash programming circuit as implemented in the sensor driver is shown in Figure 5-2.

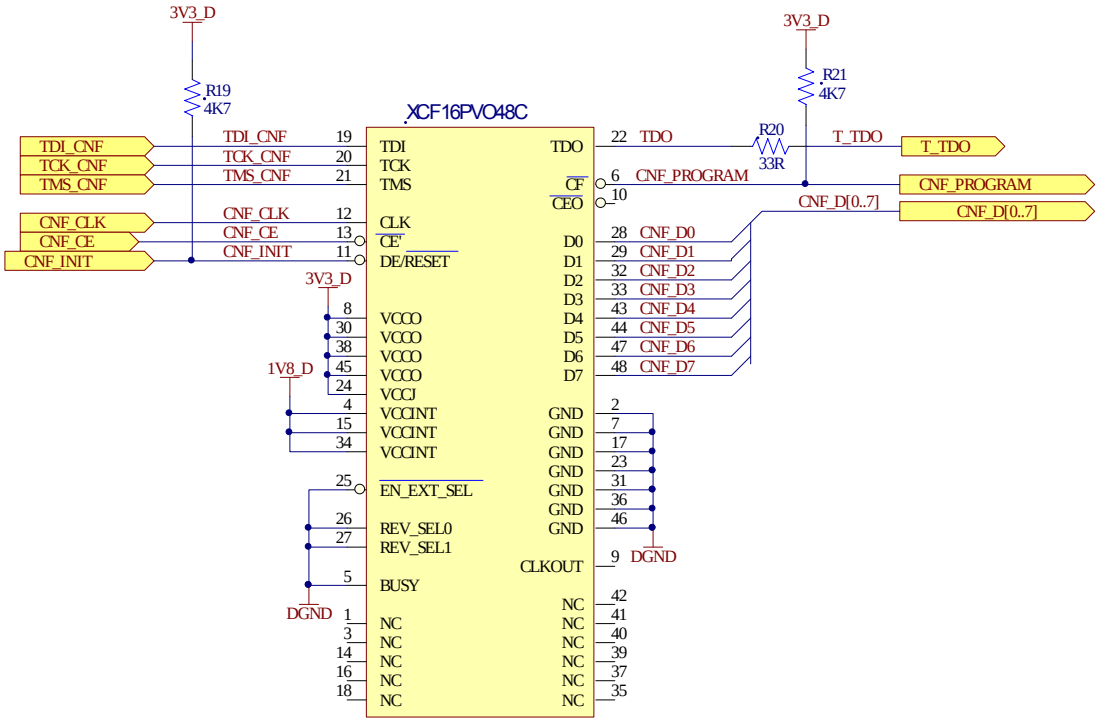


Figure 5-2 Schematic of Flash programming circuit

3) USB interface

The USB interface consists of a single-chip USB to UART bridge, namely the CP2102-GM. It is an integrated USB transceiver, requiring no additional external resistors. The chip also does not require an external crystal for its integrated clock. The connection between the USB connector and the USB bridge is protected against electro-static discharge (ESD) by the ESDA6V1 quad bidirectional transil suppressor.

The relevant specifications of the **CP2102-GM** are [42]:

- 3.3 V supply voltage
- Integrated 1024-Byte EEPROM for vendor ID, product ID, serial number, power descriptor, release number, and product description strings.
- On-chip power-on reset circuit
- On-chip voltage regulator: 3.3 V output
- USB specification 2.0 compliant; full-speed (12 Mbps)
- Supports all handshaking and modem interface signals
- Supports baud rates of 300 bps to 1 Mbps
- 576 byte receive buffer; 640 byte transmit buffer
- Event character support
- Line break transmission

The circuit schematic for the USB interface circuit is shown in Figure 5-3.

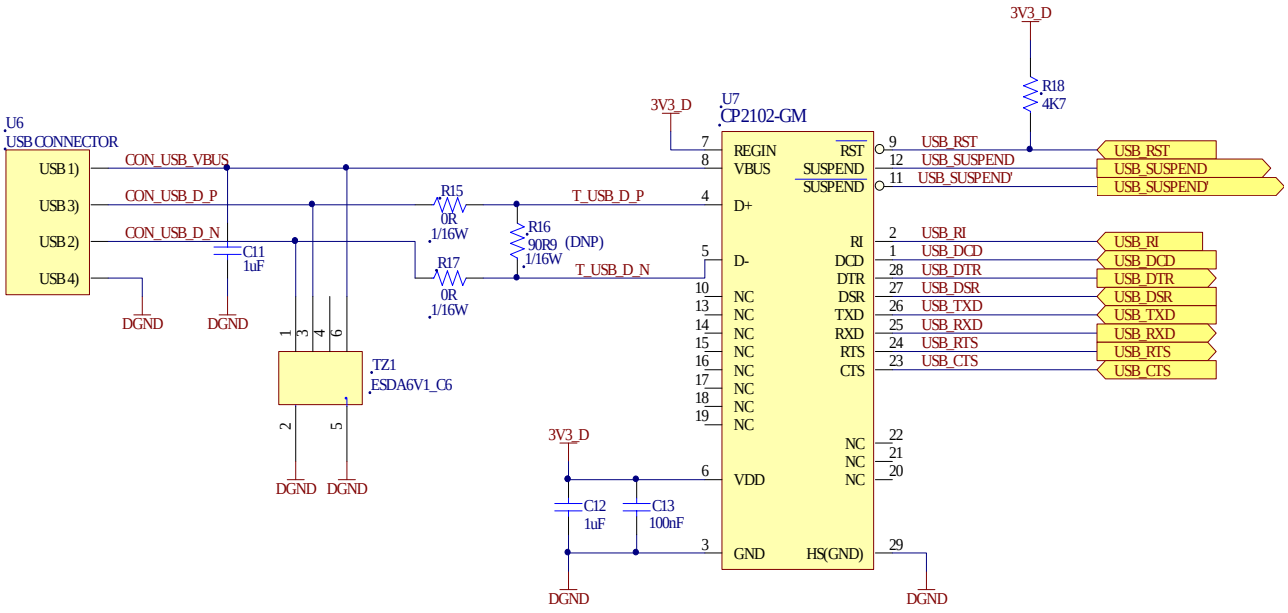


Figure 5-3 Circuit schematic of USB interface circuit

4) Digital power supply circuit

The power supply circuit of the digital processing circuit consists of dc-dc converters and regulators in order to convert the received 24 V into the required 5 V, 3.3 V, 1.8 V, and 1.2 V supplies. The RS-485 communication circuit also requires a separate, floating and isolated 5 V power supply. The conceptual design of the digital power supply is shown in Figure 5-4.

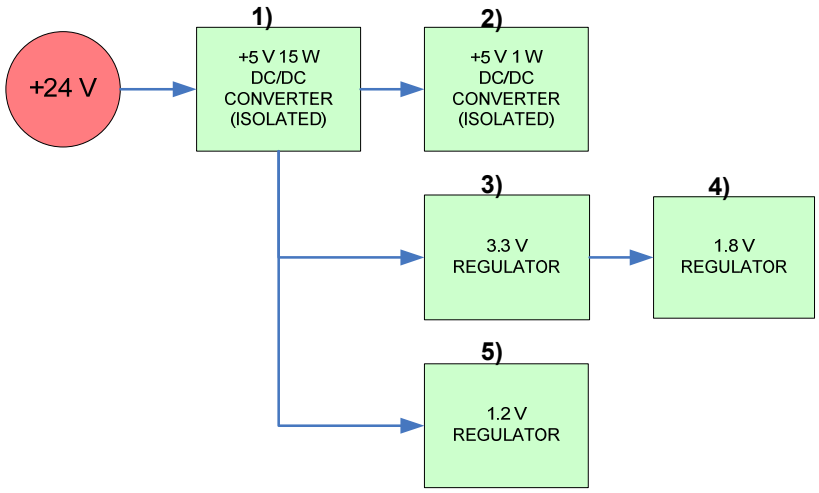


Figure 5-4 Conceptual design of digital power supply circuit

The following components (as corresponding to Figure 5-4) were selected for the digital power supply circuit:

1) THD15-2411:	+5 V 15 W DC/DC converter
2) TES1-0511:	+5 V 1 W DC/DC converter
3) LM20133MH:	3A, Synchronous buck regulator with Input synchronization
4) TPS73218DBVT:	1.8 V low dropout regulator with reverse current protection
5) LM20133MH:	3 A, synchronous buck regulator with input synchronization

5.1.2.4 Communication

The FPGA uses two RS-485 isolated half-duplex differential line transceivers for the RS-485 communication with the main controller. The ISO3088DW was selected for this design. The relevant specifications of the **ISO3088DW** are [44]

- 4000-V_{PEAK} isolation, 560-V_{PEAK} V_{IORM}
- 1/8 Unit load – up to 256 nodes on a bus
- Meets or exceeds TIA/EIA RS-485 requirements
- Signalling rates up to 20 Mbps
- Thermal shutdown protection
- Low bus capacitance – 16 pF
- 50 kV/μs typical transient immunity
- Fail-safe receiver for bus open, short, idle
- 3.3 V inputs are 5 V tolerant

The circuit schematic of the communications circuit is shown in Figure 5-5. The ISO3088DW provides galvanic isolation between its inputs and outputs, which makes them ideal for long transmission lines. The output signals are protected against ESD by ESDA6V1 quad bidirectional transil suppressors.

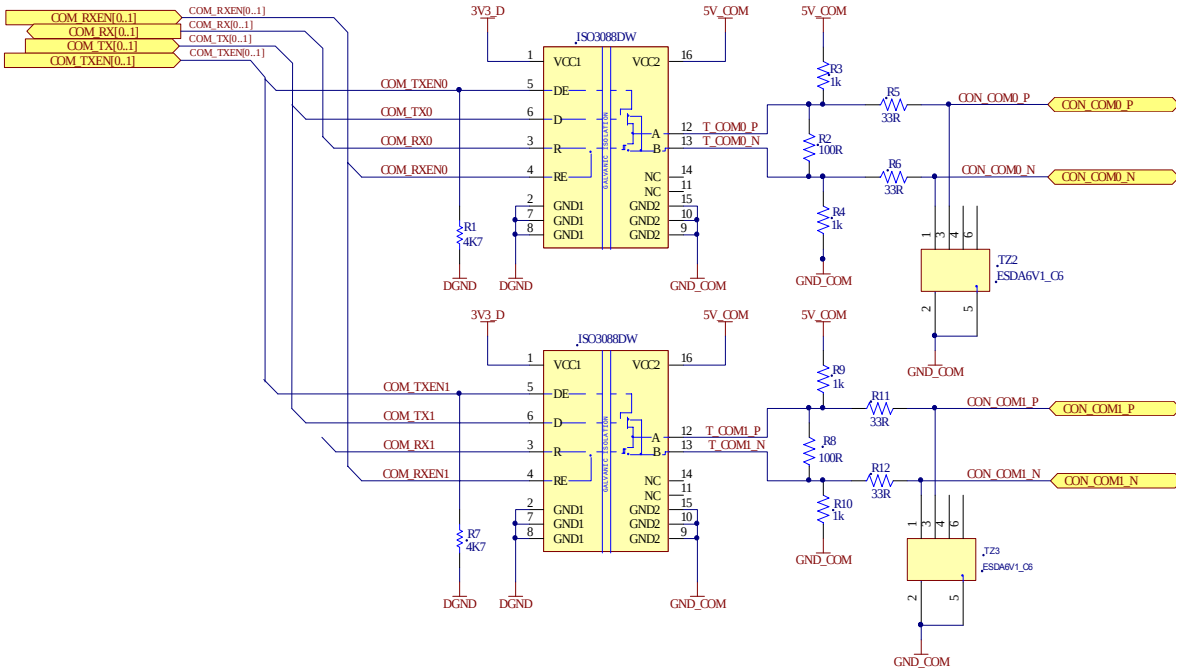


Figure 5-5 Circuit schematic of RS-485 communication circuit

5.2 Firmware design

The firmware design was completed by means of a software development process. This process includes the software requirement specification in natural language, the system software model, the structural analysis of the sensor driver software and the design.

5.2.1 Requirement specification of firmware design

In this section the requirement specifications of the sensor driver software is discussed. Figure 5-6 shows a basic input-output flow diagram for the digital implementation, illustrating the main functional software blocks. The inputs are obtained from the ADCs, and the outputs are sent to the communication drivers. The main functional software blocks as given in the figure are the low-pass filters (LPFs), differential position extraction, linearization, scaling and communication.

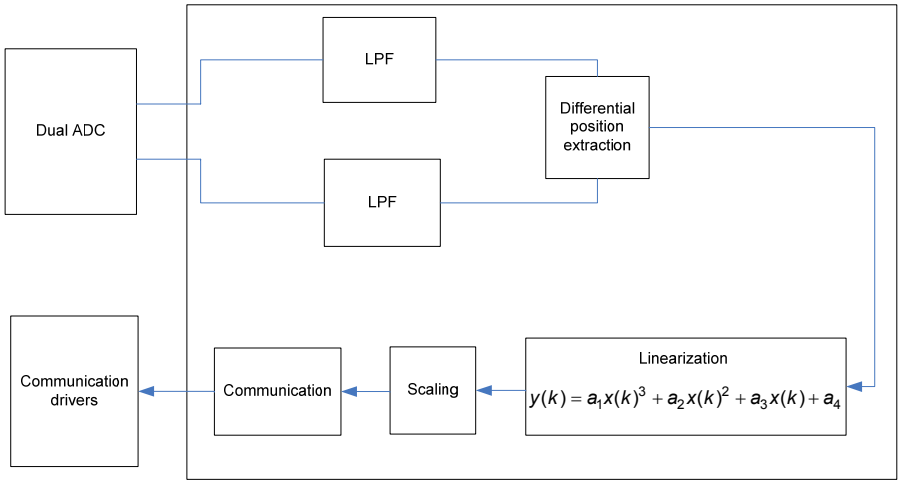


Figure 5-6 Input-output flow diagram of digital implementation

Figure 5-7 shows the sensor driver block diagram. From this diagram the sub-components requiring software development can be identified, namely the programmable waveform generator, the analogue-to-digital converters, the USB interface, the memory interface, the RS485 communications interface and the LED display. Each of these sub-components will now be discussed.

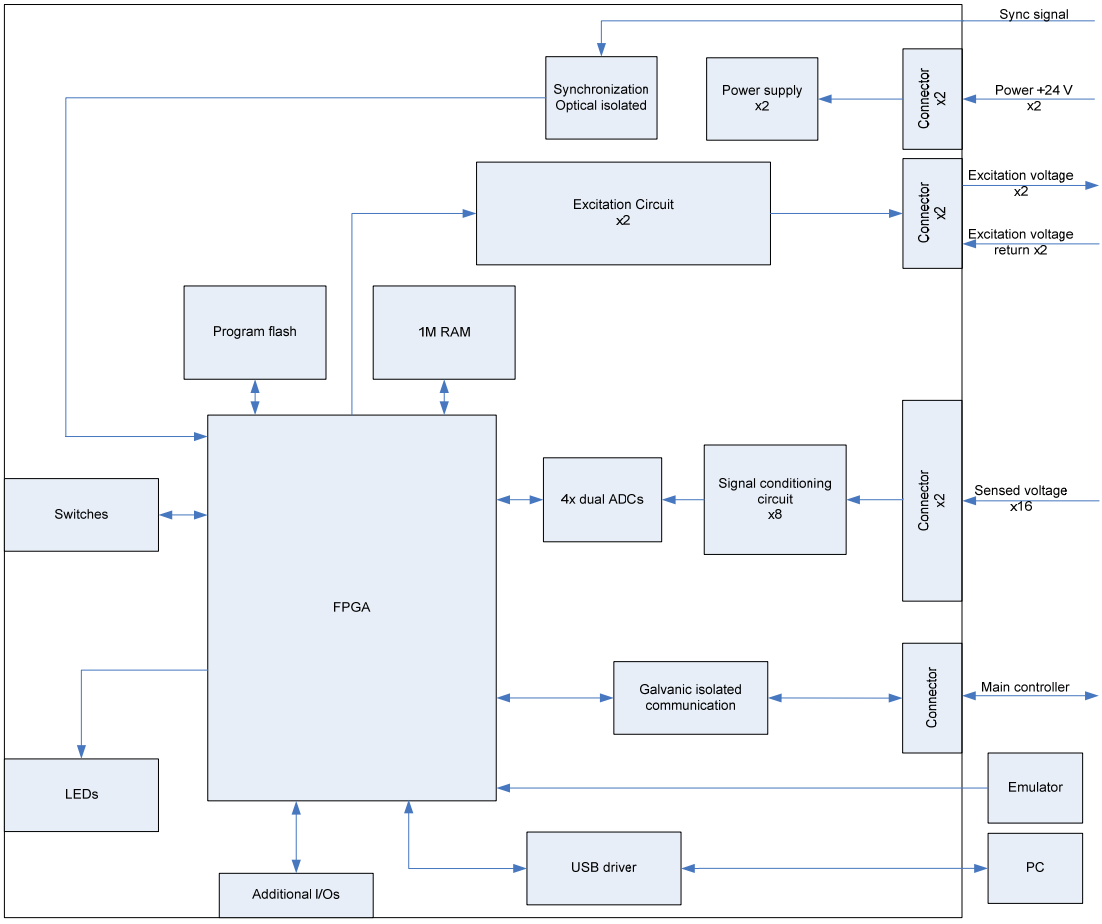


Figure 5-7 Sensor driver block diagram

5.2.1.1 Programmable waveform generator

The programmable waveform generator requires three communication lines for setup purposes for each AD9833 device used [27]. In the final sensor driver design the master clock signals of the two AD9833s are supplied by the FPGA and not by an external clock or crystal as was the case in the sensor driver test circuit. A software clock must therefore be generated to function as the master clock. The program required to setup the AD9833 can be derived from the timing diagrams of the device as given in the datasheet.

5.2.1.2 Analogue to digital converters

From the AD7367 ADC datasheet it is determined that nine communication lines are required to connect one ADC to the FPGA. These nine communication lines are: SCLK, CNVST, CS, BUSY, ADDR, RANGE0, RANGE1, DOUTA and DOUTB. From the timing diagrams supplied in the device's datasheet, the required program to operate the AD7367 can be derived [38].

5.2.1.3 USB interface

Software development for the CP2102 USB interface requires the device's timing diagram, as supplied in the datasheet [42]. Software must be developed for interfacing the USB with the RAM via the FPGA in order to access the data. The interface between the USB driver and the FPGA consists of 10 data lines, of which only some are to be implemented in this design.

5.2.1.4 Memory interface

The interface software for the IS61WV102416BLL used in the sensor driver design must be designed using the device's timing diagram given in the datasheet [43]. The data on the RAM must be accessible via the USB port in order to obtain measurement results from the sensor to be used in the linearization and scaling processes, as well as to be able to validate the sensor driver system.

5.2.1.5 RS-485 interface

The RS485 communication lines, using the ISO3088 half-duplex communications driver, must be set up correctly in order to send the position information to the main controller. The frequency rate is limited by the communications driver to 20 MBPS. The design and development of the RS-485 interface is not part of the scope for this Masters project, but is done by a fellow Masters student [46].

5.2.1.6 LED display

The LEDs are connected to I/O pins of the FPGA. The main function of the LEDs are to indicate the correct operation or completion of certain software flags en processes. The first software flag displays that the code is operating correctly. The second and third flags are currently undefined, but will also indicate correct operation or completion of a certain process.

5.2.1.7 Digital implementation method

From Figure 5-6 the basic digital implementation method can be seen. The data received from the ADC is passed to the digital implementation method. The first part of the method consists of a predefined FIR low-pass filter (LPF). This LPF will be designed using Matlab's fdatool. The differential signals are then subtracted from each other to obtain the true position signal. The true position signal is then passed through a nonlinear compensation function in order to linearize the position signals. This output is then sent to the main controller via the RS485 communication.

5.2.2 System software model

The system model as it is to be implemented in software on the FPGA is shown in Figure 5-8. The software blocks at the outer line of the FPGA represent the interface software between physical components and the FPGA. The internal interfaces or data transmission software are represented by the software blocks on the inside of the FPGA outer line. In the next section the system software model will be used to determine the classic analysis.

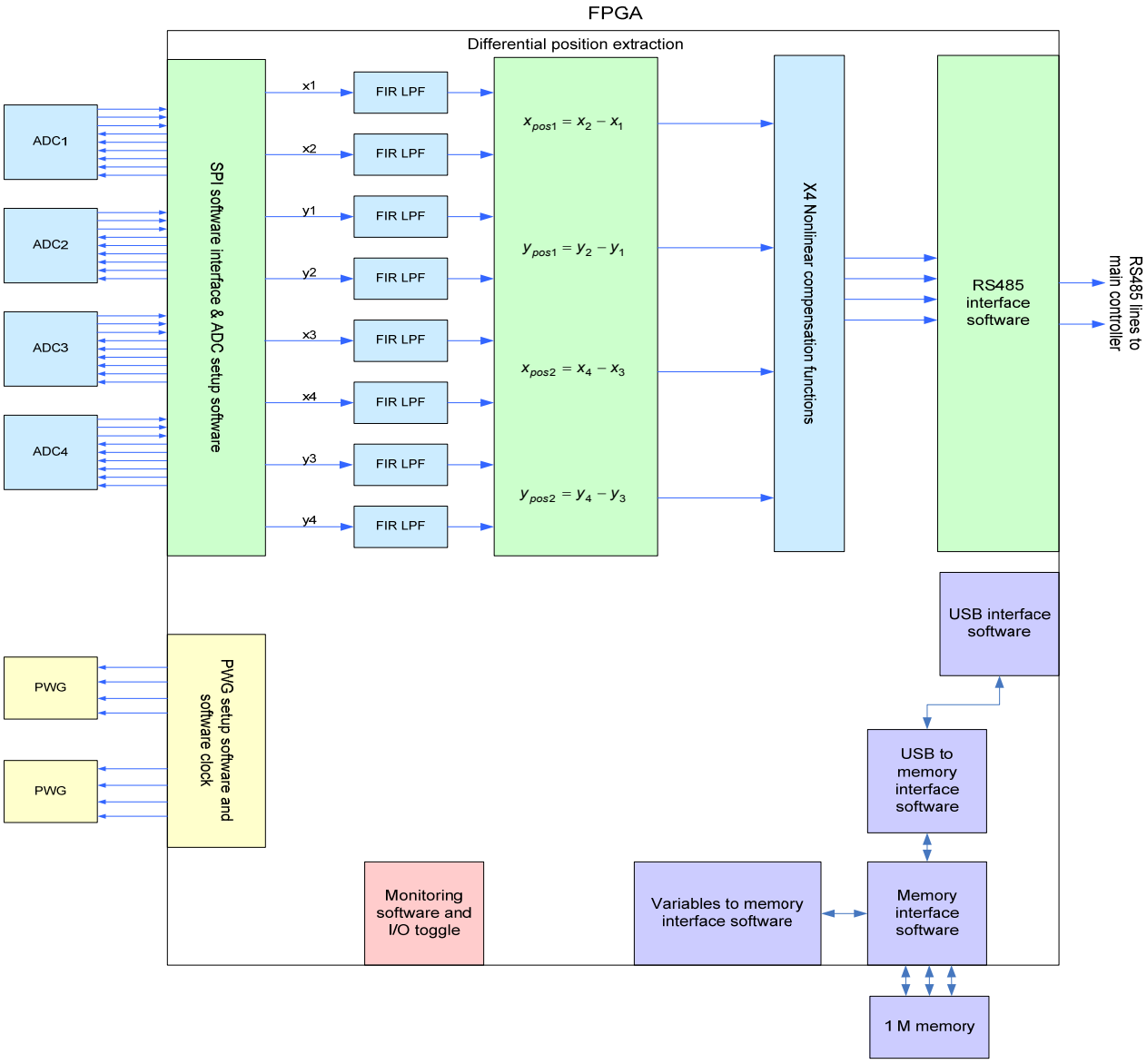


Figure 5-8 System model

5.2.3 Classic analysis

In this section each of the components shown in the system software model will be analysed using the Gane and Sarsen's structure. In the case of multiple copies of components, analysis will be done on a single component only for simplicity. Each data flow component will be discussed in detail so that the interfaces between software blocks and hardware are clearly defined.

5.2.3.1 Programmable waveform generator

The software structure of the PWG is shown in Figure 5-9. The direction of data flow is only in one direction from the FPGA to the PWG. There are four dataflow lines, namely MCLK, FSYNC, SDATA and SCLK. The purpose of MCLK is to supply the AD9833 with a master clock. The master clock frequency should be in the range of 25 MHz for the sensor driver design to ensure high output accuracy. SDATA is the serial data input. A 16-bit serial data-word is written to SDATA to set up the AD9833 device. The serial data is then clocked into the AD9833 on each falling edge of the SCLK signal. FSYNC is an active low control input and is the frame synchronization signal for the input data. When FSYNC is made low, the internal logic is informed that a new word is being loaded into the device. In this design, the FSYNC signal will be used to synchronize the two AD9833 ICs [27].

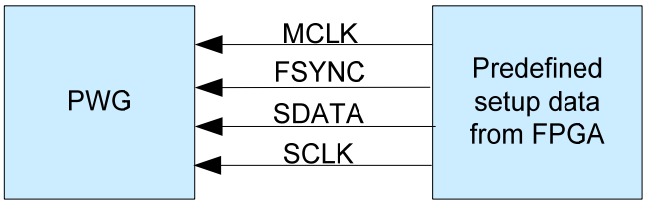


Figure 5-9 PWG structure analysis

The timing diagram and timing characteristics of the AD9833 PWG are shown in Figure 5-10 [27]. This timing diagram will be used to design the interface software.

TIMING CHARACTERISTICS* (VDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, unless otherwise noted.)

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	40	ns min	MCLK Period
t_2	16	ns min	MCLK High Duration
t_3	16	ns min	MCLK Low Duration
t_4	25	ns min	SCLK Period
t_5	10	ns min	SCLK High Duration
t_6	10	ns min	SCLK Low Duration
t_7	5	ns min	FSYNC to SCLK Falling Edge Setup Time
$t_{8\ min}$	10	ns min	FSYNC to SCLK Hold Time
$t_{8\ max}$	$t_4 - 5$	ns max	
t_9	5	ns min	Data Setup Time
t_{10}	3	ns min	Data Hold Time
t_{11}	5	ns min	SCLK High to FSYNC Falling Edge Setup Time

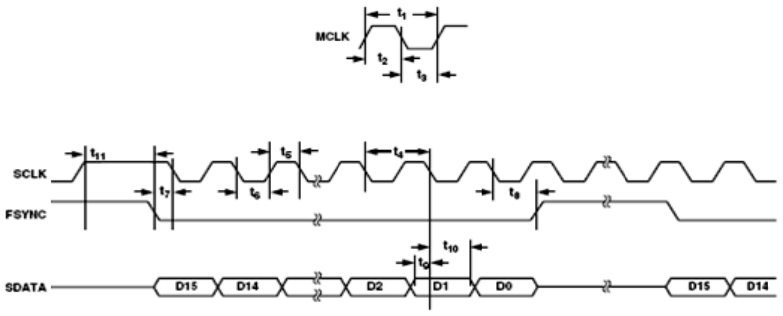


Figure 5-10 PWG timing characteristics and timing diagram [27]

5.2.3.2 Analogue to digital converters

The structure analysis of the ADC is shown in Figure 5-11. The direction of dataflow is in both directions, namely three from the ADC to the FPGA and six from the FPGA to the ADC. There are nine dataflow lines, namely CS, CNVST, DOUTA, DOUTB, BUSY, ADDR, RANGE1 and RANGE0. CS is an active low logic input, which frames the serial data transfer. When low, the output bus is enabled and the conversion result is sent on both D_{OUT} pins. SCLK supplies the AD7367 with a master clock. For this design, the master clock should be in the range of 20 MHz in order to meet the required SPI throughput of 1 MHz. D_{OUT}A and D_{OUT}B are the serial data outputs. The data output to each pin is supplied as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 14 SCLK cycles are required to access the data. The data simultaneously appears on both pins from the simultaneous conversions of both ADCs, and the data stream consists of 14 bits which is provided MSB first. BUSY is the busy output. It makes a high transition when a conversion is started and remains high until the conversion is complete. ADDR is a logic input selecting the multiplexer. It is used to select the pair of channels to be simultaneously converted, either channel 1 of both ADC A and ADC B, or channel 2 of both ADC A and ADC B. The logic state on this pin is latched on the rising edge of BUSY to set up the multiplexer for the next conversion. RANGE0 and RANGE1 are logic inputs selecting the analogue input range. The polarity on these pins determines the input range of the analogue input channels [38].

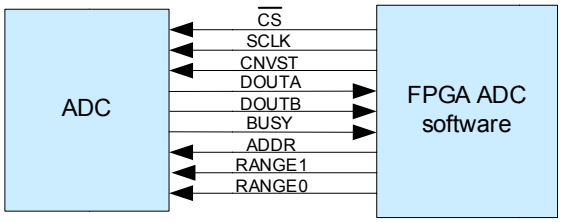


Figure 5-11 ADC structure analysis

Figure 5-12 and Figure 5-13 show the timing diagram and specifications of the AD7367 ADC.

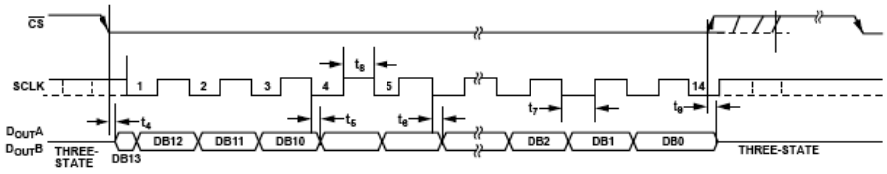


Figure 5-12 Serial interface timing diagram for AD7367 ADC

TIMING SPECIFICATIONS

AV_{CC} = DV_{CC} = 4.75 V to 5.25 V, V_{DD} = 11.5 V to 16.5 V, V_{SS} = −16.5 V to −11.5 V, V_{DRIVE} = 2.7 V to 5.25 V, T_A = −40°C to +85°C, unless otherwise noted.[1]

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX}		Unit	Test Conditions/Comments
	2.7 V ≤ V_{DRIVE} < 4.75 V	4.75 V ≤ V_{DRIVE} ≤ 5.25 V		
$t_{CONVERT}$				Conversion time, internal clock; $\overline{CNVST}$ falling edge to BUSY falling edge
	680	680	ns max	AD7367
	610	610	ns max	AD7366
f_{SCLK}	10	10	kHz min	Frequency of serial read clock
	35	48	MHz max	
t_{QUIET}	30	30	ns min	Minimum quiet time required between the end of serial read and the start of the next conversion
t_1	10	10	ns min	Minimum $\overline{CNVST}$ low pulse
t_2	40	40	ns min	$\overline{CNVST}$ falling edge to BUSY rising edge
t_3	0	0	ns min	BUSY falling edge to MSB, valid when $\overline{CS}$ is low for t_4 prior to BUSY going low
t_4	10	10	ns max	Delay from $\overline{CS}$ falling edge until Pin 1 ($D_{OUT}A$) and Pin 23 ($D_{OUT}B$) are three-state disabled
t_5[2]	20	14	ns max	Data access time after SCLK falling edge
t_6	7	7	ns min	SCLK to data valid hold time
t_7	0.3 × t_{SCLK}	0.3 × t_{SCLK}	ns min	SCLK low pulse width
t_8	0.3 × t_{SCLK}	0.3 × t_{SCLK}	ns min	SCLK high pulse width
t_9	10	10	ns max	$\overline{CS}$ rising edge to $D_{OUT}A$, $D_{OUT}B$, high impedance
$t_{POWER-UP}$	70	70	µs max	Power-up time from shutdown mode; time required between $\overline{CNVST}$ rising edge and $\overline{CNVST}$ falling edge

[1] Sample tested during initial release to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V. All timing specifications are with a 25 pF load capacitance. With a load capacitance greater than 25 pF, a digital buffer or latch must be used. See the Terminology section, Figure 25, and Figure 26.
[2] The time required for the output to cross is 0.4 V or 2.4 V.

Figure 5-13 Timing specifications for the ADC [38]

5.2.3.3 USB interface

As already mentioned, the CP2102 USB interface IC is used in the sensor driver design. The structure analysis for the USB interface is shown in Figure 5-14. For the sensor driver design a standard UART communication method will be used between the FPGA and the USB interface IC, requiring only the RX and TX pins to be used. The rest of the interface pins will not be used, but will still be connected to the FPGA [42].

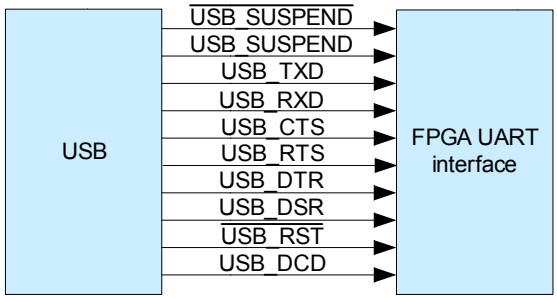


Figure 5-14 USB structure analysis

5.2.3.4 Memory interface

The IS61WV102416BLL memory module is a high speed asynchronous CMOS static RAM. Figure 5-15 shows the structure analysis of the SRAM module. The interface software must be developed using the device's timing diagram provided in the datasheet [43].

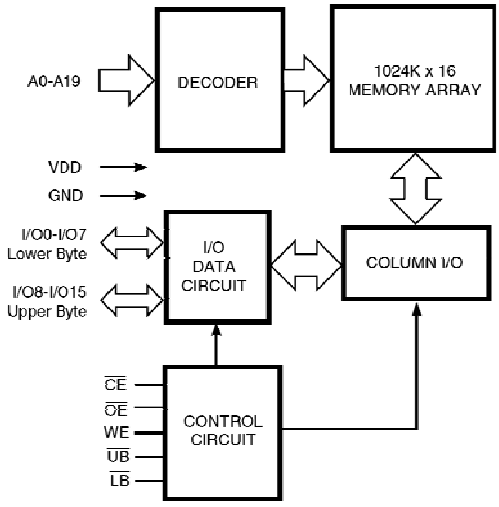


Figure 5-15 SRAM structure analysis [43]

The truth table for the control inputs is shown in Figure 5-16. The truth table will be required in coding the read and write cycles of the SRAM.

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

Figure 5-16 Control inputs truth table [43]

The timing constraints for the read cycle of the SRAM IC are shown in Figure 5-17, and for the write cycle in Figure 5-18.

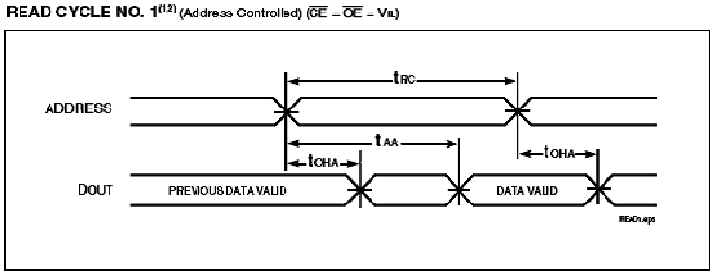


Figure 5-17 Read cycle timing diagram [43]

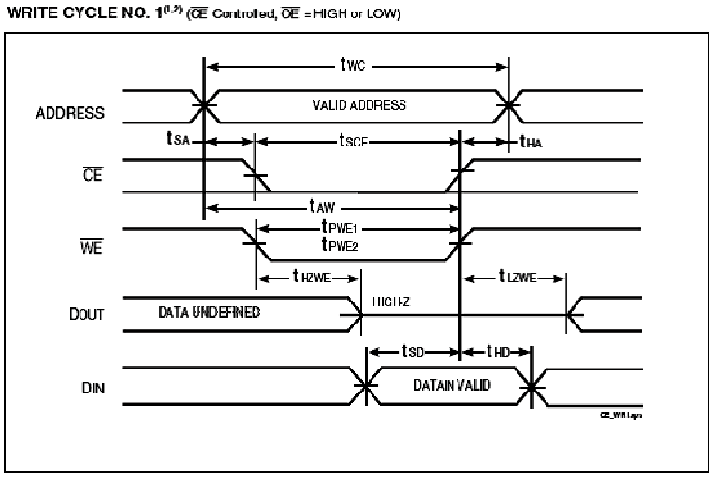


Figure 5-18 Timing diagram of write cycle [43]

5.2.3.5 RS485 interface

As previously mentioned, the RS485 software interface will be developed by another current Master's degree student within the McTronX research group [46].

5.2.3.6 LED display

The LED interface requires the toggling of I/O pins in order to switch the LEDs on or off. The structure analysis for the LED interface is shown in Figure 5-19.

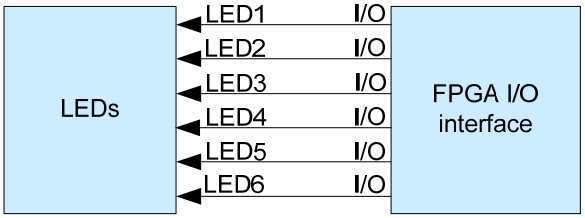


Figure 5-19 LED interface structure analysis

5.2.3.7 Digital processing method

The digital processing algorithm forms the main component of the sensor driver firmware design. The inputs of the algorithm are the ADC inputs. The structure analysis of the digital processing algorithm is shown in Figure 5-20. The inputs from the ADCs are first passed through a low-pass filter (LPF). The differential signals are then subtracted from each other in order to obtain the true position value. This value is then linearized through nonlinear compensation, and sent to the RS-485 communication drivers.

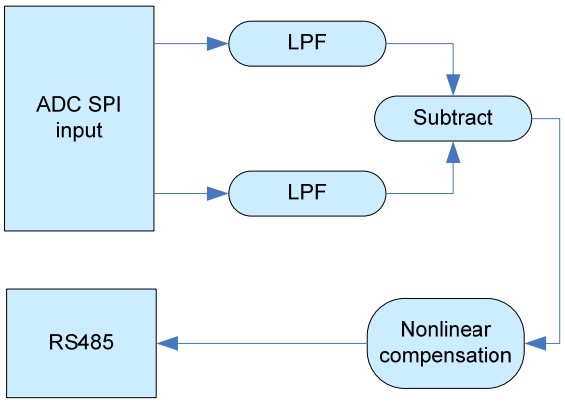


Figure 5-20 Digital processing algorithm structure analysis

5.2.4 Sensor driver software structure diagram

Figure 5-21 shows the overall software structure of the sensor driver firmware design. In this design different structures will be connected via dual-port RAM (DPR) blocks. The programming of the sensor driver board will be based on this software structure diagram.

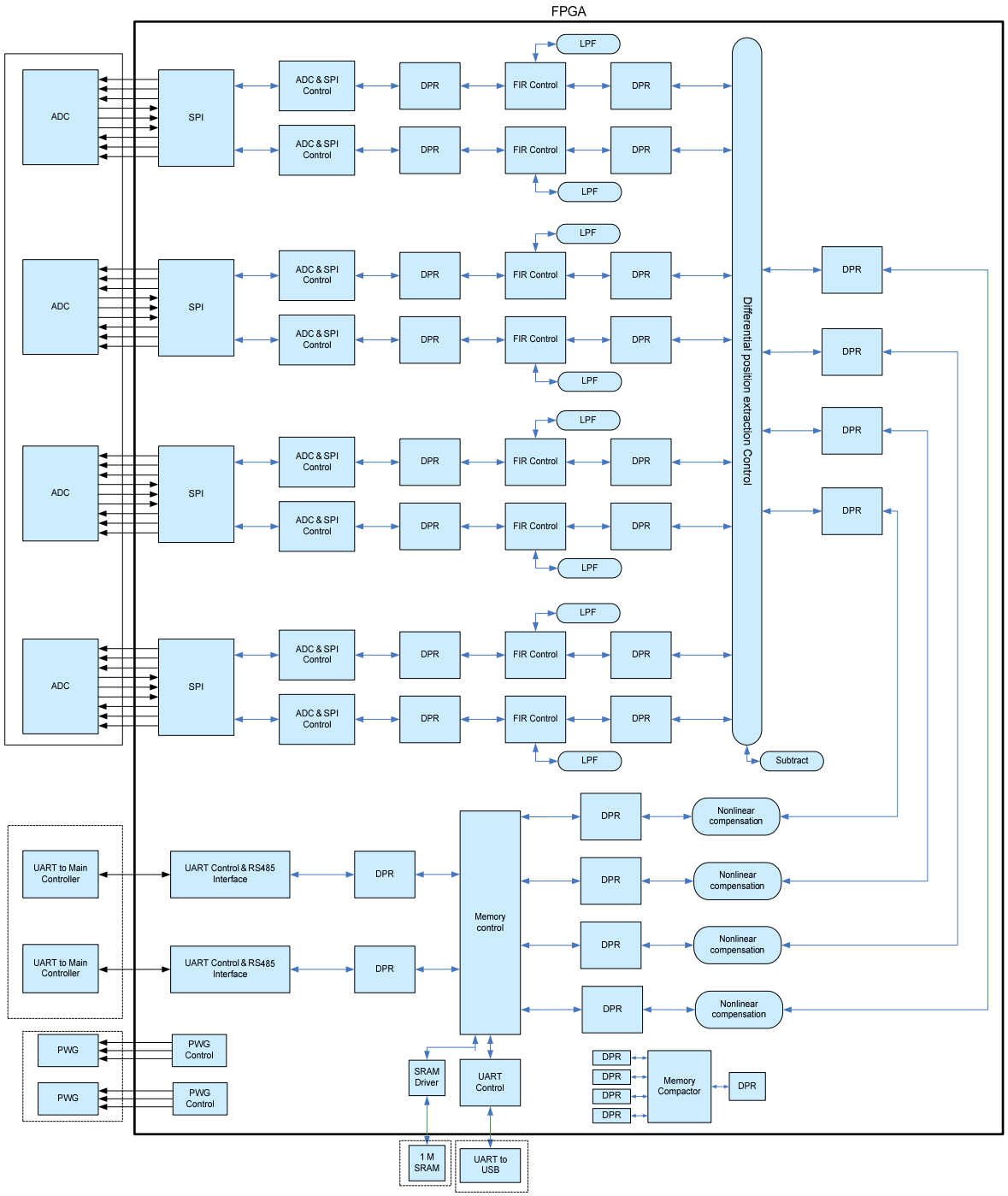


Figure 5-21 Sensor driver software structure diagram

5.2.5 VHDL code analysis

The analysis of the VHDL code used to implement the firmware is done by means of describing and analysing all the interfaces as seen in the sensor driver software structure diagram (Figure 5-21).

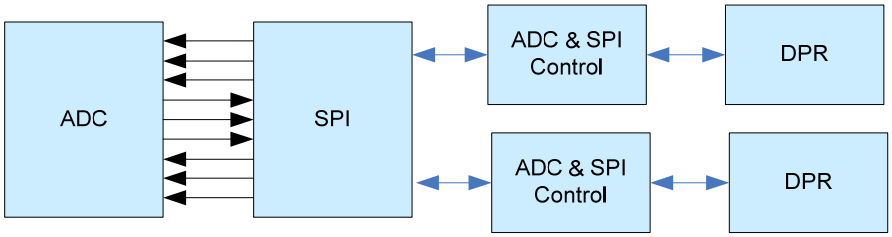


Figure 5-22 SPI basic block diagram

5.2.5.1 ADC to SPI interface

The first interface is between the ADC and the FPGA, and consists of an SPI software component. The SPI software component consists of the input signals from the ADCs, the SPI and ADC control blocks and the DPR interface. Figure 5-22 shows the basic block diagram of the ADC to SPI interface. The interface between the ADC and the SPI is defined by the ADC's datasheet. Nine dataflow signals pass between the ADC and the SPI, of which three are logic inputs required for setup, two are serial data outputs, one is the ADC SPI clock, and three are for ADC control. SCLK supplies the ADC with its master clock in the range of 20 MHz. RANGE0 and RANGE1 are logic inputs for the setup of the analogue input range. ADDR is also a logic input that selects the pair of channels to be simultaneously converted. For the ADC to begin conversion, $\overline{\text{CNVST}}$ must be taken low. On the falling edge of $\overline{\text{CNVST}}$ BUSY goes high to indicate that the conversion is taking place. After the conversion has been completed, BUSY goes low to indicate the end of the conversion. In order to access the data, $\overline{\text{CS}}$ must be taken low for 14 clock cycles in order to enable the output bus and place the data on D_{OUTA} and D_{OUTB}.

5.2.5.2 SPI to ADC & SPI control interface

The interface between the SPI and the ADC & SPI Control can be defined by the programmer. In this case an enable signal will be used to trigger the SPI to start sending and receiving data. The enable signal is active high and will be triggered only for one system clock cycle (100 MHz). When the enable is activated by the SPI Control, the SPI must read the data (vector

format) which must be written to the ADC. This data is sent via the SPI to the ADC to set up the ADC for the next cycle. In the same time the data is written to the ADC, the sampled data is sent to the SPI from the ADC. Both of these data packages have a data length of 14. After the data have been retrieved from the ADC, the done signal can be triggered, which sends an active high signal to the ADC & SPI Control. In this design the aim is to operate the ADC at its maximum frequency which is 1 MHz.

- **Throughput rate**

Since the system clock operates at 100 MHz, the SPI must ideally be a factor 5 smaller than the system clock which results in a 20 MHz SPI clock (max. SPI clock), but a factor of 5 results in 2.5 system clock cycles high and 2.5 low. This results in a factor of 6 to be used and results in 3 cycles high and 3 cycles low. Due to this the performance of the ADC is altered and this will be investigated. The throughput rate can be calculated as follows:

$$Throughput = \frac{1}{14 \times t_{SCLK} + t_{Quiet}} \approx 1.11 \text{ MHz}$$

where t_{SCLK} is $\frac{1}{f_{SCLK}}$, f_{SCLK} = $\frac{100\ MHz}{6}$ = 16.6667 MHz and t_{Quiet} = 60 ns.

5.2.5.3 DPR interface

The DPR interface refers to all DPR write and read interfaces throughout the sensor driver software structure diagram. Figure 5-23 shows the basic inputs and outputs of the DPR. For a write procedure, the address to which must be written is placed on ADDW, and the data to be written is placed on DIN. WE is then pulsed high to write the data to the DPR. For a read procedure, the address from which the data must be read is placed on ADDR, and the data is written out on DOUT.

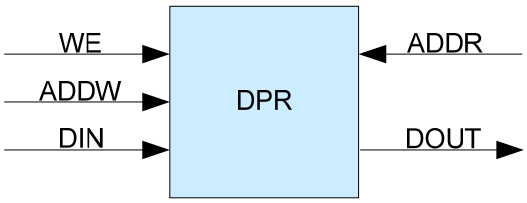


Figure 5-23 Inputs and outputs of DPR

5.2.5.4 FIR Control and FIR LPF interface

Figure 5-24 shows the basic block diagram for the FIR LPF. The interface between the FIR Control and the FIR LPF consists of six data lines to co-ordinate the I/O operations, namely ND (New Data), RFD (Read For Data), RDY (Ready), CLK, DIN and DOUT. When data is ready on DIN, ND must be made high in order to load the new input sample into the filter, on condition that the core is ready to accept new input samples. When the core is ready to accept a new input sample, the RFD signal goes high. As soon as a new output signal is available on DOUT, RDY goes high for a single clock period. CLK provides the system clock to the core, where the clock rate may be greater than or equal to the sample frequency of the input signal.

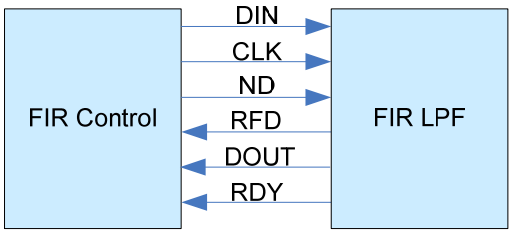


Figure 5-24 FIR LPF basic block diagram

5.2.5.5 Differential position extraction control and subtract interface

Figure 5-25 illustrates the interface between the differential position extraction Control and the subtract. The two differential values received by the differential position extraction control is sent to the subtract software block, where the signals are subtracted from each other to obtain the output value (DOUT = DIN1-DIN2).

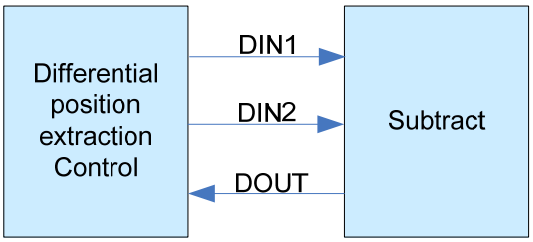


Figure 5-25 Differential position extraction basic block diagram

5.2.5.6 Nonlinear compensation interface

Figure 5-26 shows the interface between the nonlinear compensation control and the linearization function. The Linearization function receives a value DIN from the nonlinear compensation control, executes the function $y(k) = a_1 x(k)^3 + a_2 x(k)^2 + a_3 x(k) + a_4$ by replacing $x(k)$ with DIN, and yields an output $y(k)$ which is sent as DOUT back to the nonlinear compensation control.

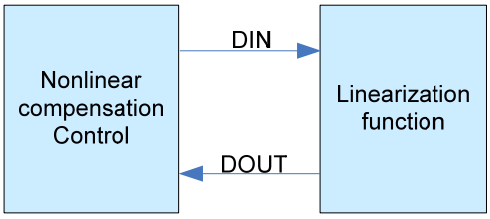


Figure 5-26 Block diagram of the Nonlinear compensation interface

5.2.5.7 Memory control and RAM driver interface

The interface between the Memory Control and RAM driver is shown in Figure 5-27. The CLK signal once again provides the master clock for the RAM driver, while the RESET signal resets all the variables of the RAM driver at system start-up. For a write operation data is placed on DataWrite and the address to which the data must be written is placed on ADDR. To start writing to the RAM driver, WE is made high. As soon as the RAM driver has finished writing the data to the RAM, DONE goes high. The RAM driver is then ready to receive the next data. For a read operation, the address of the data to be read is placed on ADDR and RE is taken high. The DONE signal then goes low while the RAM driver reads the data. As soon as the RAM driver has finished reading the data from the RAM, the DONE signal goes high again. The data is then available on DataRead.

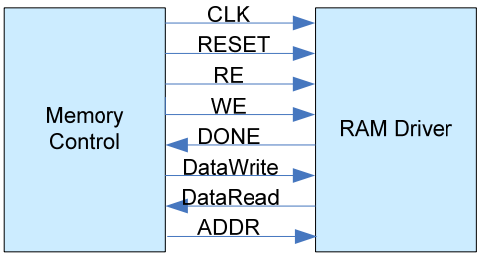


Figure 5-27 Block diagram of interface between memory control and RAM driver

5.2.5.8 RAM driver and RAM interface

Figure 5-28 shows the interface between the RAM driver and the RAM. $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, $\overline{UB}$ and $\overline{LB}$ are active low inputs controlling the read and write operations of the RAM. DATA is an input/output signal, and ADDR is the address input to the RAM. For a write operation, the RAM driver places the data to be written on DATA, places the data address on ADDR, and takes $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, $\overline{UB}$ and $\overline{LB}$ low. When the write operation has been completed, $\overline{UB}$ and $\overline{LB}$ are taken high, which notifies the RAM driver to make DONE high. For a read operation, the RAM driver places the data address on ADDR and takes $\overline{WE}$ high and $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, $\overline{UB}$ and $\overline{LB}$ low. The data is then placed on DATA and $\overline{UB}$ and $\overline{LB}$ are taken high, which notifies the RAM driver to make DONE high.

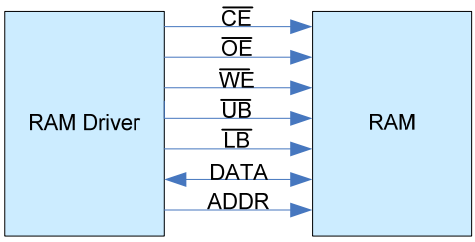


Figure 5-28 Block diagram of RAM driver and RAM interface

5.2.5.9 RS485 interface

The position values are passed on to the RS485 interface, which includes among others a UART Control. The RS485 interface does not form part of the sensor driver project, but was accomplished by [46].

5.2.5.10 PWG to PWG Control interface

Figure 5-29 shows the interface between the PWG and the PWG Control. The AD9833 PWG has a standard 3-wire serial interface that is SPI compatible. The data is loaded into the device as a 16-bit word under the control of SCLK, which is the serial clock input. FSYNC is a level triggered input that performs frame synchronization on the data and acts as a chip enable. SDATA is a 16-bit serial data input. To start the serial communication, FSYNC must first be made low. The control register data is then placed on SDATA in multiple write operations. The control register data consists of setting the reset bit, writing the least-significant byte (LSB) of the desired frequency, followed by the most-significant byte (MSB), writing the values of Phase0 and Phase1, and returning the Reset bit's value to 0. After the write operations have been finished, FSYNC is taken high again.

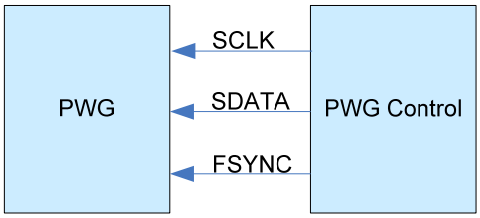


Figure 5-29 Interface between PWG and PWG Control

5.2.5.11 Memory Control and UART Control interface

The interface between the memory control and the UART control was obtained from the *iSensor* design [45].

5.2.5.12 UART Control and UART to USB interface

The UART Control and UART to USB interface were also obtained from the *iSensor* design [45].

5.3 Conclusion

The design of the digital processing circuit was presented and discussed in this chapter. The design of the firmware to be implemented on the FPGA was also discussed. Each element of the digital processing circuit was reviewed together with the firmware design, consisting of a detailed description of the algorithms and interfaces used in the design. The design of the final sensor driver is presented and discussed in chapter 6.

Chapter
6
Final sensor driver design

This chapter discusses the final implementation of the sensor driver, and the requirements for the final sensor system. The changes made to the analogue design after evaluation of the sensor driver test circuit are discussed, as well as the process of fitting the analogue and digital designs together to form the final sensor driver design. The conceptual and final PCB layout designs, as well as issues concerning it, are also described in detail.

6.1 AMB system implementation

The final implementation of the sensor driver system will be in a complete 5-axis AMB system. A 5-axis AMB system consists of two x-, two y- and one z-axis, therefore having 5 degrees of freedom. The sensor driver system for a complete AMB system must therefore consist of two radial- and one axial sensor. As discussed earlier, each radial sensor senses in both the x- and y-axis. The axial sensor senses in only the z-axis. The sensor driver system will however only consist of two radial sensors, since the axial position can be derived from the two radial sensors' position signals. Each sensor requires its own power supply circuit, excitation circuit and signal conditioning circuits. Only one FPGA will be used for all three sensors, and will communicate all the position signals to an external main controller. Figure 6-1 illustrates the concept of the complete sensor driver system.

6.2 Final sensor driver requirements

For the final sensor driver to excite and condition two radial sensors, the main components and circuits required are the following:

- Two isolated analogue power supplies
- An isolated digital power supply
- Two excitation circuits

- Eight signal conditioning circuits
- Four dual ADCs
- One FPGA
- One 1Mx16 CMOS Static RAM module
- One USB to UART bridge
- One Flash in-system programmable PROM
- Two RS-485 transceivers

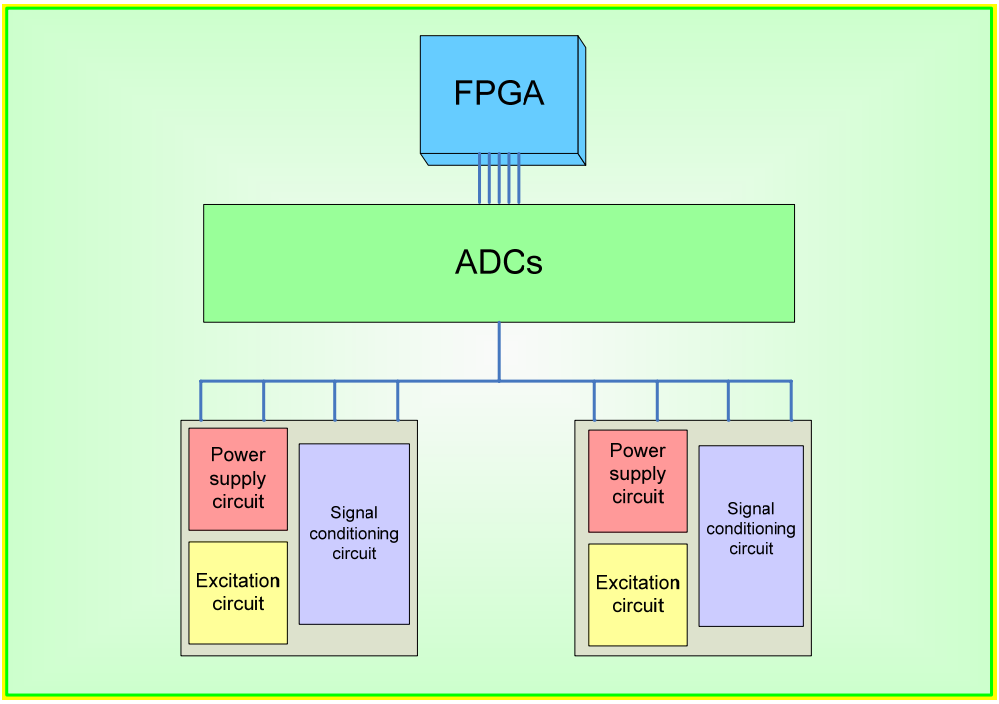


Figure 6-1 Complete sensor driver system for a 5-axis AMB

The final sensor driver circuit also have the following requirements:

- ESD protection on ADC inputs
- Digital buffering on high speed, long distance digital signal lines
- Adequate decoupling of all devices
- JTAG programming
- LEDs to indicate that the power supplies are functioning correctly and to indicate certain processes taking place on the FPGA
- An optically isolated SYNC signal to synchronize communication
- ESD protection on all communication lines, including USB

Figure 6-2 illustrates the system diagram of the final sensor driver system.

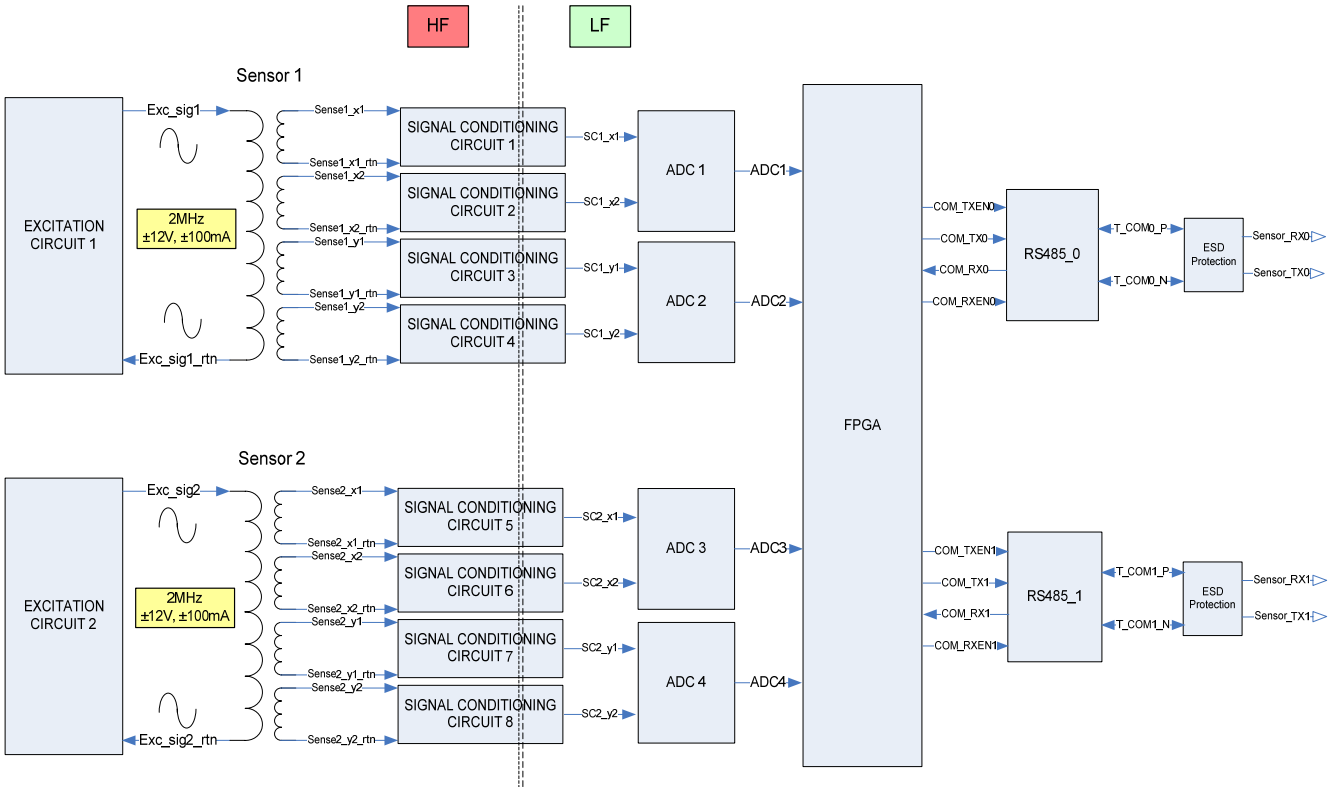


Figure 6-2 Final sensor driver system diagram

The high frequency section of the sensor driver includes the excitation circuits and signal conditioning circuits up to the demodulator output, from where the low frequency section starts. It is important to separate the high frequency and low frequency sections in the design of the sensor driver, or else interference may occur. This interference may lead to a poorer sensor accuracy and measuring resolution due to an inferior signal-to-noise-ratio.

6.3 Modifications to analogue design

After building and testing the sensor driver test circuit, it became apparent that there was room for improvement with regards to the analogue design. Modifications were therefore made to the original analogue design as described in Chapter 4. These modifications will now be discussed.

6.3.1 Analogue power supply

The most essential change to the analogue circuit design was the modifications to the analogue power supply design. The LT1931 -15 V inverting DC-DC converter was found to exceed its specified operating temperature due to the power demand of the analogue circuit when used without a heat-sink. The insufficient heat dissipation of the device led to a increased power dissipation in the device, nearing the device's rated power and operating temperature. Due to the device's current limit feature, the circuit could not be operated for extended time periods as the power would switch off when the current became greater than 1.2 A. As the analogue circuit was not even half of the final sensor driver circuit, it became apparent that the power rating of the LT1931 was not sufficient for the device to be used in the final sensor driver analogue design. Another modification to the original power supply design is the addition of a LC-filter at the 24 V input in order to prevent any noise from the circuit affecting the +24 V power bus, and vice versa. A different analogue power supply design was therefore chosen, and will now be described.

6.3.1.1 Requirement specifications for analogue power supply

The requirement specifications of the power supply circuit remains the same as that given in Chapter 4, but is presented again. The power supply circuit is required to provide the following voltages to the different parts of the sensor driver circuit:

- ±15 V output voltage (analogue)
- ±5 V output voltage (analogue)
- +5 V output voltage (digital)
- +24 V input voltage
- Balanced output
- Regulated output
- ±1.5% output accuracy
- >1.2 A output current
- ±0.015%/°C temperature stability

6.3.1.2 Conceptual circuit design for analogue power supply

The design of the analogue power supply circuit for the final sensor driver consists of two DC-DC converters and two linear voltage regulators. The DC-DC converters receive the supplied input voltage of 24 V DC, and provide as output +15 V and -15 V respectively. This forms the

±15 V to all devices requiring ±15V dual supply. The linear regulators receive the +15 V and -15 V respectively and supplies +5 V and -5 V correspondingly as outputs. Figure 6-3 illustrates the functional diagram of the analogue power supply circuit.

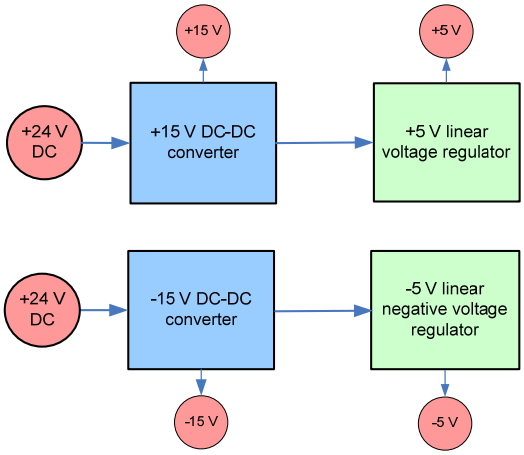


Figure 6-3 Analogue power supply functional diagram

As already mentioned in Chapter 4, the performance parameters of each dual supply consists of only the performance parameters of the positive and negative supply which make up that specific dual supply. In other words, the preceding supplies do not influence the performance of the subsequent supplies.

6.3.1.3 Detail circuit design of analogue power supply

The following components were chosen for the design:

- **+15 V DC/DC Converter:**
  - **THN15-2413** 15 V 15 W high performance DC/DC converter [47]
- **+5 V linear LDO regulator:**
  - **TL750M05** Low-dropout voltage regulator [24]
- **-15 V DC/DC converter:**
  - **THN15-2413** 15 V 15 W high performance DC/DC converter [47]
- **-5 V linear LDO regulator:**
  - **UA7905** Low-dropout 1.5 A negative linear regulator [48]

The component selection was based on the power dissipation capabilities and output stability of each device. Once again referring back to Chapter 4, an estimate of the power dissipation of the analogue sensor driver circuit can be determined by summing the power dissipation of each

device in the circuit with the power dissipation of the sensor excitation coil. The estimated power dissipation equation was given in (4.2), and is used to calculate the estimated power dissipation of the analogue sensor driver circuit.

$$P_{D(TOTAL)} = 2 \times P_{D(LM7171)} + 10 \times P_{D(LM7372)} + 8 \times P_{D(AD637)} + 2 \times P_{D(AD8099_1)} + 8 \times PDAD80992 + 8 \times PDLT1568 + 8 \times PDAD80993 + 2 \times PDAD9833 + 4 \times \mathrm{PD(AD7367)} + PDcoil$$

$$= (2 \times 495\ \mathrm{mW}) + (10 \times 645\ \mathrm{mW}) + (8 \times 108\ \mathrm{mW}) + (2 \times 450\ \mathrm{mW}) + (8 \times 241\ \mathrm{mW} + 8 \times 125\ \mathrm{mW} + 8 \times 241\ \mathrm{mW} + 2 \times 22.5\ \mathrm{mW} + (4 \times 88.8\ \mathrm{mW}) + 1.36\ \mathrm{W}$$

$$= 15.82\ \mathrm{W}$$

The selected components for the analogue power supply circuit is therefore sufficient to be used in the final sensor driver design, since the power rating of the ±15 V dual supply alone is 30 W. The analogue power supply circuit will therefore be capable of supplying enough power to the whole analogue circuit.

6.3.1.4 Schematic circuit of analogue power supply

The schematic circuit for the analogue power supply circuit design is shown in Figure 6-4.

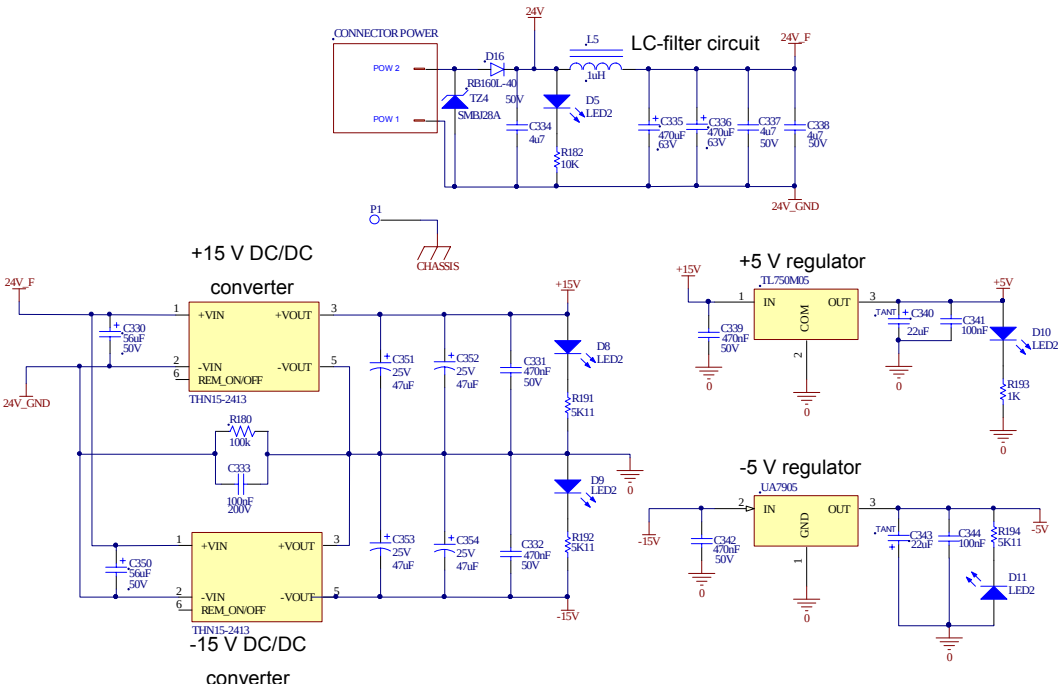


Figure 6-4 Schematic of analogue power supply circuit

6.3.1.5 Performance parameter specifications for analogue power supply

- **Linearity**

The linearity of this design is mainly determined by the output accuracy of the components, namely the two DC/DC converters and the two linear regulators. The linearity of the dual supplies are as follows:

- **±15 V supply:**
  - **+15 V supply**: THN15-2413 DC/DC converter [46]
    - Output accuracy: ±0.2 % @ 25°C
  - **-15 V supply**: THN15-2413 DC/DC converter [47]
    - Output accuracy: ±0.2 % @ 25°C
  - **Total output accuracy ±15 V supply: ±0.2 %**

- **±5 V supply:**
  - **+5 V supply:** TL750M05 linear LDO regulator [24]
    - Output accuracy: ±1 % @ 25°C
  - **-5 V supply:** UA7905 negative linear LDO regulator [48]
    - Output accuracy: ±2 % @ 25°C

∴ **Total output accuracy ±5 V supply: ±1.5 %**

- **Temperature stability**

The temperature stability of the circuit is given by the output accuracy of the regulators and the DC/DC converters measured over their entire operating temperature range of -40°C to +85°C.

- **±15 V supply:**
  - **+15 V supply:** THN15-2413 [46]
    - Temperature coefficient: ±0.02 %/°C = ±200 ppm/°C
    - Output accuracy @ 85°C: ±0.2 % + (±0.02 % x 60°C) = ±1.4 %/°C
  - **-15 V supply:** THN15-2413 [46]
    - Temperature coefficient: ±0.02 %/°C = 200 ppm/°C
    - Output accuracy @ 85°C = ±0.2 % + (±0.02 % x 60°C) = ±1.4 %/°C
  - ±15 V output accuracy over -40°C to +85°C temperature range: ±1.4 %/°C

∴ **±15 V temperature stability =** $\frac{\pm 1.4\% - \pm 0.2\ \%}{85℃ - 25℃} = \pm 0.020\ \%/℃ = \pm 200\ \mathrm{ppm}/℃$

- **±5 V supply:**
  - +5 V supply: TL750M05 linear LDO regulator [24]

- Output accuracy: ±2 %
- Temperature range: -40°C to +125°C
- Temperature coefficient = $\frac{\pm 1\%}{125℃-25℃} = \pm 0.01\ \%/℃$
- Output accuracy (-40°C to +85°C) = $\pm 1\ \% + (\pm 0.01 \times 60℃)$ = ±1.6%

➢ -5 V supply: UA7905 negative linear LDO regulator [48]

- Temperature coefficient: 80 ppm/°C
- Output accuracy = ±2 % + (0.008 % x 60°C) = 2.48 %/°C

➢ ±5 V Total output accuracy over -40°C to +85°C temperature range = ±2.04 %

∴ **±5 V Total temperature stability =** $\frac{\pm 2.04\ \% - \pm 1.5\ \%}{85℃-25℃} = \mathbf{0.009}\ \%/℃ = \mathbf{90\ ppm}/℃$

➢ Performance parameters summary

The summary of the performance parameters of the analogue power supply design is given below:

- **Required performance parameters:**
  - Linearity: $\pm 1.5\ \%$
  - Temperature stability: ± 100 ppm/°C
- **Estimated achievable performance parameters:**
  - Linearity:
    - ±15V: **±0.2 %** << ±1.5 % required
    - ±5V: **±1.5 %** = ±1.5 % required
  - Temperature stability:
    - ±15V: **200 ppm/°C** > 100 ppm/°C
    - ±5V: **91.67 ppm/°C** < 100 ppm/°C

Although the temperature stability of the ±15 V supply is greater than 100 ppm/°C, its linearity is significantly less than the specified ±1.5 %, making it an attractive choice for implementation in the analogue power supply circuit. Another important fact to consider is that the performance of the power supply circuit does not directly influence the performance of any devices in the analogue sensor driver circuit. The temperature stability of the ±15 V supply therefore does not play a significant part in the performance of the rest of the analogue circuit.

6.3.2 PCB sensors

Two new PCB sensors were manufactured for this project, incorporating the sensor driver connectors. The PCBs of the sensors turned out to be 0.8 mm thicker than those used previously [7]. The central hole for the test rotor was also machined to be 0.12 mm smaller than the previous PCB sensor, decreasing the air gap to 380 µm, or ±190 µm on either side of the rotor. The increase in distance between the top and bottom coils resulted in the impedance of the new sensors to differ from the previous sensors. This meant that the specification for the excitation signal also had to be altered. The load resistance of the sensor together with the sensor cables was measured as 141.5083 Ω. Assuming that it is an inductive load, the reactance of the coil equals the measured load resistance, and makes up 95 % of the impedance of the coil. The voltage applied to the excitation circuit during the measurements was ±11.25 V, and the frequency of the applied signal was 2.083 MHz. The excitation current was then calculated as follows:

$$I_{RMS} = \frac{V_{RMS} \times 95\%}{X_{exc}}$$

$$= \frac{7.955\ \text{V} \times 0.95}{141.5083\ \Omega}$$

$$= 53.405\ \text{mA}_{\text{RMS}}$$

$$= \pm 75.526\ \text{mA}$$

The determined reactance of the coil and the frequency of the signal could then be used to determine the inductance of the sensor's excitation coil as follows:

$$X_L = 2\pi f L$$

$$\therefore L = \frac{X_L}{2\pi f}$$

$$= \frac{141.5083\ \Omega}{2 \times \pi \times 2.083\ \text{MHz}}$$

$$= 10.812\ \mu\text{H}$$

6.3.3 Excitation circuit

6.3.3.1 Master clock

In the final sensor driver, the AD9833 programmable waveform generator does not receive its master clock signal from an external crystal oscillator, but from the FPGA. The estimated frequency and temperature stability of the oscillator circuit will therefore be improved.

- **Frequency stability**

Due to the fact that the external crystal was the only contributor to the frequency instability, the frequency stability of the circuit is improved to 100% stable over time.

- **Temperature stability**

The external crystal contributed to frequency instability over temperature, which is eliminated by replacing the external crystal with a clock signal from the FPGA. The oscillator circuit's temperature stability is therefore only determined by the AD9833:

- **AD9833 [27]:**
  - V_{OUT} Temperature coefficient = 200 ppm/°C
  - Operating temperature range: -40°C to +105°C

∴ **Total temperature stability:**

- **Amplitude = 200 ppm/°C**

6.3.3.2 Voltage to current converter circuit

During evaluation of the excitation circuits of the sensor driver, it was observed that the voltage to current converter circuits became unstable when connected with the PCB sensor. Possible explanations are that the impedance of the new PCB sensors with the full-length cables are different to that of the previous PCB sensor, resulting in the voltage to current converter becoming unstable. The output of the voltage to current converter of the test circuit could also be very precisely adjusted, as potentiometers were used. With the final sensor driver circuit, all the potentiometers were replaced with fixed resistors, making it more difficult to acquire the precise gain required. The voltage to current converter design also included only negative feedback, providing only one feedback loop for stability improvement. Although attempts were made to improve the stability by adding capacitors to the negative feedback loop, it was still not enough to obtain a stable output. It was therefore decided to change the design of the voltage to current converter circuit.

The design was changed by replacing the voltage to current converter with a Howland current pump. This design employs both a positive and negative feedback, thereby providing more feedback loops to add capacitors to in order to improve the stability of the output. The circuit schematic as implemented in the voltage to current converter design is shown in Figure 6-5.

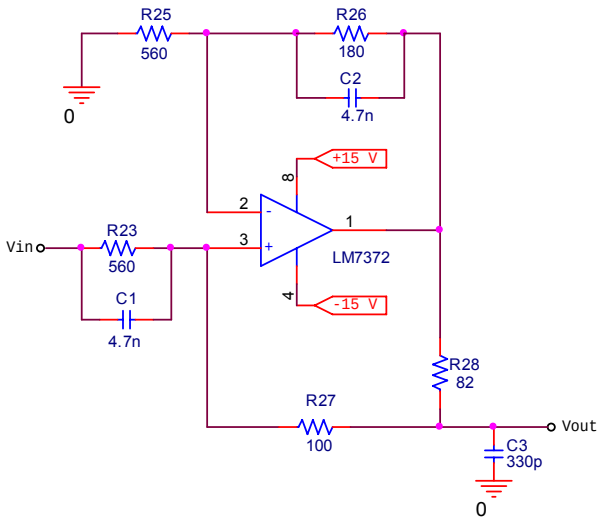


Figure 6-5 Howland current pump circuit schematic

This design was first evaluated on its own, and then implemented on the final sensor driver board. This design produced a stable output signal. The measurements of the excitation circuit's outputs are presented in chapter 7.

6.3.4 ESD protection

Electro-static discharge protection was placed on several vulnerable signal lines, namely the inputs to the ADCs, the RS-485 communication lines and the USB communication lines. On the communication lines, multi-input ESD protection devices were used, while on the inputs to the ADCs, single input ESD protection devices were used. The devices used are the following:

- **ESDA6V1** quad bidirectional transil suppressor for ESD protection [49]
- **SM6T12CA** over-voltage and ESD protection transil diode [50]

6.3.5 Digital buffering

Digital buffering is used in the sensor driver design to buffer high-speed digital signals that may be susceptible to interference from switching devices on the board, like the DC/DC converters, power amplifiers and high frequency clock signals. The signals that are buffered are the MCLK master clock signals from the FPGA to the PWGs. These signals required buffering due to the distance between the FPGA and the excitation circuit.

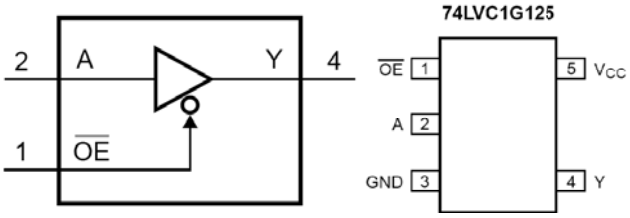


Figure 6-6 Logic symbol and pin configuration of 74LVC1G125 digital buffer

6.3.6 Digital isolators

High speed data transmission lines require digital isolation in order to protect both systems and users from potentially hazardous voltages. The digital isolation protects against electromagnetic fields, surges, fast transient, and high noise floors, and many other occurrences that might cause low-voltage devices to be destroyed or damaged. In the sensor driver circuit, digital isolators are used on the inputs of the PWG to protect both the FPGA and PWG, and keep the analogue and digital circuits of the sensor driver isolated from each other. The digital isolator used is the ADμM3400 quad-channel digital isolator with enhanced system-level ESD reliability [51].

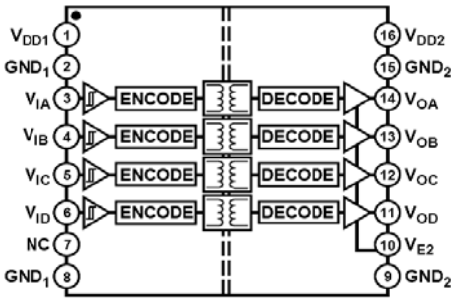


Figure 6-7 Functional block diagram of the ADuM3400 digital isolator

6.4 Combining analogue and digital designs

After the design of both the analogue and digital circuits of the final sensor driver had been completed, the two designs were merged into a single design. In order to prevent digital interference from coupling in on the analogue signals, and vice versa, the two circuits must be kept separate and isolated from each other. The only analogue devices directly connected to the digital circuit are the ADCs and the PWGs. In order to keep the analogue and digital circuits isolated, digital isolation devices are placed at the ADCs' and PWGs' input- and output signals.

6.5 PCB layout

6.5.1 Conceptual layout

The conceptual layout for the final sensor driver board was done in Microsoft Visio©. The conceptual layout is not yet a component-level layout, but a circuit-level layout, illustrating the sections within which certain groups of components will be placed. As the sensor driver board is intended to be used in an AMB system, it was decided to make the PC board a double-euro (6U) size, and standardize it for mounting in a rack.

Figure 6-8 shows the conceptual layout of the sensor driver. The sensor driver board is a ten-layer PCB to accommodate all the different signal, ground and power circuit requirements, as well as the PCB manufacturing capabilities of local PCB manufacturers. The board is meant to be symmetrical about the FPGA, with the analogue power supply circuits and excitation circuits at the two opposite ends of the PC board. The signal conditioning circuits are located in the centre of the board, and are separated into high-frequency (HF) and low-frequency (LF) sections, each of which will be routed on different layers. Each differential pair of sensor signals are also isolated from the other differential signal pairs as to prevent possible interference. Incisions in the copper plane are made on the ground and power planes to guide the return current flowing in the planes to flow only through certain appointed areas.

The placement of the ADCs is one of the most important factors with regards to the layout of the board. The ADCs are placed back-to-back on the analogue- and digital ground partition. The analogue ground (AGND) and digital ground (DGND) are only connected in one point, namely in the centre between the ADCs. This is done due to the fact that according to the ADC's datasheet, the analogue-to-digital ground connection must be made as close as possible to the

AGND and DGND pins of the ADC device. Since there are four ADCs, it was decided to place the ADCs back-to-back and make the AGND to DGND connection in the middle between them. The distance between the ground connection and the ground pins of the ADCs are therefore all more or less the same.

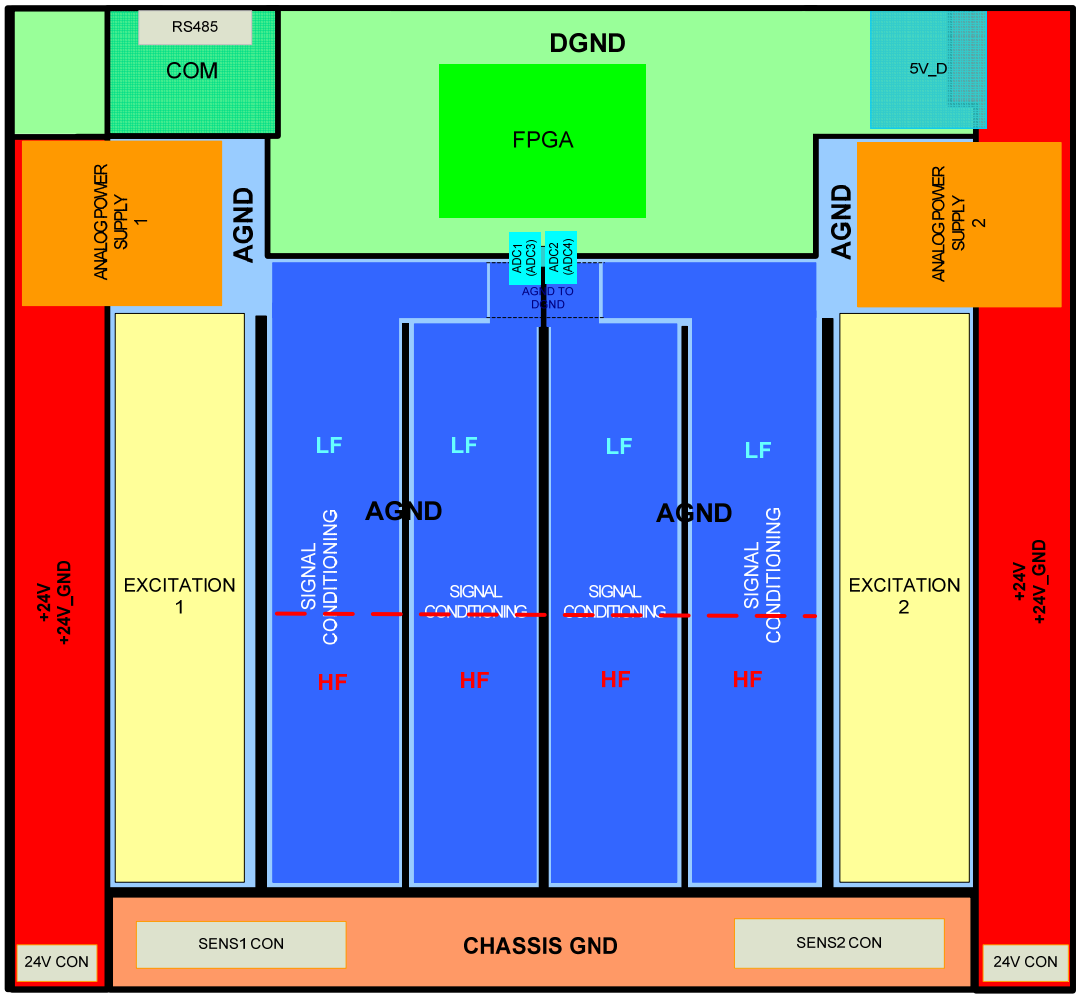


Figure 6-8 Conceptual layout of final sensor driver board

The power connectors and the sensor connectors are located at the bottom side of the board, while the communication connectors (RS-485, JTAG, USB) are situated at the top side of the board. This again separates the analogue and digital signals of the board. This also corresponds to the standardization of the board to double-euro standards.

Component placement is done on both the top- and bottom layers of the board. The top layer of the board contains most of the low-frequency signals, along with tracks from components to vias. Some digital signals and power supply signals are also present on the digital side of the board.

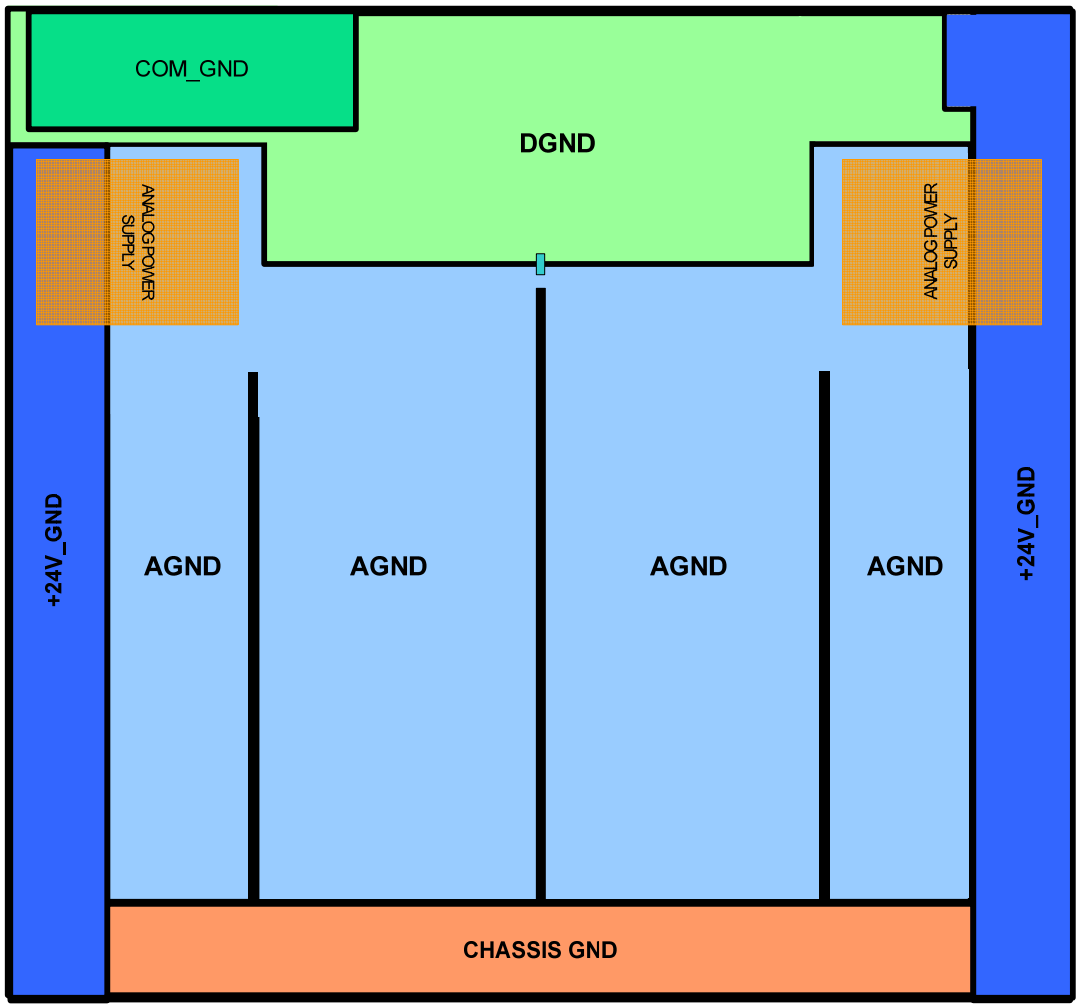


Figure 6-9 Conceptual layout of the ground layers of the sensor driver board

The 2nd, 4th, 7th, and 9th layers of the board are ground layers, containing the chassis ground (CHASSIS GND), analogue ground (AGND), digital ground (DGND), communications ground (COM_GND) and the +24 V supply voltage ground (+24V_GND). The conceptual layout for the ground layers is shown in Figure 6-9.

The 3rd layer of the board contains the high-frequency (HF) signals, as well as digital signals in the digital section. The high-frequency and low-frequency signals are routed on different layers in order to prevent possible interference between the signals and minimize noise.

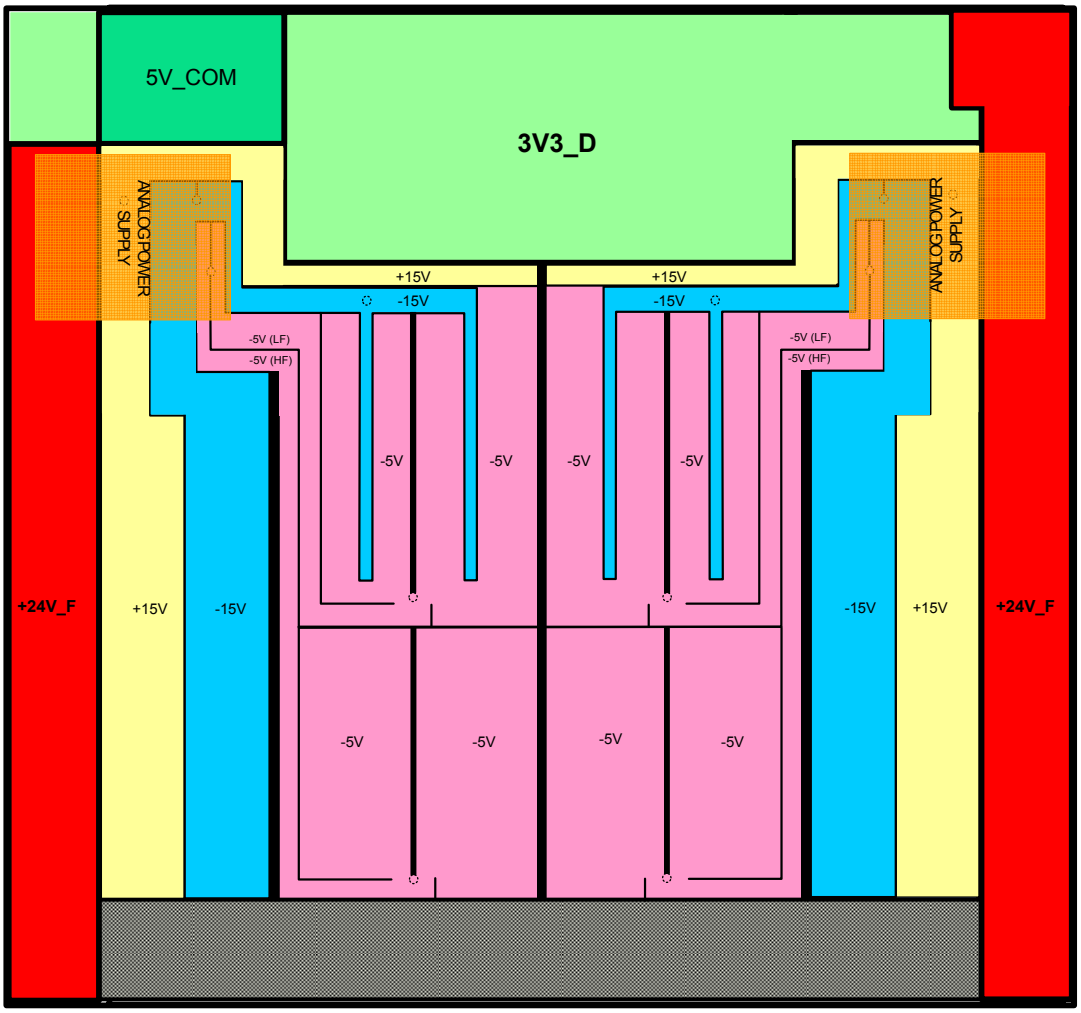


Figure 6-10 First power layer of the conceptual layout

The 5th layer of the board is the first power layer, and is shown in Figure 6-10. This layer contains separate power planes for the following:

- filtered +24 V supply voltage (+24V_F),
- +15 V for the excitation circuits and ADCs,
- -15 V for the excitation circuits and signal conditioning circuits,
- -5 V for the high-frequency signal conditioning circuits, and
- -5 V for the low-frequency signal conditioning circuits.

On the digital side it contains separate power planes for

- 3V3_D and
- communications power (5V_COM).

All of the power planes either originate from a star-point, or are guided to form a star-point connection which have adequate decoupling capacitors.

The 6th layer of the board is the second and last power layer and is shown in Figure 6-11. This layer contains the following separate power planes:

- filtered +24 V supply voltage (+24V_F),
- -5 V for the excitation circuits,
- +5 V for the excitation circuits, HF signal conditioning circuits and LF signal conditioning circuits,
- +15 V for the signal conditioning circuits, and
- -15 V for the ADCs

On the digital side it contains the following separate power planes:

- 5V_D,
- 1V2_D,
- 1V8_D, and
- 5V_COM.

The 8th layer contains the rest of the high-frequency signals of the signal conditioning circuits and excitation circuits, as well as digital signals in the digital section of the board.

The bottom layer contains the rest of the low-frequency signals of the signal conditioning circuits. The low frequency signals are therefore kept on the outsides of the board, with ground planes directly beneath the top layer and above the bottom layer shielding the low-frequency signals from the high-frequency signals. By locating the high-frequency signals on the centre layers of the board, surrounded by ground- and power planes, these noise susceptible signals are also shielded from external interference and from transmitting interference to the outside world. The complete conceptual layout is provided in Appendix B.

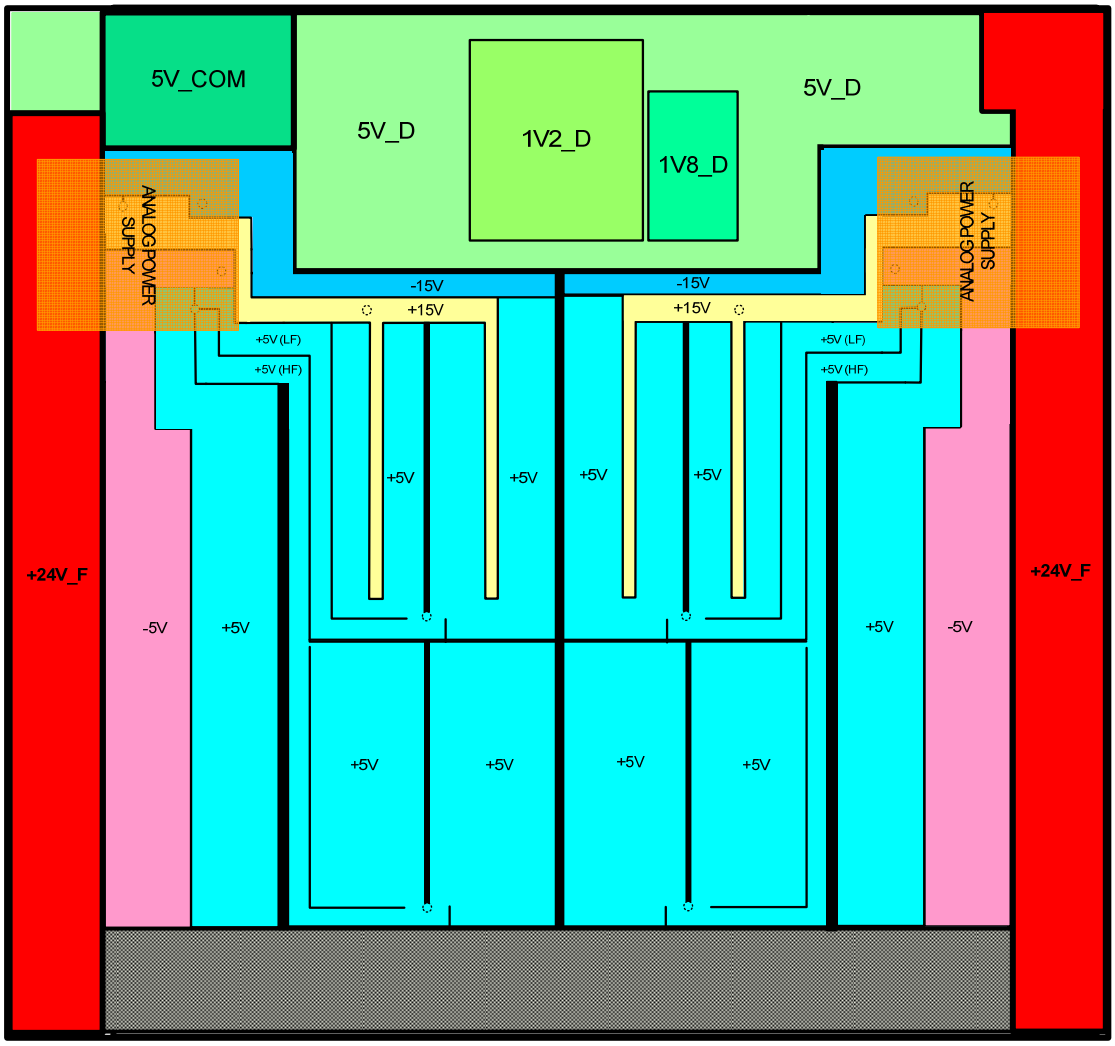


Figure 6-11 Second power layer of conceptual layout

6.5.2 Final layout

After the conceptual layout has been finalized, the physical PCB layout of the sensor driver board can commence. The PCB layout is done in Altium Designer©. The final layout will now be discussed in detail. The proposed stack-up of the board is shown in Figure 6-12, and is based on information and layout suggestions given by 0.

1) LF signal layer
2) GND layer
3) HF signal layer
4) GND layer
5) PWR layer 1
6) PWR layer 2
7) GND layer
8) HF signal layer
9) GND layer
10) LF signal layer

Figure 6-12 Stack-up of PCB

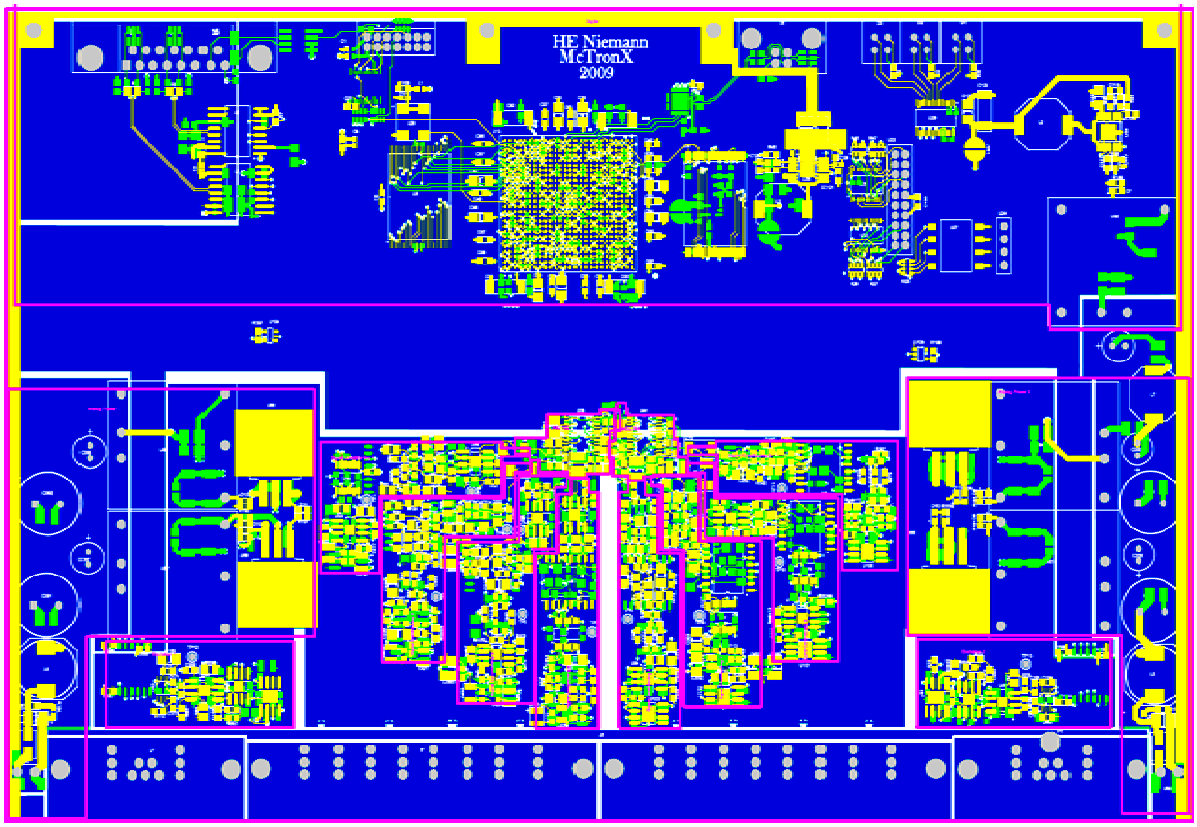


Figure 6-13 Overview of final PCB layout

The final PCB layout in general is shown in Figure 6-13. This overview is not of just one layer, but of the top layer, bottom layer and a ground layer combined to give a clearer picture of the complete layout of the board. The areas of the different sub-circuits are also shown. The

analogue power supply circuits are located at the sides of the board, with the excitation circuits just below them. The signal conditioning circuits are located in the centre of the board, radiating outwards from the ADCs. The digital circuit is located at the top of the board, with the digital power supply circuit at the top right and the communication circuit in the top left corner. The sensor connectors are located at the bottom of the board, and the communications connectors at the top, as designed in the conceptual layout. The component placement on the top- and bottom layers is shown in Figure 6-14 and Figure 6-15.

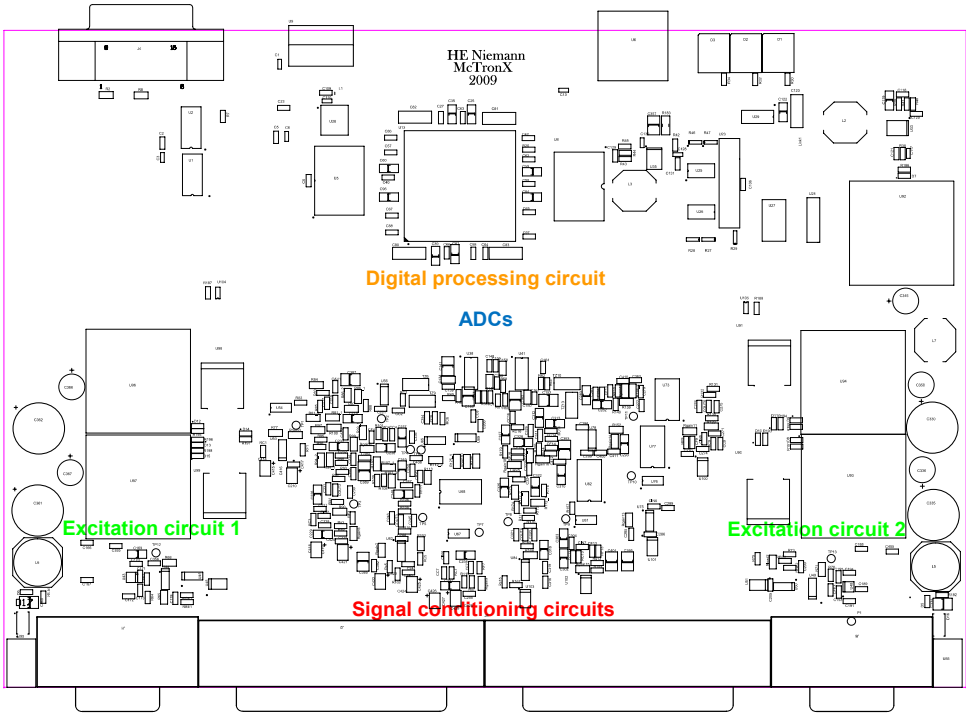


Figure 6-14 Top layer component placement

The sensor driver board layers can be grouped together as follows according to type:

- LF signal layers
- HF signal layers
- Ground layers
- Power layers

Each of these layers will be shown and discussed.

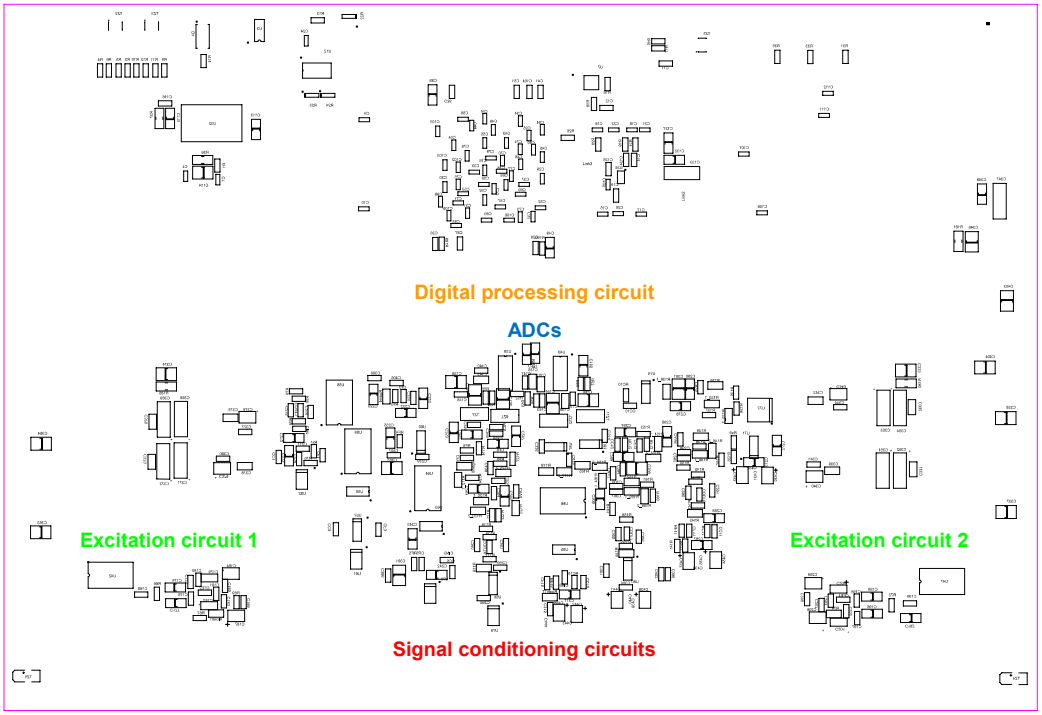


Figure 6-15 Bottom layer component placement

6.5.2.1 LF signal layers

The LF signal layers are located on the top-and bottom layers of the board. The track length of all other signals of the analogue circuits present on these layers are kept as short as possible in order to minimize possible high-frequency interference. In the digital section, all the signal layers of the board are utilized for routing of the digital signals. The routing of the power supplies are also done on the top- and bottom layers in order to minimize track length of high current and high power tracks. Figure 6-16 shows the layout of the LF signal layers.

6.5.2.2 HF signal layers

The HF signal layers are located on the 3rd and 8th layers of the board, meaning that they are surrounded by ground- and power layers to minimize the length of current return paths and shield the signals from any interference and external noise. The signals between the FPGA and the ADCs and PWGs are also located on the HF signal layers. Figure 6-17 shows the layout of the HF signal layers.

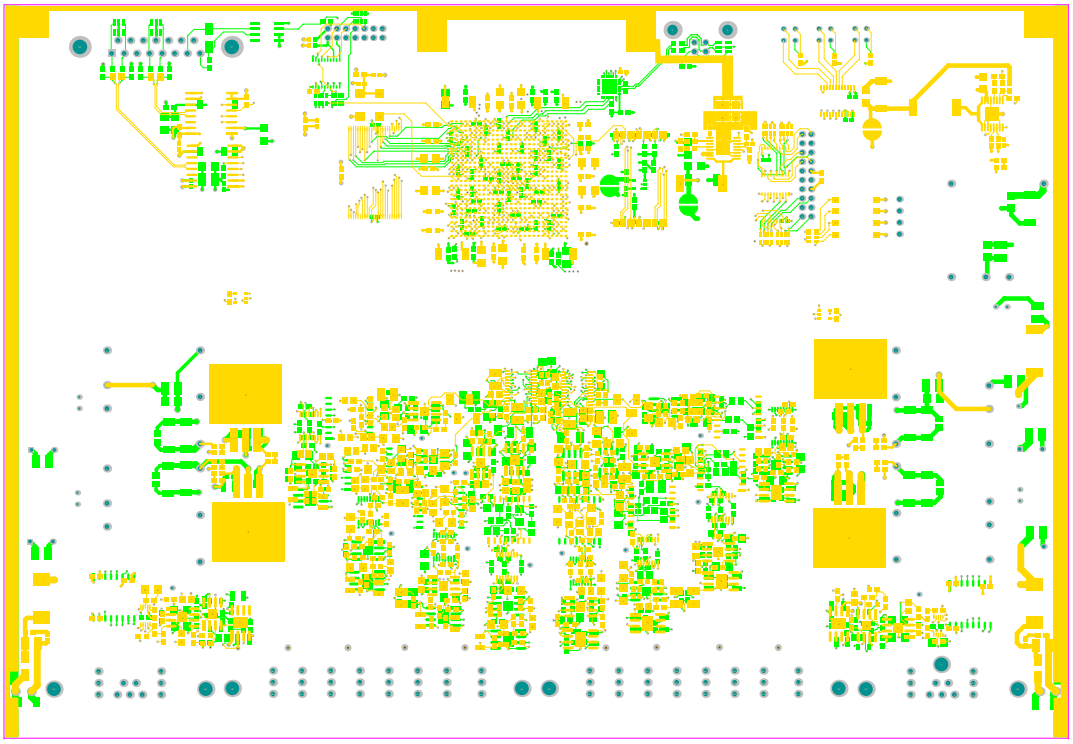


Figure 6-16 LF signal layers on top- and bottom layers

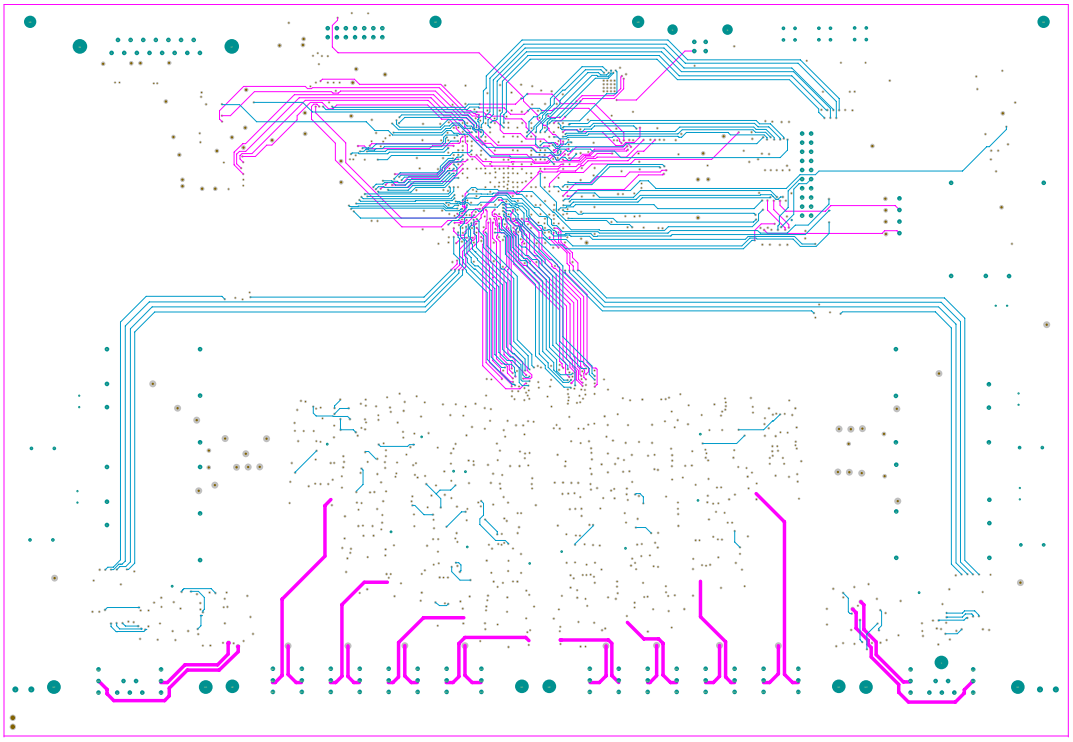


Figure 6-17 HF signal layers

6.5.2.3 Ground layers

There are four ground layers in the sensor driver board, located on layers 2, 4, 7 and 9. The analogue ground planes of the two sensors form a star point-connection just below the ADCs, and the analogue- and digital ground planes also form a star point-connection in the centre of the ADCs. The ground planes of the +24 V supply voltage are kept isolated from the rest of the ground planes, and the communications ground plane is isolated from the digital ground plane and form a floating ground. The ground layers consist of separate ground planes for AGND, DGND, CHASSIS_GND, +24V_GND and COM_GND, as proposed in the conceptual design. Figure 6-18 shows the layout of the ground layers.

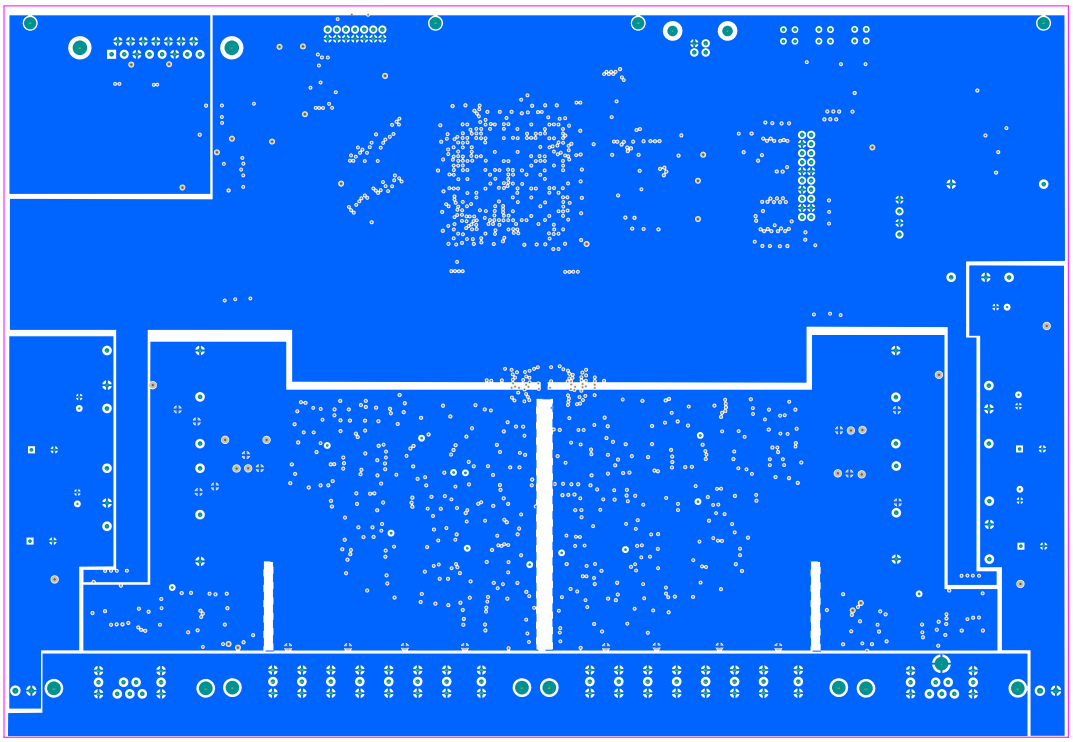


Figure 6-18 Ground layer

6.5.2.4 Power layers

The sensor driver board has two power layers located on the 5th and 6th layers. Unlike the ground layers that are all identical, the two power layers differ slightly from each other. The power planes for the signal conditioning circuits are somewhat different, but are still kept as similar in form as possible. The power planes of the analogue power supply circuits are identical, as well as the power plane for the RS-485 communication. The two power layers are shown in Figure 6-19 and Figure 6-20, followed by a discussion of each.

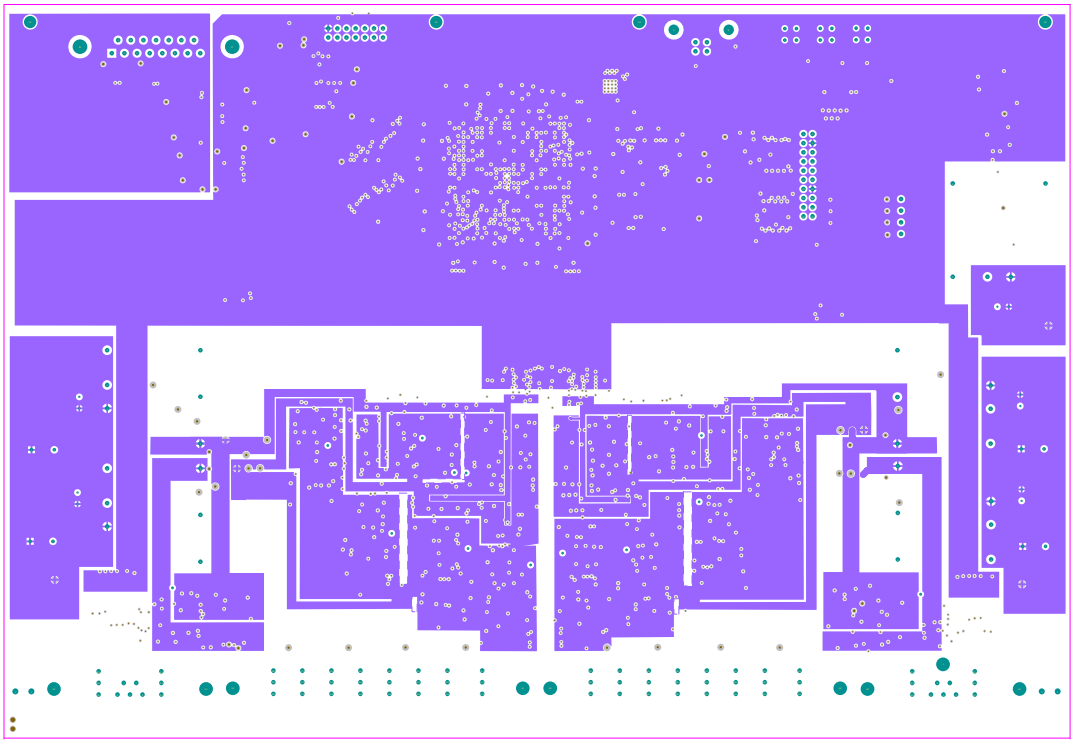


Figure 6-19 First power layer

Figure 6-19 shows the layout for the first power layer. The circuit for sensor 1 is located on the left half, and the circuit for sensor 2 on the right. This power layer consists of separate power planes for the following:

- +24V_F
- +15 V for both excitation circuits
- +15 V for signal conditioning circuits and ADCs of sensor 1
- -15 V for both excitation circuits
- -15 V for signal conditioning circuits and ADCs of sensor 2
- -5 V for the HF and LF signal conditioning circuits
- 3V3_D
- 5V_COM

The layout for the second power layer is shown in Figure 6-20. This power layer consists of separate power planes for the following:

- +24V_F
- +5 V for both excitation circuits

- +5 V for HF and LF signal conditioning circuits and ADCs of both sensors
- -5 V for both excitation circuits
- -15 V for signal conditioning circuits and ADCs of sensor 1
- +15 V for signal conditioning circuits and ADCs of sensor 2
- 5V_D
- 1V8_D
- 1V2_D
- 5V_COM

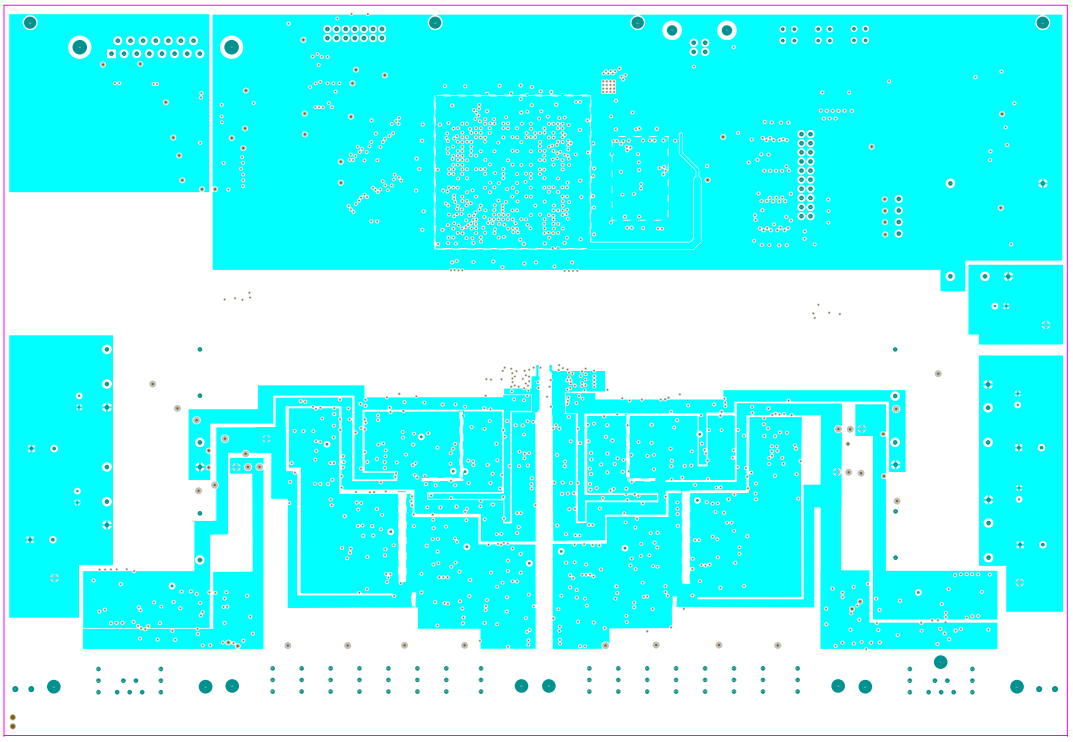


Figure 6-20 Second power layer

6.6 Final sensor driver board

Figures 6-21 to 6-25 are photographs of the final sensor driver board. Figure 6-21 shows the top layer of the sensor driver PCB, while Figure 6-22 shows the bottom layer. Figure 6-23 shows a close-up of one of the excitation circuits, where the alteration to the voltage to current converter design can clearly be seen. Figure 6-24 shows the signal conditioning circuits of the sensor driver along with the ADCs, and Figure 6-25 shows the digital processing circuit.

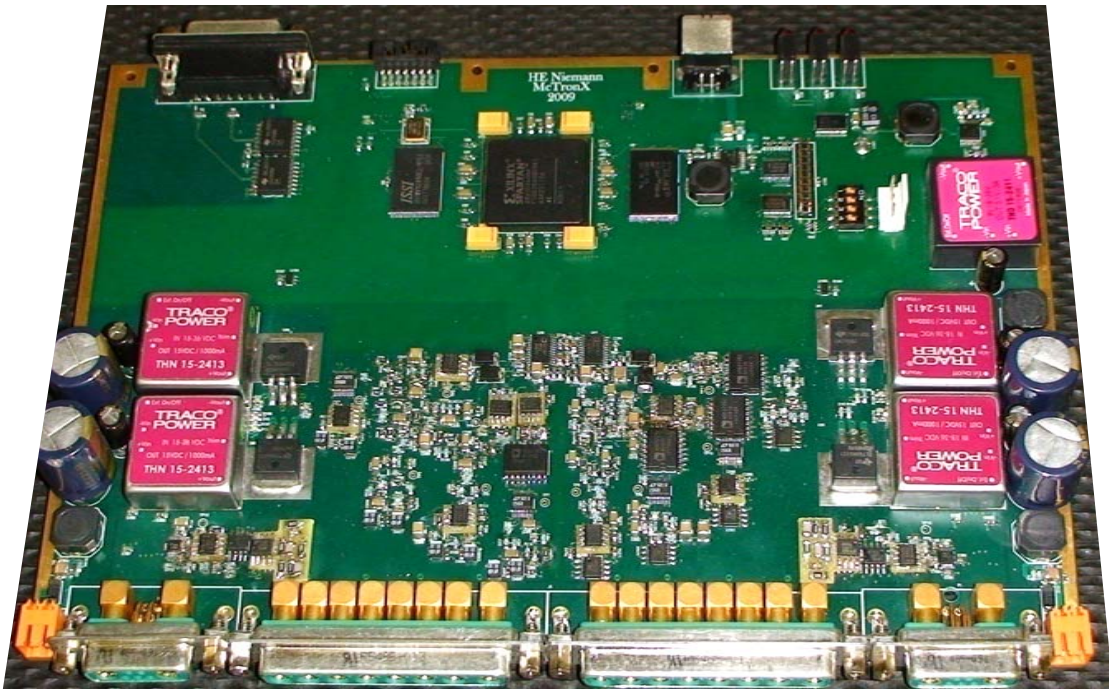


Figure 6-21 Top layer of final sensor driver PCB

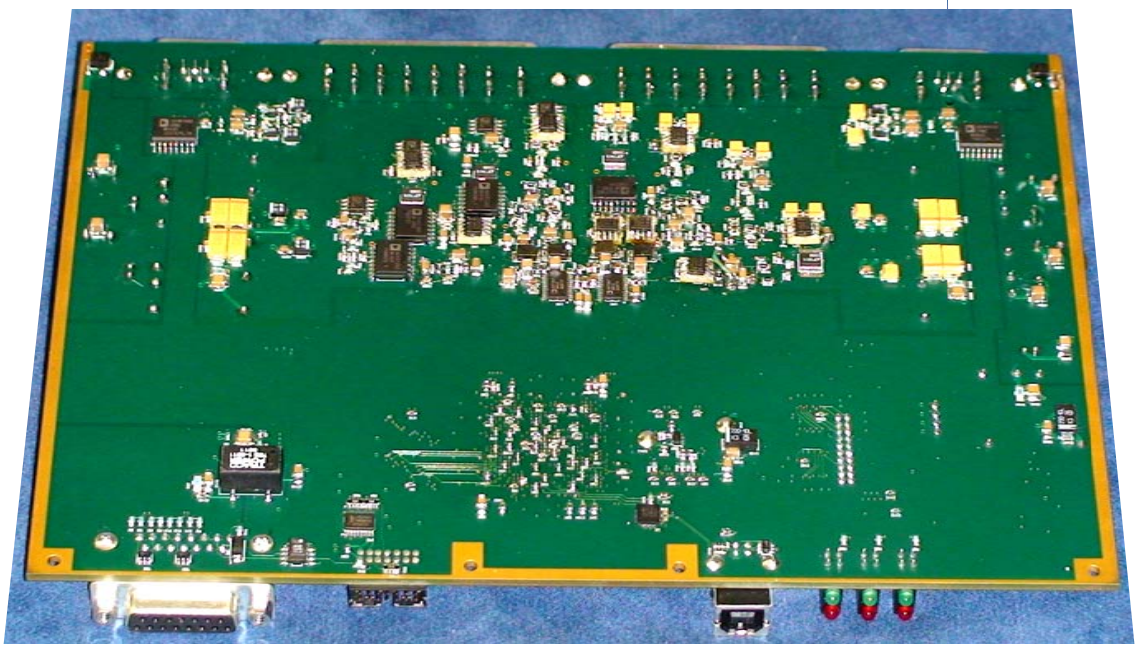


Figure 6-22 Bottom layer of final sensor driver PCB

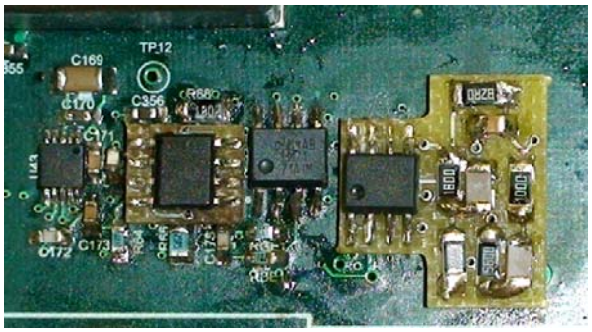


Figure 6-23 Excitation circuit

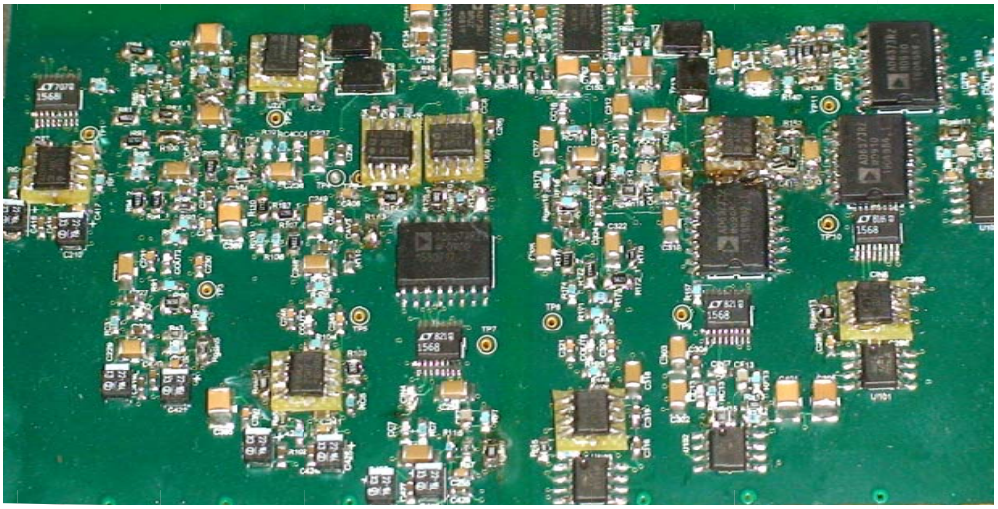


Figure 6-24 Signal conditioning circuits

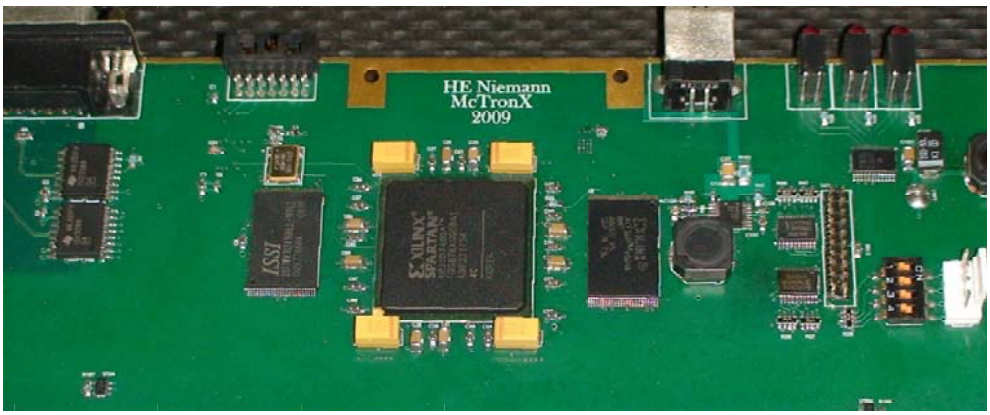


Figure 6-25 Digital processing circuit

6.7 Conclusion

The final sensor driver is the result of all the planning and design of the sensor driver system, and the end goal of this Master's project. The entire design process together with the PCB layout were the main aspects of this project, and were successfully completed in order to produce the final sensor driver board. The results and measurements of the final sensor driver board are given in chapter 7.

Chapter 7

Evaluation

In this chapter the results obtained from all the circuits of the sensor driver that were constructed and tested are provided and discussed. This includes the measurements taken from the oscillator test circuit, the sensor driver test circuit and the final sensor driver circuit. These measurements will be used to verify the design of the different circuits with regards to its set specifications. The measurements of the final sensor driver in particular will be used to validate the sensor driver system against its set of requirement specifications.

7.1 Oscillator circuit

7.1.1 Test 1: Amplitude stability

The amplitude stability of the oscillator circuit was evaluated over a time period of 24 hours at room temperature. The output signal was recorded on a digital oscilloscope at specific time intervals, namely:

1. During start-up (t=0)
2. After 5 minutes (t=5)
3. After 10 minutes (t=10)
4. After 15 minutes (t=15)
5. After 30 minutes (t=30)
6. After 1 hour (t=60)
7. After 2 hours (t=120)
8. After 18 hours (t=1080)
9. After 24 hours (t=1440)

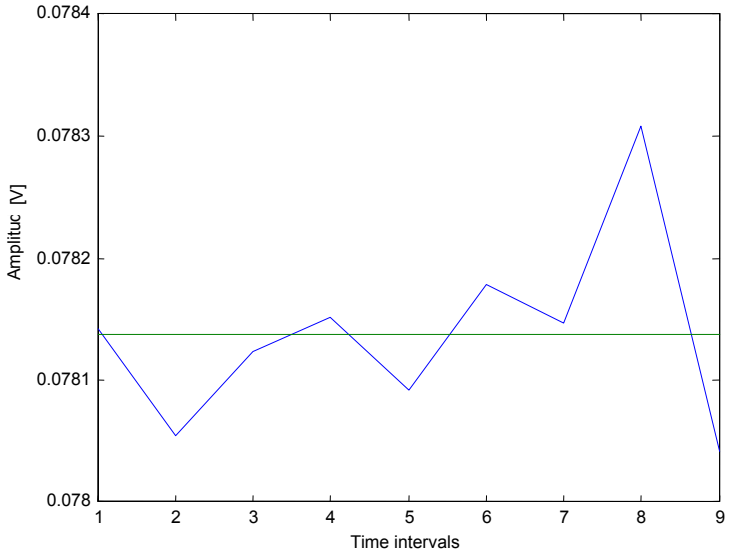


Figure 7-1 Recorded amplitude over time

In each case the FFT of the recorded signal was taken, and the amplitude of the FFT used to evaluate the linearity and amplitude stability of the design.

Figure 7-1 shows the amplitude variation over time. The mean amplitude was calculated as 78.1374 mV, and is also plotted in Figure 7-1. The total amplitude variation was calculated as ±0.1709 %

∴ **Total amplitude stability: ±0.1709 %**

7.1.2 Test 2: Frequency stability

The frequency stability of the designed oscillator circuit was also determined by taking the FFT of the recorded signals. The FFT shows the frequency components of a signal, meaning that for a frequency stable design, the amplitude of all other frequencies need to be significantly less than that of the excitation frequency. The frequency used in this design was 2.083 MHz. The FFT plots of the first and last recorded signals are shown in Figure 7-2 and Figure 7-3.

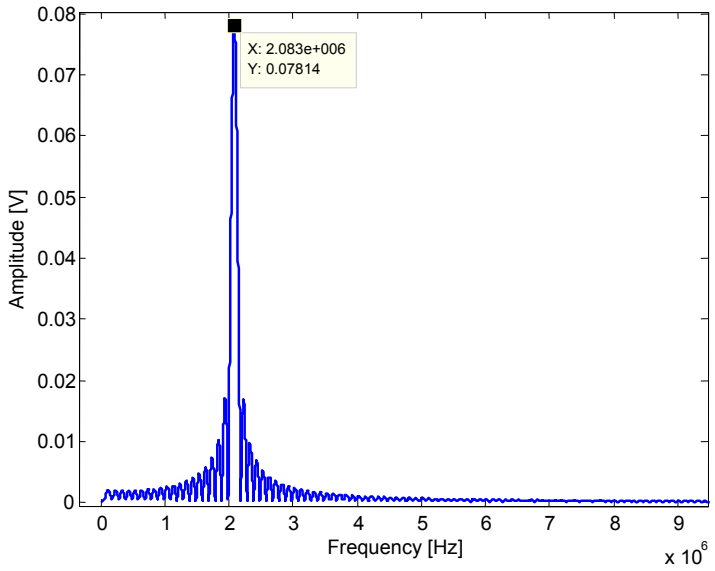


Figure 7-2 FFT plot of output during start-up

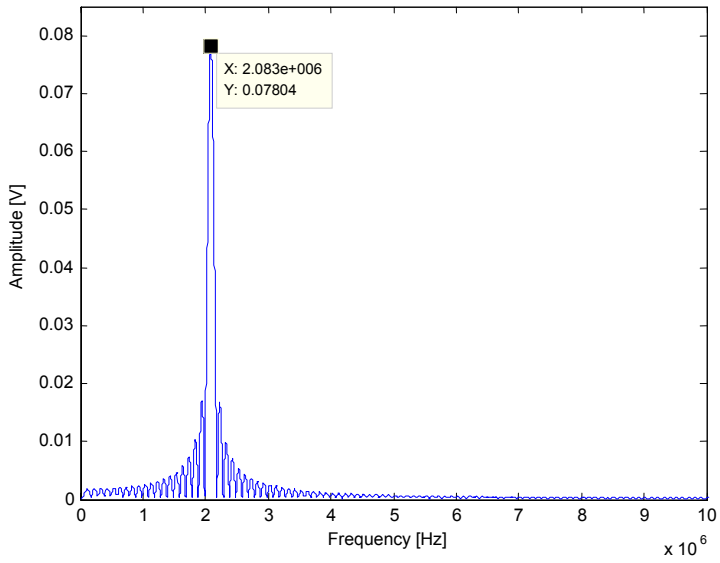


Figure 7-3 FFT plot of output after 24 hours

The recorded signals showed no frequency variation, and no other frequency components near the operating frequency, making it extremely frequency stable at room temperature. The recorded output frequency over time is shown in Figure 7-4. Due to the fact that the oscillator signal is at a high frequency and the sample rate of the digital oscilloscope is limited, the oscilloscope cannot obtain a finer frequency resolution than 1kHz for the oscillator signal.

Therefore, if there are any frequency deviations over temperature, it is less than 0.048 % or 480 ppm.

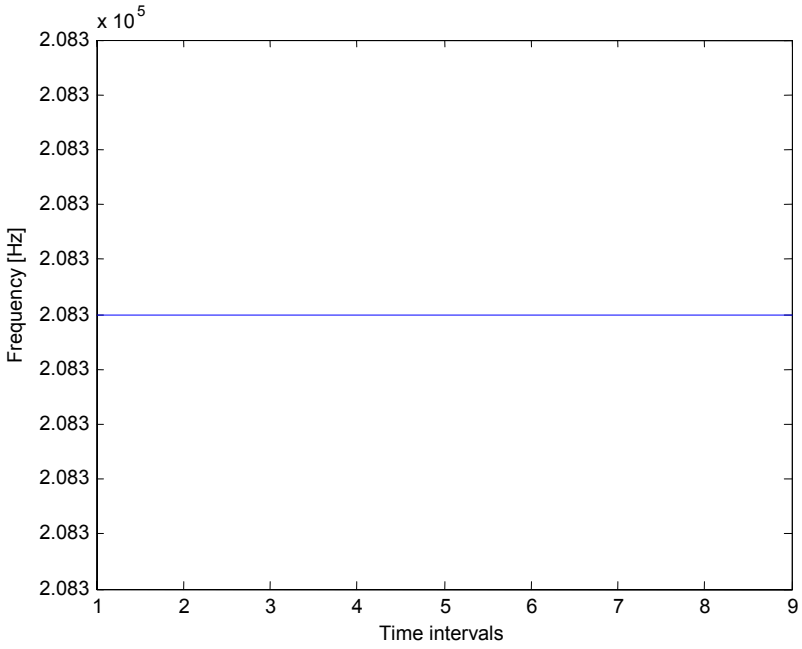


Figure 7-4 Recorded frequency output over time

7.1.3 Test 3: Temperature stability

The temperature stability of the designs consists of both the amplitude and frequency stability of the output signal at different temperatures. The temperature stability of each design will be tested by exposing the circuit to a heating element (e.g. a light bulb) while in operation. The board temperature will be read continuously using an infrared temperature sensor. The output signals will be recorded at set board temperature levels on a digital oscilloscope, namely at:

- Initial room temperature
- 30°C
- 40°C
- 50°C
- 60°C
- 70°C
- 80°C

The board temperature will be monitored on a part of the PCB without copper tracks or planes connected to the circuit, and will therefore not be influenced by power dissipation of the

components, but only by the heating element. The circuit will be on for 5 minutes before the heating element is switched on in order to eliminate the effect of any start-up irregularities in the readings.

- **Amplitude stability**

The temperature stability of the oscillator circuit was evaluated for both amplitude and frequency. The circuit was heated, and the output signal recorded on a digital oscilloscope at the set board temperature levels mentioned before.

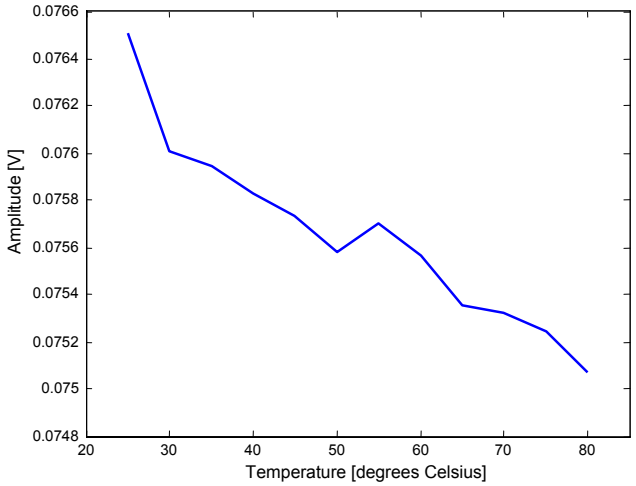


Figure 7-5 Recorded amplitude over temperature

Figure 7-5 shows the recorded amplitude over temperature. As can be seen from the figure, the signal's amplitude decreases as the temperature increases. Figure 7-6 shows the deviation of the amplitude with an increase in temperature.

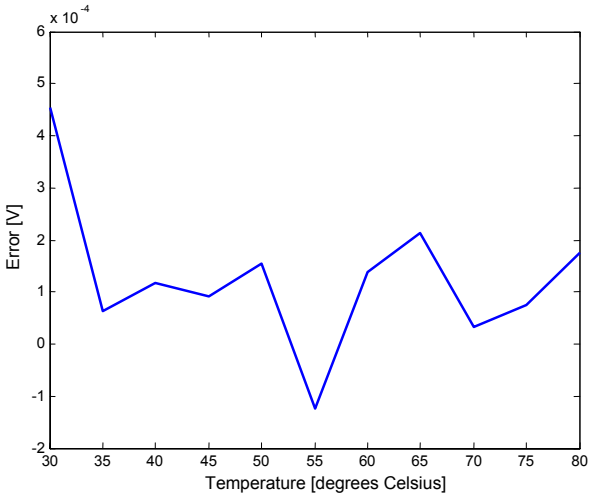


Figure 7-6 Amplitude error over temperature

By taking the average of the amplitude error, the average error per degree Celsius was determined as 0.033%/°C or 330.612 ppm/°C. The requirement specification set for the amplitude temperature stability of the oscillator circuit was 200 ppm/°C. Although the measured amplitude temperature stability is worse than the specification, the error is still negligibly small.

A modulated frequency on the signal was observed on the oscilloscope. It manifested as a slight 'peak' and 'flat' on the peak of the oscillator signal. In the FFTs of the oscillator signal over temperature, no other significant frequencies were noted. The modulated frequency therefore appeared to be at a low frequency which could not be measured with an FFT. In order to attempt to identify the modulated frequency, the FFT of the signal was determined for five 'peak' and 'flat' signals. Figure 7-7 shows an example of 'peak' and 'flat' signals.

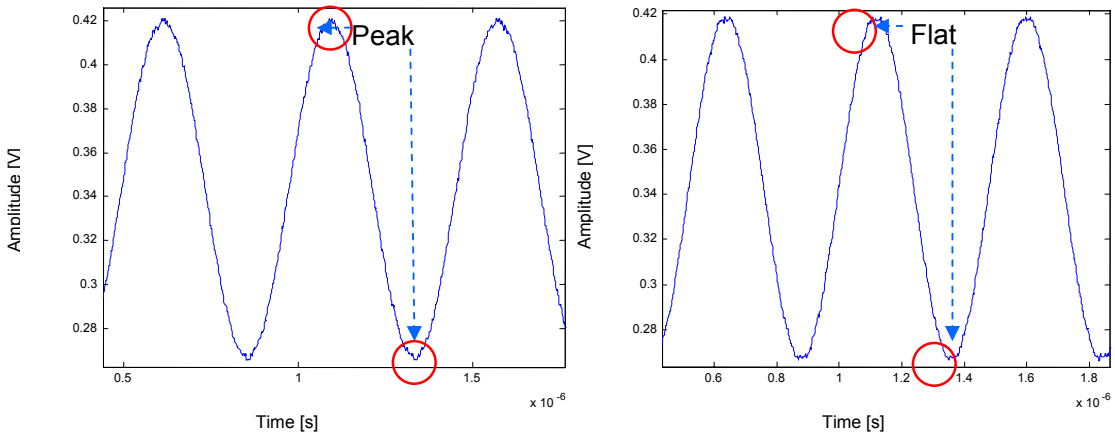


Figure 7-7 'Peak' (left) and 'flat' (right) signals

The average difference in amplitude of the signals was determined as 0.1197223 %. This corresponds to 90.5945 µV with regards to the average oscillator amplitude. The end-effect that this modulated frequency will have on the sensor driver system was evaluated by calculating the corresponding voltage-error it will produce in the sensor. The excitation circuit is excited with ±12 V, which equals 24 $V_{p\text{-}p}$. This converts to a maximum sensor output voltage difference of 100 mV for the entire measuring range (V_{max} – V_{min}), for V_{max}=0.52 V and V_{min}=0.42 V. The ratio between input and output voltage of the sensor is therefore $\frac{1}{240}$. The voltage gain of the voltage-to-current converter circuit is 150 V/V. The corresponding voltage-error of the modulated signal is therefore:

$$V_{Error} = 90.5945\ \mu V \times 150\ V/V \times \frac{1}{240} \tag{7.1}$$

$$= 56.62156\ \mu V$$

The sensitivity of the sensor is determined as:

$$S = \frac{V_\Delta}{x} \tag{7.2}$$

where

S is the sensor sensitivity,

V_Δ is the maximum voltage difference for the sensor output, and

x is the maximum measuring range of the sensor.

$$S = \frac{100\ \text{mV}}{0.5\ \text{mm}}$$

$$\therefore S = 200\ \text{V/m}$$

This corresponds to 200 µV/µm. The influence that the voltage-error will have on the sensor resolution is therefore:

$$= \frac{56.62156\ \mu\text{V}}{200\ \mu\text{V/µm}}$$

$$= 283.1078\ \text{nm}$$

The effect of the modulated frequency on the sensor is therefore negligibly small, and will not be investigated further.

- **Frequency stability**

The frequency stability of the design over temperature was also determined by taking the FFT of the recorded signals. The FFT plots of all the first and last recorded signals are shown in Figure 7-8 and Figure 7-9.

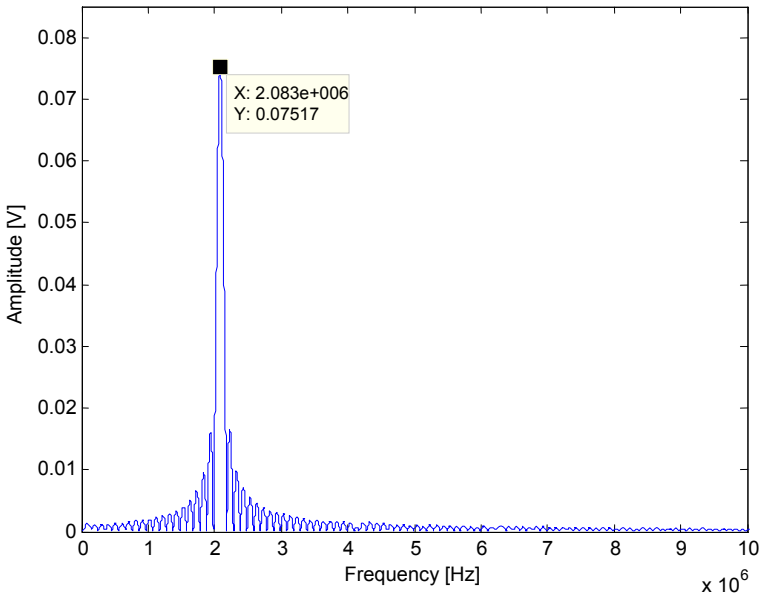


Figure 7-8 FFT plot of frequency at start-up room temperature (25.5°C)

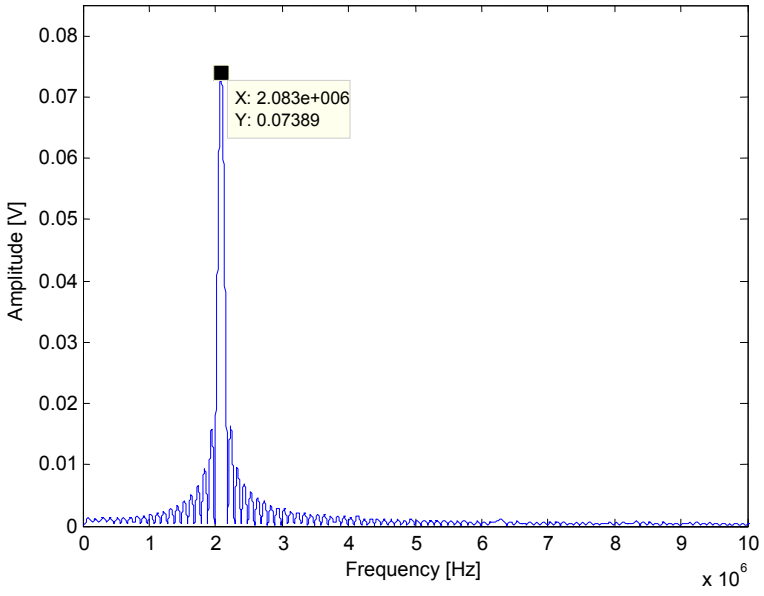


Figure 7-9 FFT plot of frequency at 80°C

Figure 7-10 shows the recorded frequency output over temperature. As mentioned before, due to the fact that the oscillator signal is at a high frequency and the sample rate of the digital oscilloscope is limited, the oscilloscope cannot obtain a finer frequency resolution than 1kHz for

the oscillator signal. Therefore, if there are any frequency deviations over temperature, it is less than 0.048 % or 480 ppm.

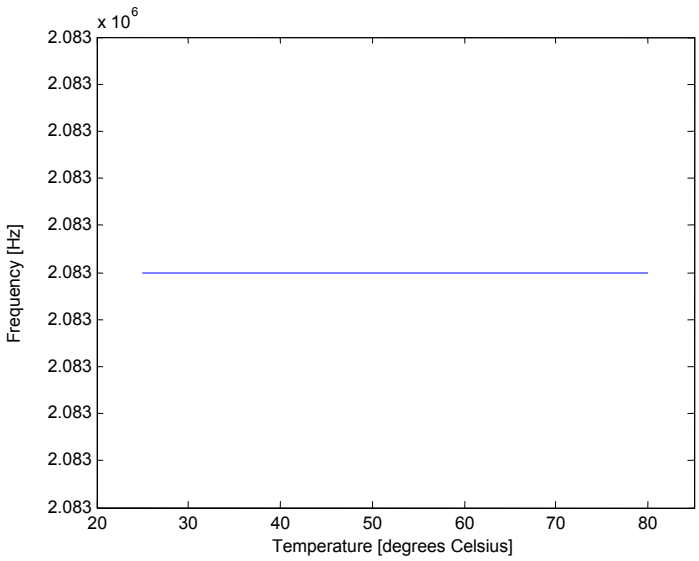


Figure 7-10 Recorded frequency output over temperature

7.1.4 Oscillator circuit performance summary

The variation of the amplitude of the oscillator output over time and temperature is higher than what was expected. The linearity estimation for the oscillator circuit was ±293 ppm, and the amplitude temperature stability was 200 ppm/°C. The increased amplitude variation may however be caused by inadequate PCB layout and routing, as well as external interference and noise. By applying good PCB layout and routing skills and by shielding the vulnerable high-frequency signals, the amplitude stability of the oscillator circuit will be improved. The frequency stability of the oscillator circuit, however, is excellent, emphasizing the design's suitability for implementation in the sensor driver.

7.2 Sensor driver test circuit

The sensor driver test circuit as discussed and described in chapter 4 was constructed and tested, and is shown in Figure 7-11. The measurements obtained from the circuit are presented in this section. The test circuit consisted of one excitation circuit and two signal conditioning

circuits, along with the first analogue power supply design. The test circuit was connected to a double-layer PCB eddy current sensor as used by [7].

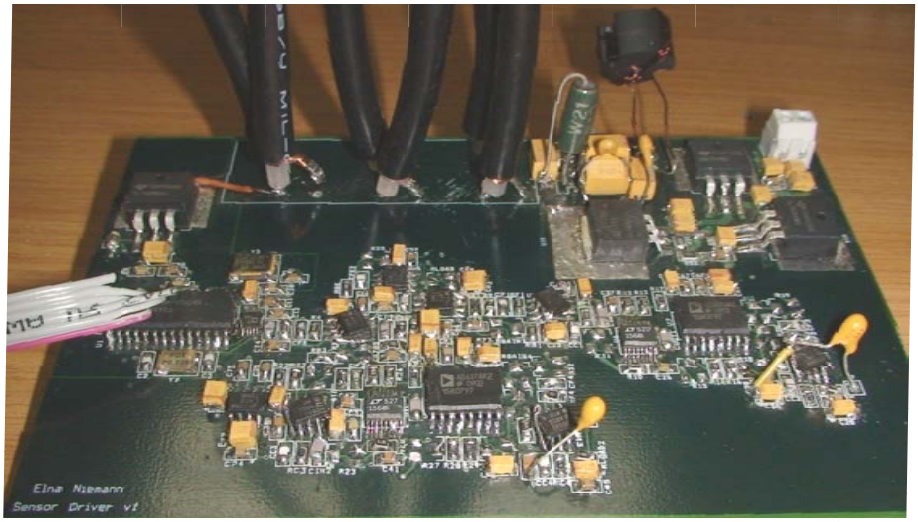


Figure 7-11 Sensor driver test circuit

The output of one x-axis and one y-axis detector coil were used in the measurements. The purpose of the test circuit was to verify the sensor driver analogue circuit design, and not for performance testing and validation. It will however be used to obtain a baseline figure regarding performance for the final sensor driver circuit. The measurements of the test circuit are divided into two sections, namely the excitation circuit's measurements and the signal conditioning circuits' measurements.

7.2.1 Excitation circuit measurements

Figure 7-12 shows the output signal of the AD9833 programmable waveform generator (PWG). The amplitude of the signal is found to be half of the expected signal at 80 mV_{p-p}. This can be can be explained by the impedance of the series AC-coupling capacitor together with the source resistor of the op-amp forming a voltage divider circuit at the operating frequency of 2.0833 MHz.

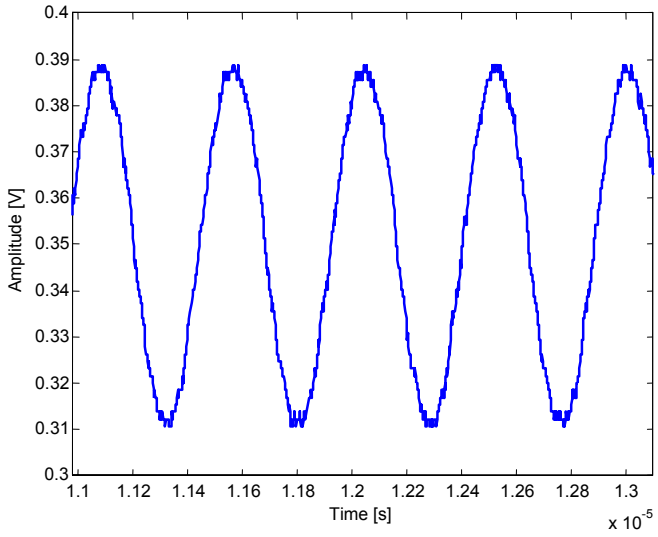


Figure 7-12 PWG output signal

The output signal of the first stage amplifier is shown in Figure 7-13. A slight DC-offset can be observed, which can again be explained by the inductance of the AC-coupling capacitor at the operating frequency of 2.0833 MHz.

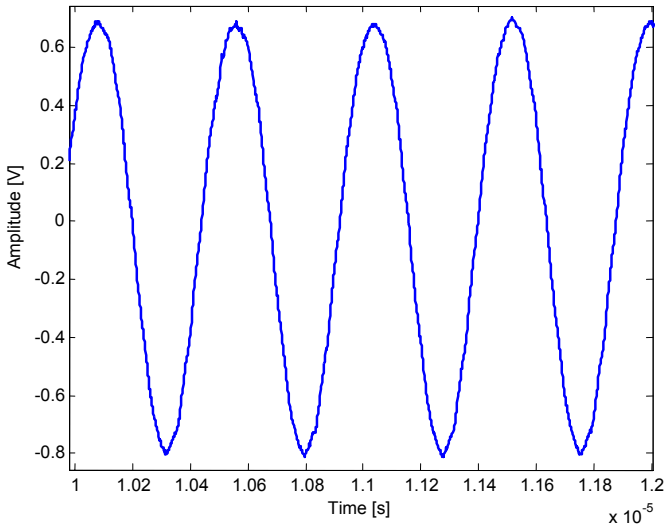


Figure 7-13 Output signal of first stage amplifier of excitation circuit

The final output of the excitation circuit, which forms the excitation signal to the PCB sensor, is shown in Figure 7-14. This measurement was taken for a constant rotor position and over a short period of time, thereby eliminating temperature variance. A closer view of the signal is shown in Figure 7-15.

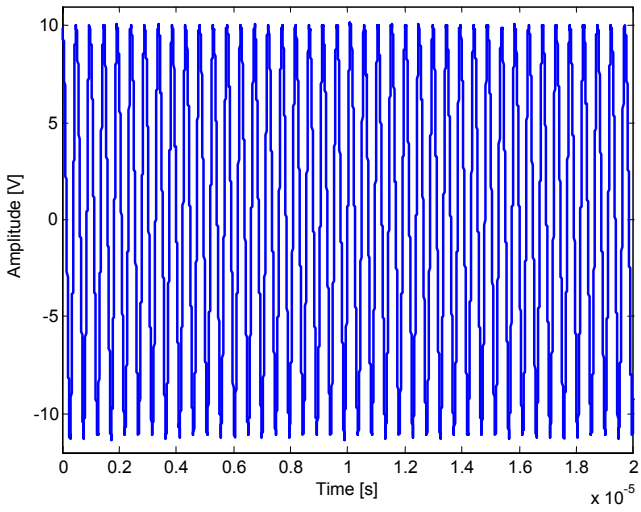


Figure 7-14 Output signal of excitation circuit

A DC-offset can again be observed in the output signal. The amplitude of the voltage signal is also less than expected at ±10 V instead of ±12 V. This can be due to saturation of some of the operational amplifiers caused by the smaller oscillator signal requiring a higher gain. This implies that the current signal is also less than expected, meaning that the excitation circuit is not capable of delivering the required current amplitude. The fact that the excitation signal applied to the sensor result in sensing signal outputs being generated means that the operational design concept of the sensor driver is verified. The current output signal of the excitation could not be measured with the test circuit, as the presence of the current probes interfered with the signal, resulting in the output signal becoming unstable.

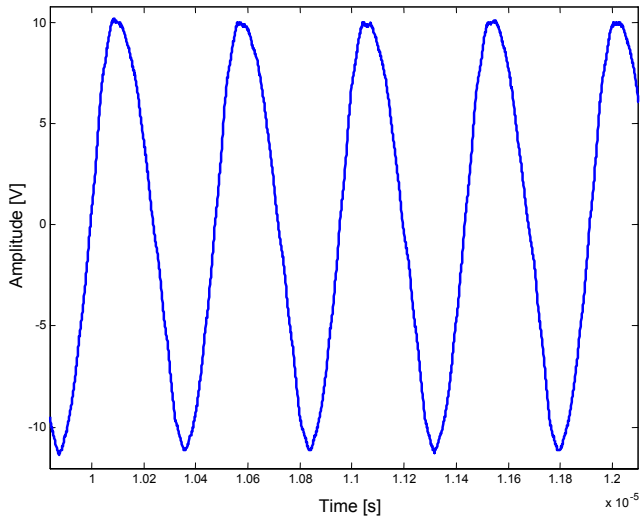


Figure 7-15 Closer view of excitation signal

7.2.2 Signal conditioning circuit measurements

The measurements of the signal conditioning circuits were taken at the input signals to the circuit. The rotor was displaced in order to obtain a maximum and minimum input signal and an output signal of the x-axis and y-axis respectively.

Figure 7- 16 shows the maximum input signal to the signal conditioning circuit for the x-axis of the sensor. The amplitude is somewhat larger than expected at ±0.71 V instead of ±0.55 V. This difference may be due to the change in excitation signal amplitude from the excitation signal used in the design of the PCB sensor in [7].

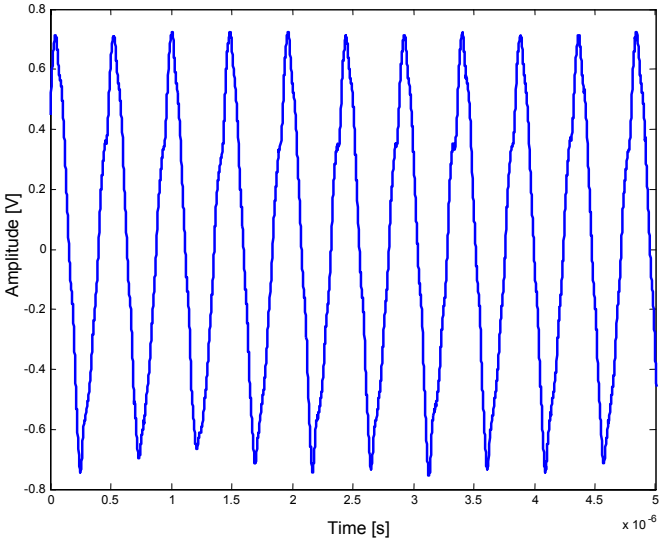


Figure 7- 16 Maximum x-axis input to signal conditioning circuit

The minimum input signal to the signal conditioning circuit for the x-axis is shown in Figure 7-17. Again, the amplitude of the signal is greater than expected at ±0.58 V instead of ±0.45 V. The voltage difference between the maximum and minimum input signals is therefore 130 mV instead of just 100 mV, which relates to greater accuracy of the sensor driver system with a greater resolution. The larger the signal compared to the noise which may be present on the signal, the more accurately the position displacement can be detected, which in turn results in a better sensor resolution.

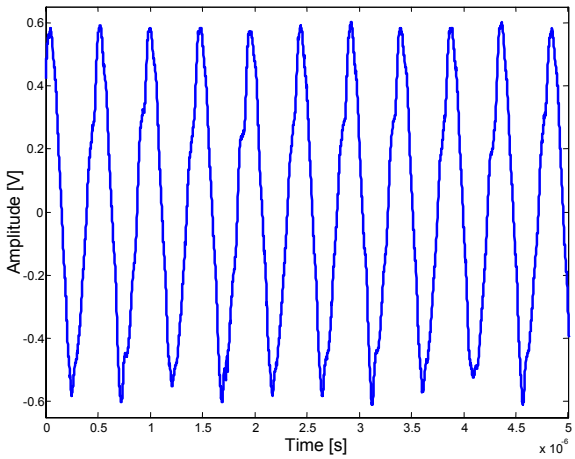


Figure 7-17 Minimum x-axis input to signal conditioning circuit

The output signal of the signal conditioning circuit for the x-axis is shown in Figure 7-18. The output corresponds to rapid random movement of the rotor from its maximum to minimum positions. From the figure it can be seen that the full output range of the gain and scaling op-amp is used. The input range of the ADC that will be utilized will therefore be ±3.8 V out of a possible ±5 V, which correlates to 76 % of the entire input range of the ADC that will be used.

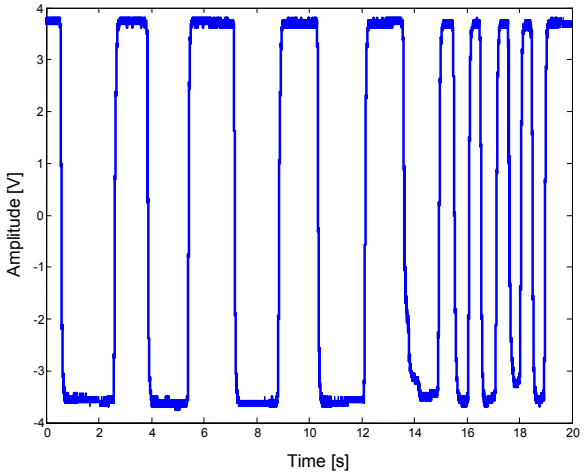


Figure 7-18 Signal conditioning circuit output for x-axis

Figure 7-19 shows the maximum input signal to the signal conditioning circuit for the y-axis of the sensor. The amplitude is once again somewhat larger than expected at ±0.70 V instead of ±0.55 V. The minimum input signal to the signal conditioning circuit for the y-axis is shown in Figure 7-20. Again, the amplitude of the signal is greater than expected at ±0.57 V instead of

±0.45 V. The voltage difference between the maximum and minimum input signals is therefore also 130 mV instead of just 100 mV.

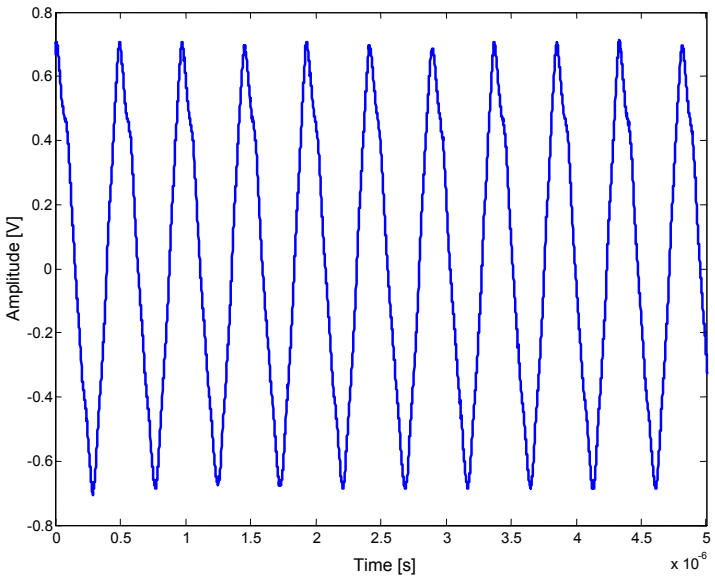


Figure 7-19 Maximum y-axis input to signal conditioning circuit

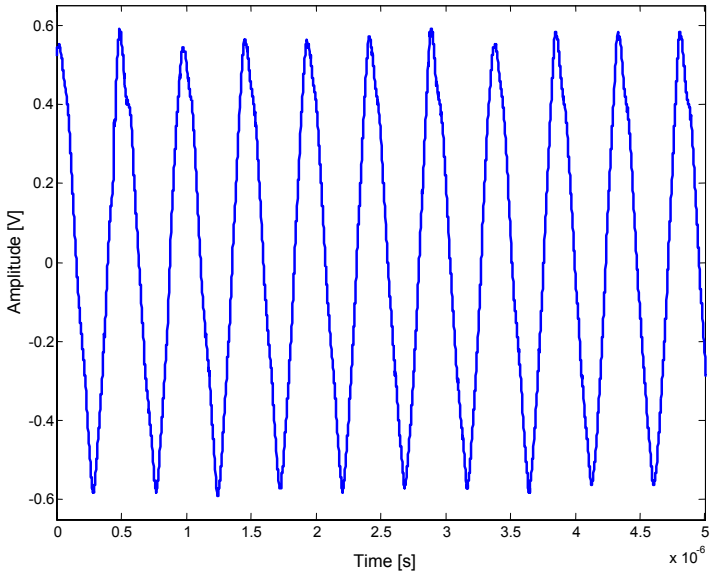


Figure 7-20 Minimum y-axis input to signal conditioning circuit

The output signal of the signal conditioning circuit for the y-axis is shown in Figure 7-21. The output corresponds to random movement of the rotor from its maximum to minimum positions in the y-axis. From the figure it can be seen that the full output range of the gain and scaling op-

amp is used. The input range of the ADC that will be utilized will therefore be ±3.8 V out of a possible ±5 V, which again correlates to 76 % of the entire input range of the ADC that will be used.

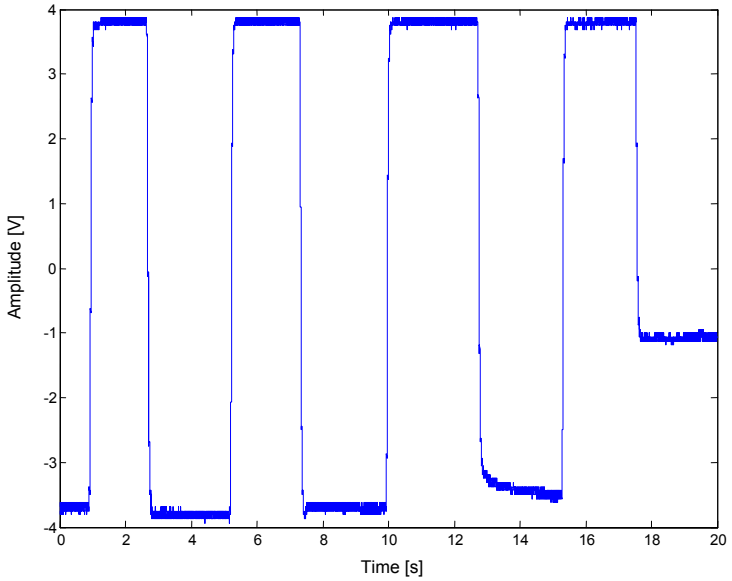


Figure 7-21 Signal conditioning circuit output for y-axis

7.3 Final sensor driver circuit

Figure 7-22 shows the test setup of the PCB sensor used during the evaluation of the sensor driver system. The test setup for the sensor driver is shown in Figure 7-23. The final sensor driver circuit is evaluated by capturing the position values with the ADCs and performing the differential position extraction on the signals in the FPGA. The differential position extraction is done by subtracting the opposite sensor signals from each other. This results in a single position signal for each axis. Since the two radial PCB eddy current sensors used in this project each measure only the x- and y-axis, the total number of position signals equal four. Figure 7-24 and Figure 7-25 illustrate how the signals from each sensor are connected to the sensor driver circuits, and how they are in turn connected to the ADCs and loaded in the software.

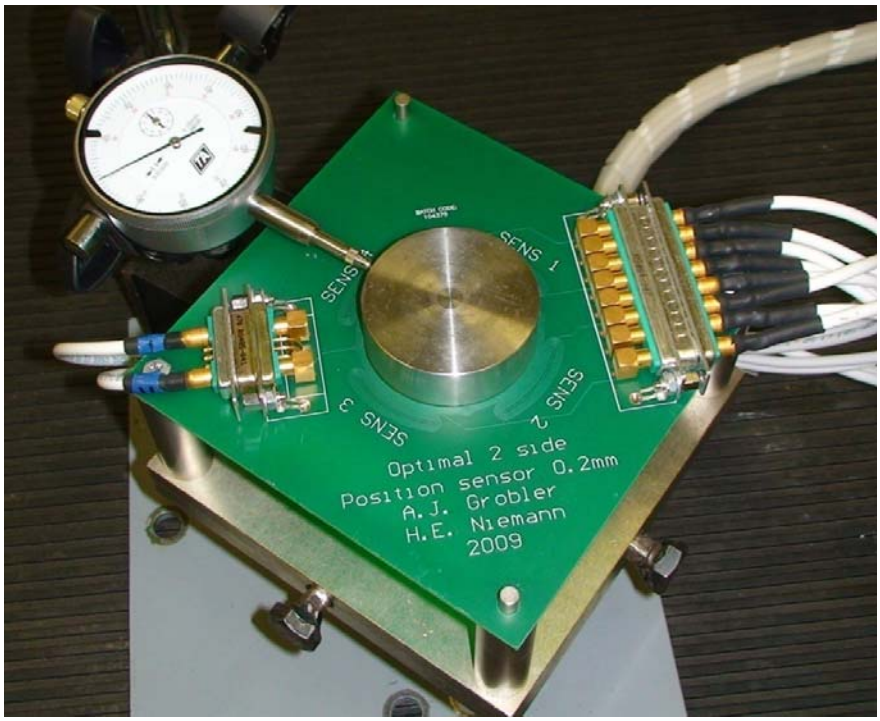


Figure 7-22 Sensor test setup

Figure 7-23 Sensor driver test setup

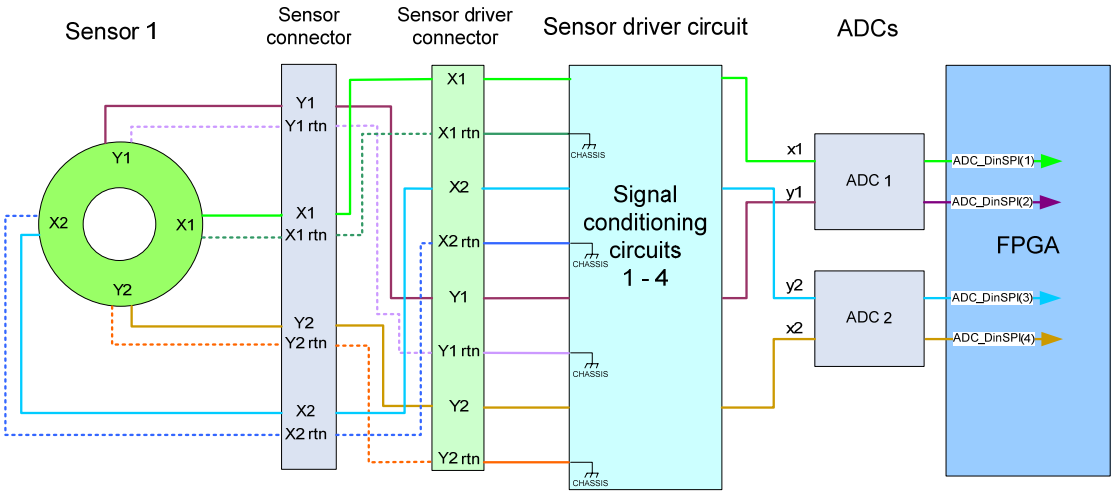


Figure 7-24 Sensor driver connection diagram for sensor 1

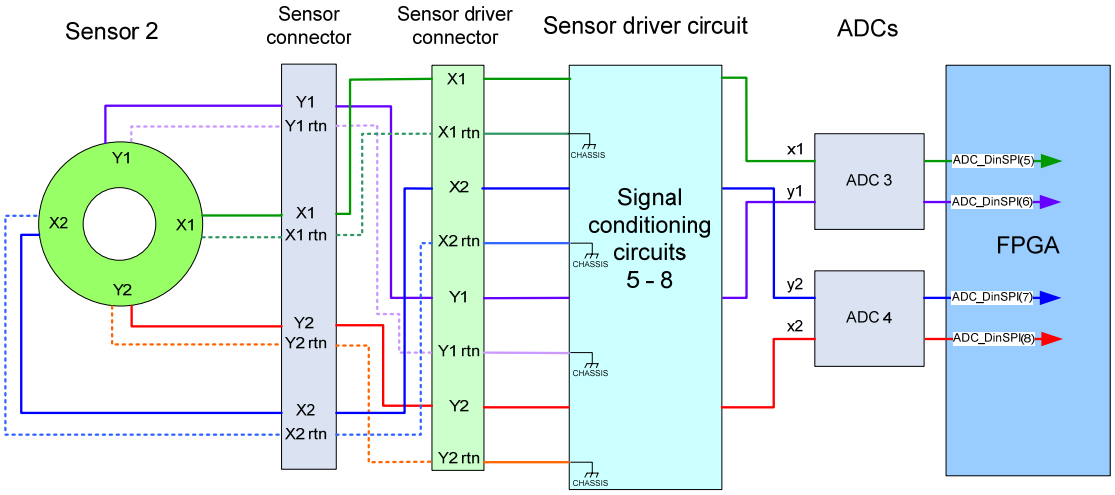


Figure 7-25 Sensor driver connection diagram for sensor 2

Figure 7-26 illustrates how the signals from the sensors, as shown in Figure 7-24 and Figure 7-25 link with the signals in the software on the FPGA. The signals from the ADCs are read into a 14-bit vector (ADCdatOut) by the ADC control block, and then sent to the FIR filter control block, FIR Control. From there the filtered signals are sent to the corresponding difference control blocks, namely DIFF Control 1 - 4, where differential position extraction is performed to produce a single position signal per axis. These uncompensated signals are then sent to their corresponding compensation blocks where they are passed through a fitting function in order to linearize the output.

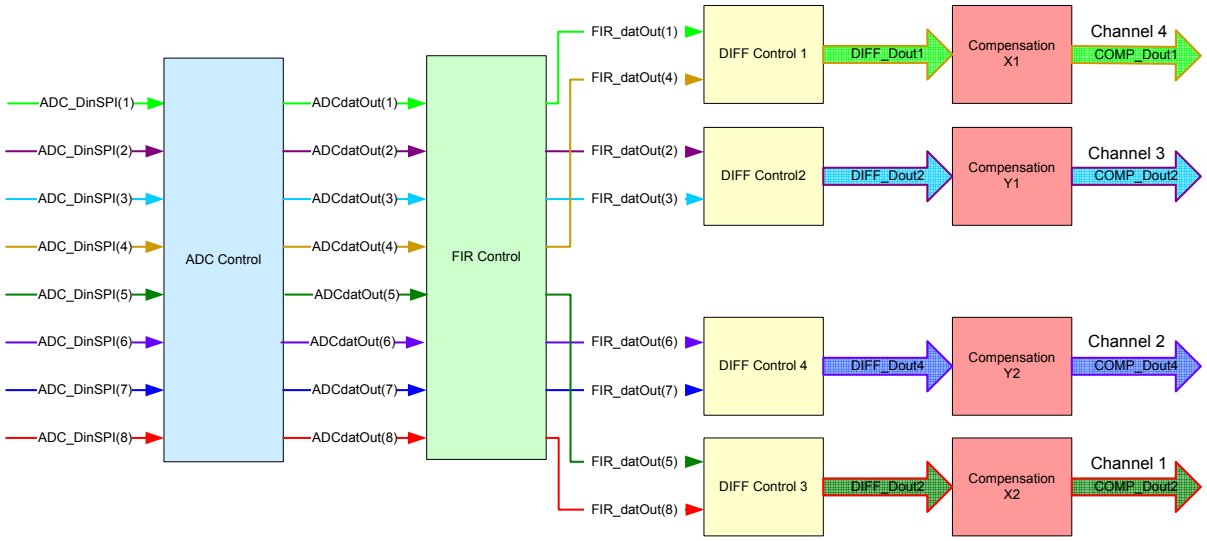


Figure 7-26 Software signal connection diagram

The channels shown in Figure 7-26 indicate the corresponding channel to be selected in the USB GUI in order to capture the corresponding axis' signals. In the software, X1 and Y1 represent the x- and y-axis signals of sensor 1, and X2 and Y2 represent the x- and y-axis signals for sensor 2. In the hardware, however, x1 and x2 are the signals from the two x-axis sensing coils on each PCB sensor, and y1 and y2 are the signals from the two y-axis sensing coils on each sensor. The final sensor driver circuit is evaluated in both the analogue and digital domains in order to verify the design of the sensor driver circuit as a whole, and validate the performance of the sensor driver system. Each domain will now be discussed.

7.3.1 Analogue evaluation

For the analogue evaluation of the sensor driver circuit, the outputs of the main sub-systems of the sensor driver circuit are measured and evaluated against the specifications set for the specific sub-system in Chapter 3 and the estimations in Chapter 4. The sub-systems to be measured are the following:

- Excitation circuits 1 & 2:
  - Final outputs
- Signal conditioning circuits 1 – 8:
  - Input signals from sensor
  - BPF output signals
  - Gain and scaling amplifier output / ADC input

- Power supply circuits:
    - ±15 V
    - ±5 V
    - 5V_D
    - 5V_COM
    - 1V2_D
    - 1V8_D
    - 3V3_D

The sub-systems will only be evaluated with regards to linearity and not temperature stability, as it is not feasible to perform temperature stability tests on a fully populated circuit board. As stated in Chapter 4, the temperature stability specifications and estimates were only determined to assist with the component selection process. A thermal analysis of the sensor driver board follows in section 7.5.2.

7.3.1.1 Excitation circuits

The voltage output signals of the excitation circuits are shown in Figure 7-27. The amplitudes of both voltage signals are around 18 V_{p-p}, with a frequency of 2.083 MHz. The current output signals of the excitation circuits are shown in Figure 7-28. The amplitude of both excitation current signals is around 200 mA_{p-p}.

Due to the fact that the excitation circuit receives an input of constant amplitude, and produces an output of constant amplitude as a result of a static rotor position, its performance cannot be measured in terms of linearity. The excitation circuit's performance is therefore given in terms of amplitude stability. The output current signal of the excitation circuit was measured for varying rotor positions, and was found to be constant throughout for both sensors. The amplitude stability of the signals are determined by taking the mean of the maximum and minimum deviations of the amplitudes of the signal, and calculating the percentage deviation with regards to the mean of the amplitude of the signal. A requirement specification was not set for the amplitude stability of the excitation circuit, as the amplitude stability of the excitation signal will influence the linearity of the sensor driver's outputs, for which a requirement specification was set.

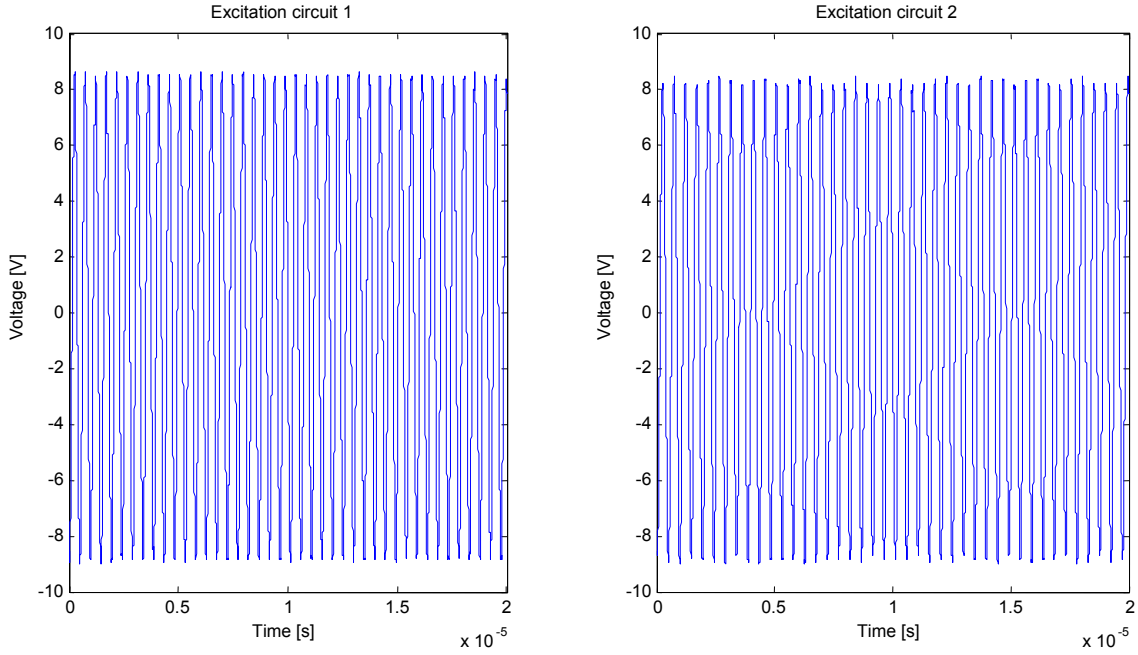


Figure 7-27 Voltage output signals of both excitation circuits

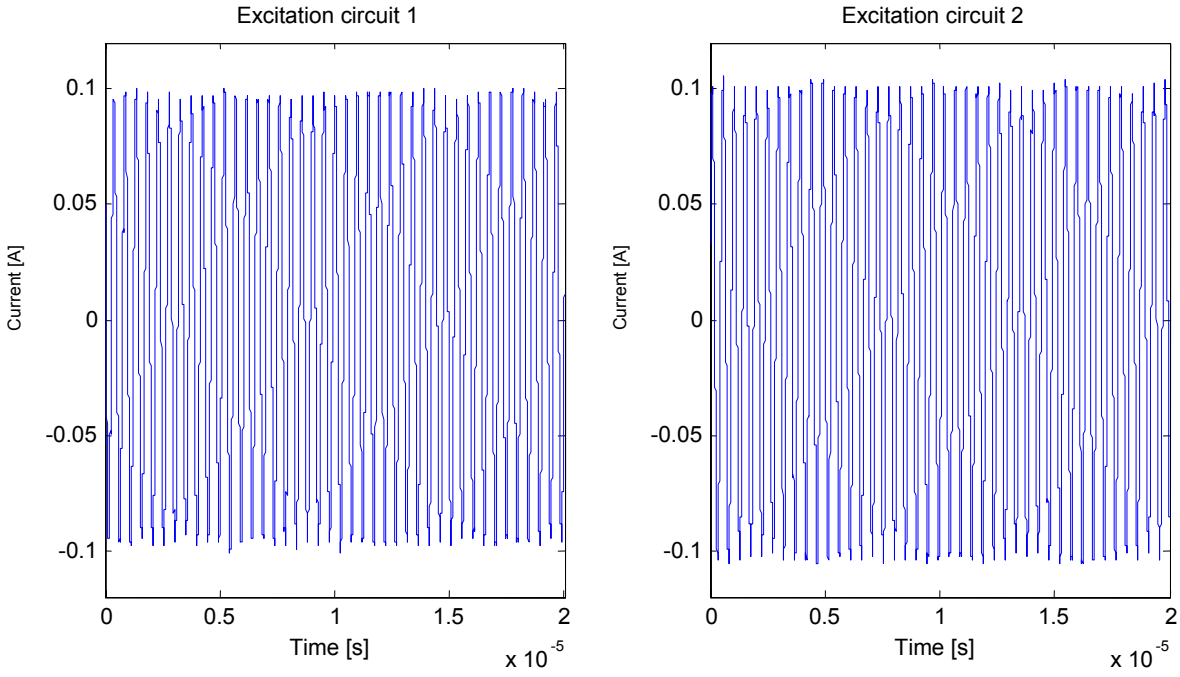


Figure 7-28 Current output signals of both excitation circuits

Table 7-1 Amplitude stability of excitation circuits

	Excitation circuit 1	Excitation circuit 2
Voltage amplitude stability	±0.877 %	±1.8 %
Current amplitude stability	±1.237 %	±0.909 %

7.3.1.2 Signal conditioning circuits

Figure 7-29 and Figure 7-30 show the measurements of the signal conditioning circuits of sensor 1 and sensor 2 respectively. Each row corresponds to a differential sensor output, with x1 and x2 being the differential x-axis outputs, and y1 and y2 the differential y-axis outputs of the sensor. The inputs to the signal conditioning circuit is presented in the first column, the outputs of the band-pass filters (BPFs) in the second column, and the outputs of the gain and scaling amplifiers, or inputs to the ADCs, in the third column.

The input signal for the signal conditioning circuits have an average range of ±50 mV or 100 mV_{p-p} for the total position deviation of the test rotor. Although the input signals are somewhat noisy, the BPF attenuates all other frequency components outside of the 200 kHz pass-band, with its centre frequency at the excitation frequency of 2.083 MHz. This results in the output signal of the BPF containing much less noise than its input.

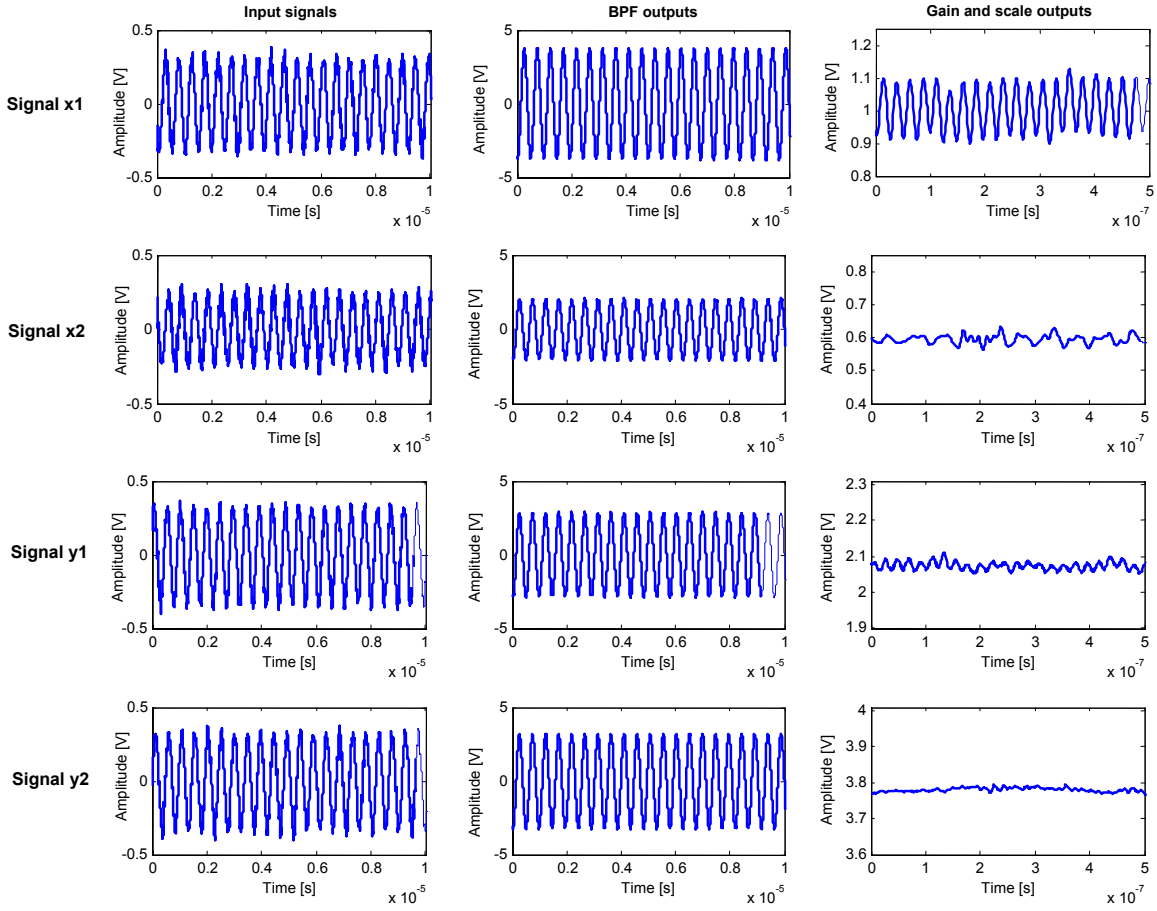


Figure 7-29 Analogue outputs for sensor 1

As can be observed in both Figure 7-29 and Figure 7-30, the gain and scaling output of signals x1 both contain a large noise component, measured to be a 40 MHz signal. With the only common denominator between these two signal conditioning circuits being their close proximity to the power supply circuits, excitation circuits and digital circuit, the noise component may be explained by the high frequencies of these circuits causing interference on the analogue signals. All the other signal conditioning circuits are located at the centre of the board, and are therefore not as greatly influenced by these high frequencies.

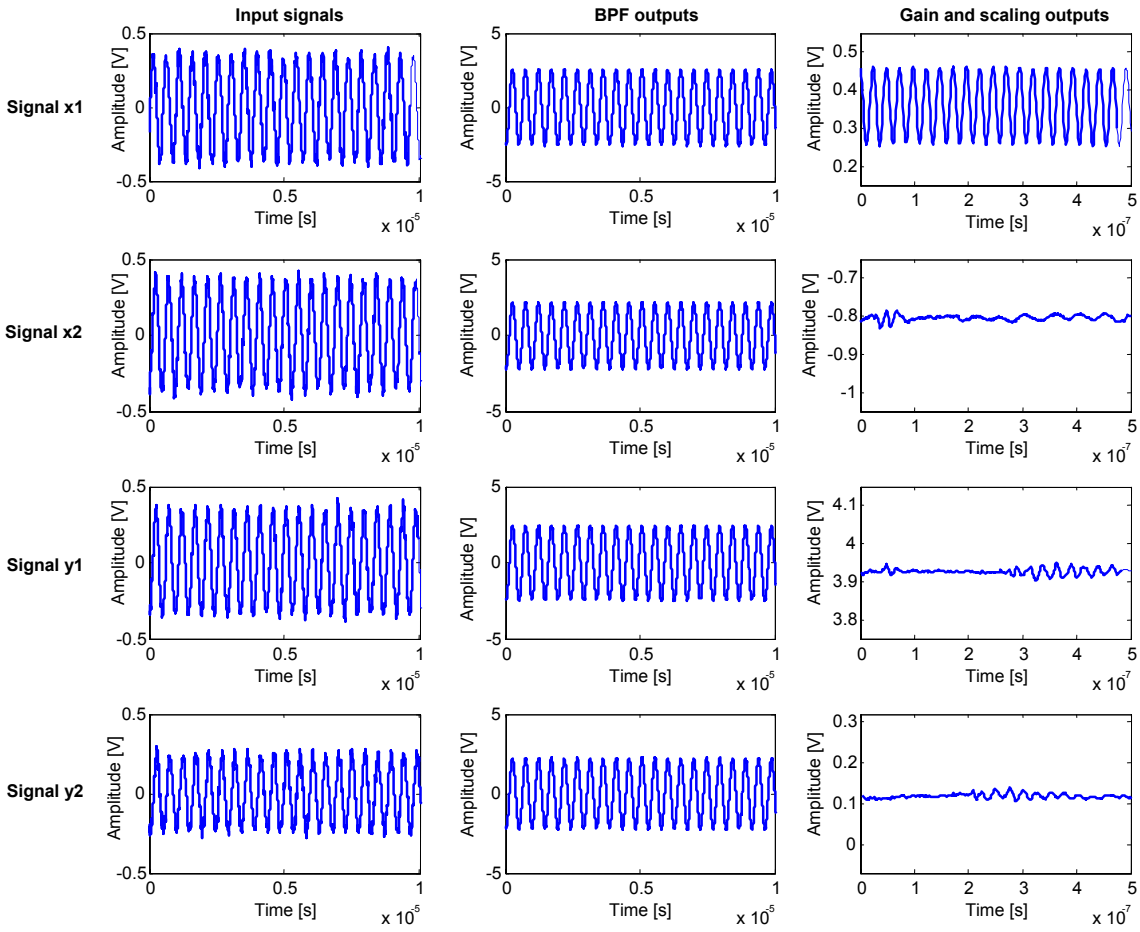


Figure 7-30 Analogue outputs for sensor 2

7.3.1.3 Power supply circuits

The power supply circuits are evaluated on three measurements, namely the output voltage, output accuracy and voltage ripple. The output voltage is the mean of the measured voltage signal, the output accuracy is the dc error or percentage deviation of the signal mean from the required voltage, and the voltage ripple is the percentage deviation of the maximum ripple on the measured mean voltage.

The analogue power supply circuits are required to each have an output accuracy of no worse than ±1.5 %, as specified in the design. The digital power supplies are required to have an output accuracy of no more than ±5 % in order for the generated voltages to be within the power supply input ranges of the FPGA. The output voltage, output accuracy and voltage ripple of each of the power supplies are presented in Table 7-2.

Table 7-2 Power supply measurements

	Output voltage	Output accuracy	Voltage ripple
Sensor 1:			
+15 V	15.0255 V	0.17 %	0.416 %
-15 V	-15.0863 V	0.5753 %	0.3221 %
+5 V	5.0143 V	0.286 %	0.4068 %
-5 V	-5.0387 V	0.7740 %	0.6212 %
Sensor 2:			
+15 V	15.0303 V	0.202 %	0.312 %
-15 V	-15.1038 V	0.692 %	0.3105 %
+5 V	5.0011 V	0.022 %	0.4379 %
-5 V	-5.0477 V	0.954 %	0.8657 %
Digital:			
5V_D	5.0783 V	1.566 %	1.8471 %
5V_COM	5.2202 V	4.04 %	0.7471 %
3V3_D	3.3599 V	1.8152 %	3.2114 %
1V2_D	1.1565 V	3.625 %	7.9723 %
1V8_D	1.8063 V	0.35 %	6.3112 %

As can be seen from Table 7-2, all the analogue power supplies' output accuracies are within the specified 1.5 %. The voltage ripple of all the analogue power supplies is also under 1 %, which implies a very stable voltage output. Both the output accuracy and voltage ripple of the digital power supplies are also all within the specified 5 %. Hence, the entire power supply circuit adheres to its requirement specifications, verifying and validating the power supply circuit design.

7.3.2 Digital evaluation

The digital evaluation is performed by loading measurements stored in the SRAM and reading it out to a computer via the USB port. Three sets of measurements are to be discussed, namely the measured value against the real value, the fitting function to be implemented in order to linearize the position signal, and the signal linearity. The measurements were taken while displacing the test rotor of the PCB sensor in increments of 20 µm. The first set of measurements was obtained by first plotting the maximum and minimum values of DIFF_Dout1

to DIFF_Dout4, determining the mean of each, and scaling the corresponding COMP_Dout values accordingly around zero. These scaling values were then programmed and the second set of measurements taken. The measurements shown in the figures are therefore that of the corresponding COMP_Dout signal, and are given in bit value.

7.3.2.1 Sensor 1 x-axis

Figure 7-31 shows the plot of the measured value COMP_Dout1 against the real value for the x-axis of sensor 1. As can be seen from the figure, the signal is not totally linear and needs to be compensated in order to obtain a linear output signal.

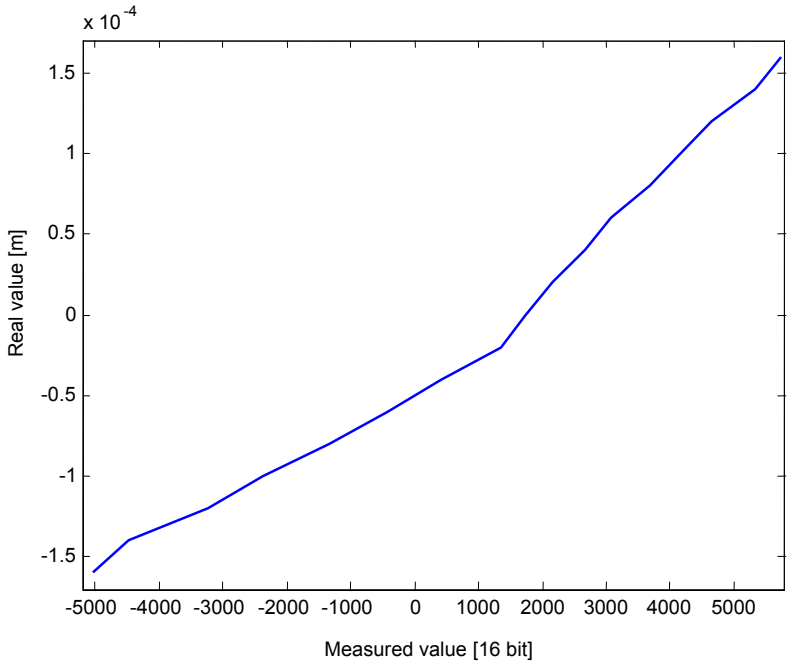


Figure 7-31 Measured value against real value for x-axis of sensor 1

The best fitting function for the uncompensated position signal is determined using the basic fitting tool in Matlab®, and is shown in Figure 7-32, along with the error between the measured value and the fitting function.

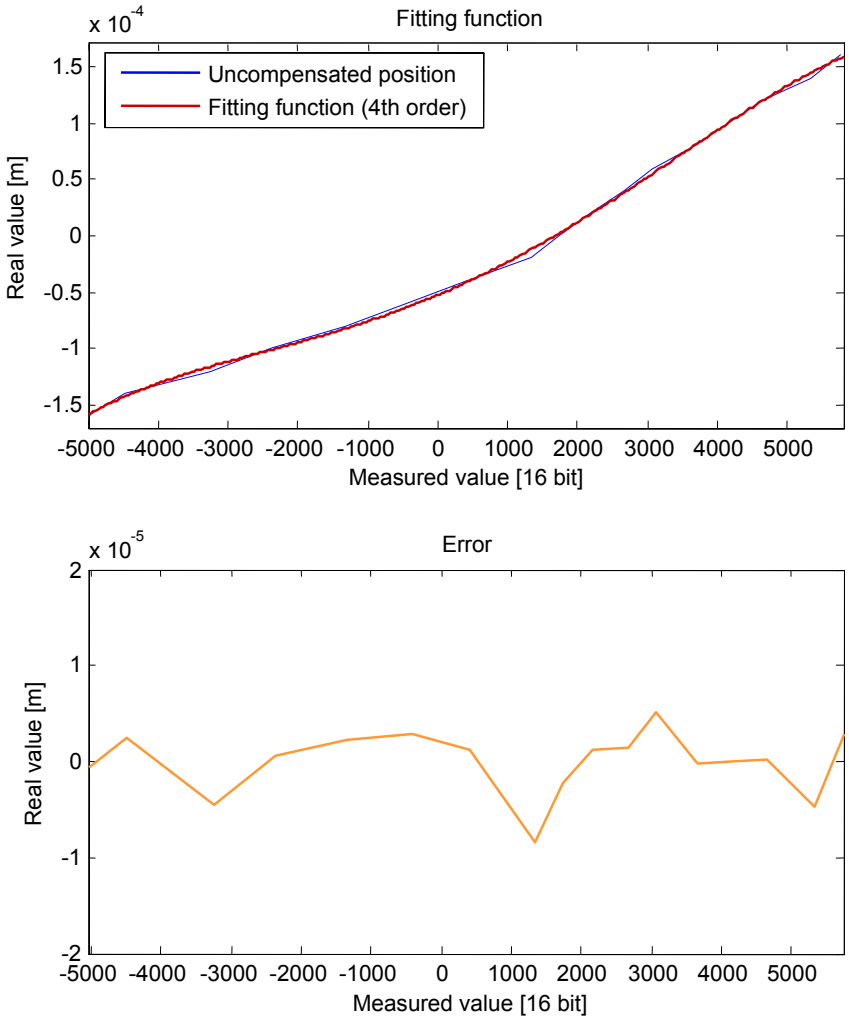


Figure 7-32 Fitting function and error for uncompensated position of x-axis of sensor 1.

A fourth order fitting function is required to linearize the uncompensated position signal, and is determined as:

$$y = (-5.9003e^{-20})x^4 + (1.1675e^{-16})x^3 + (3.071e^{-12})x^2 + (2.6169e^{-8})x - 5.2458e^{-5} \quad (7.3)$$

This fitting function poses a problem for implementation in the FPGA, as the required timing constraints are not met when it is implemented using basic fixed-point numeric multiplication methods. It is therefore recommended to perform the linearization on a floating point main controller instead of on the FPGA.

- **Linearity of x-axis signal of sensor 1**

The linearity of the signal is determined by plotting the measured value together with a straight line. The deviation of the measured signal from the straight line is its non-linearity. The better the measured signal fits the straight line, the more linear the signal is. Figure 7-33 shows the signal linearity of the x-axis position signal of the first sensor.

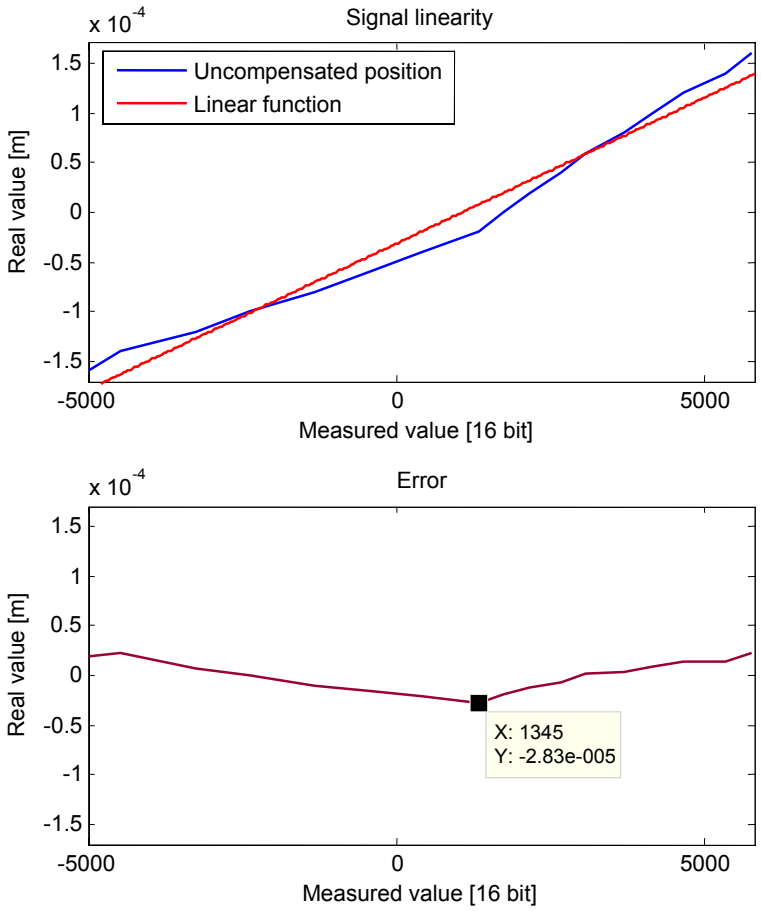


Figure 7-33 Signal linearity and error of the x-axis position signal of sensor 1

The full scale output (FSO) linearity of the signal is equal to the highest percentage deviation of the measured signal from the straight line. For the x-axis of sensor 1, its linearity is calculated as follows:

$$\text{Linearity (\%)} = \frac{\text{Deviation (m)}}{\text{Output range (m)}} \times 100 \qquad (7.4)$$

$$= \frac{2.83e^{-5}\ \text{m}}{320e^{-6}\ \text{m}} \times 100$$

= 8.8437 % FSO

7.3.2.2 Sensor 1 y-axis

The measured value against real value plot for COMP_Dout2 is shown in Figure 7-34. This is the measured output for the y-axis of sensor 1. As can be seen from the figure, the uncompensated value of the measurement is not linear, and must therefore be compensated by implementing a fitting function. Figure 7-35 shows the fitting function for the uncompensated signal.

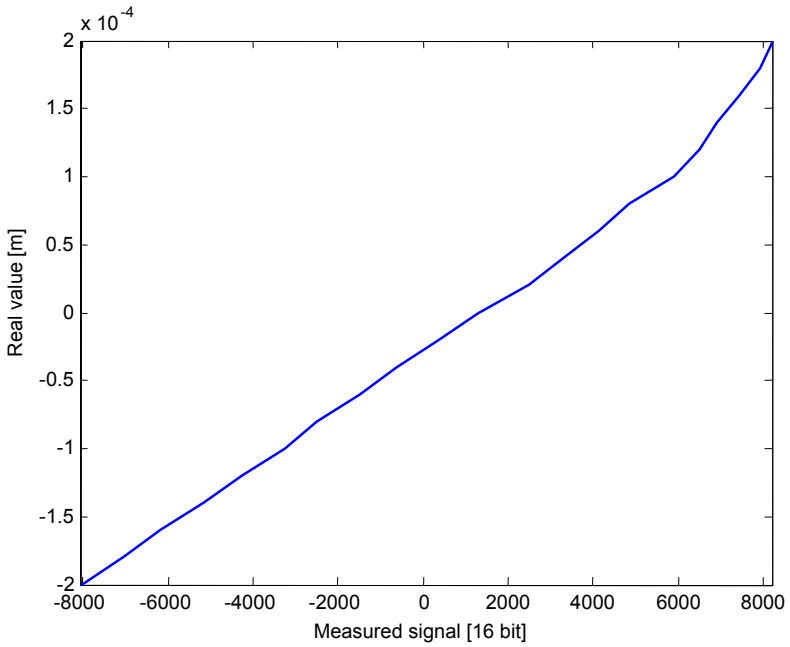


Figure 7-34 Measured value against real value for y-axis of sensor 1

The fitting function required to linearize the output of the measured signal was determined to be a fourth degree function, and is given as follows:

$$y = (1.0545e^{-20})x^4 + (6.0277e^{-17})x^3 + (-3.3707e^{-13})x^2 + (2.0109e^{-8})x - 2.7206e^{-5} \qquad (7.5)$$

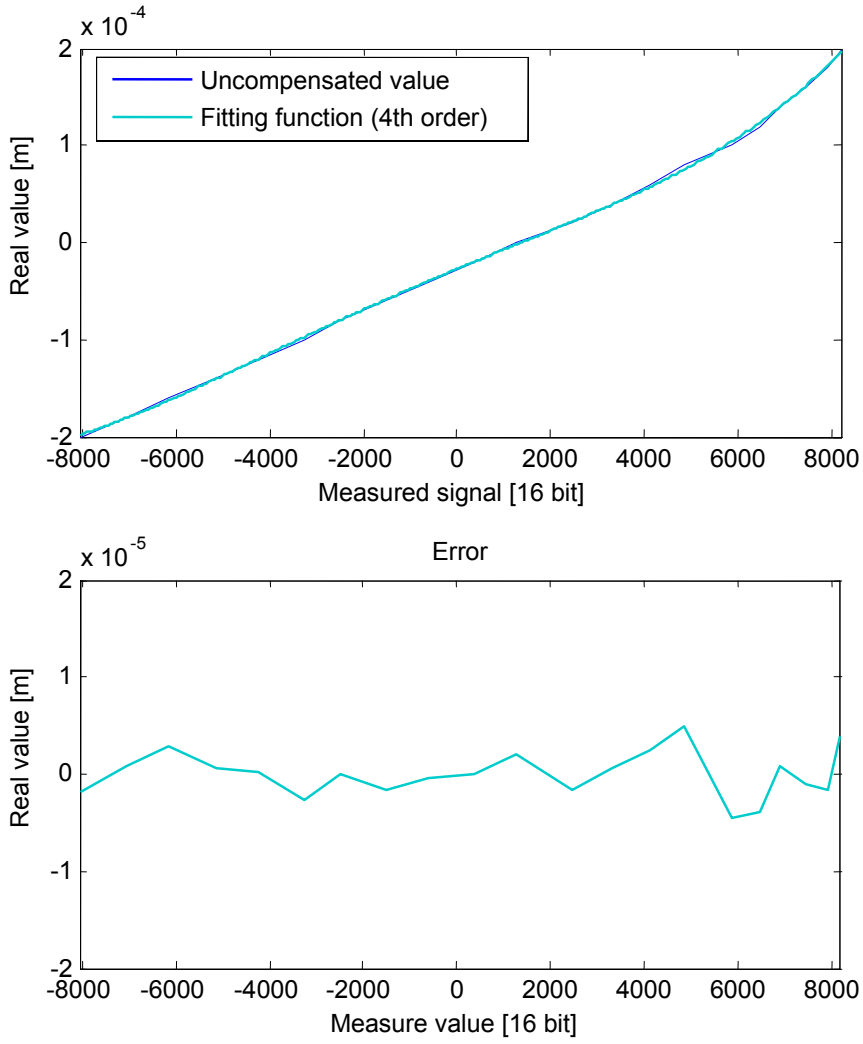


Figure 7-35 Fitting function and error for uncompensated position of y-axis of sensor 1

- **Linearity of y-axis signal of sensor 1**

Figure 7-36 shows the signal linearity of the y-axis position signal of the first sensor. The FSO linearity of the y-axis signal of sensor 1 is calculated as follows:

$$\text{Linearity (\%)} = \frac{\text{Deviation (m)}}{\text{Output range (m)}} \times 100 \qquad (7.6)$$

$$= \frac{3.227e^{-5}\ \text{m}}{400e^{-6}\ \text{m}} \times 100$$

= 8.0675% FSO

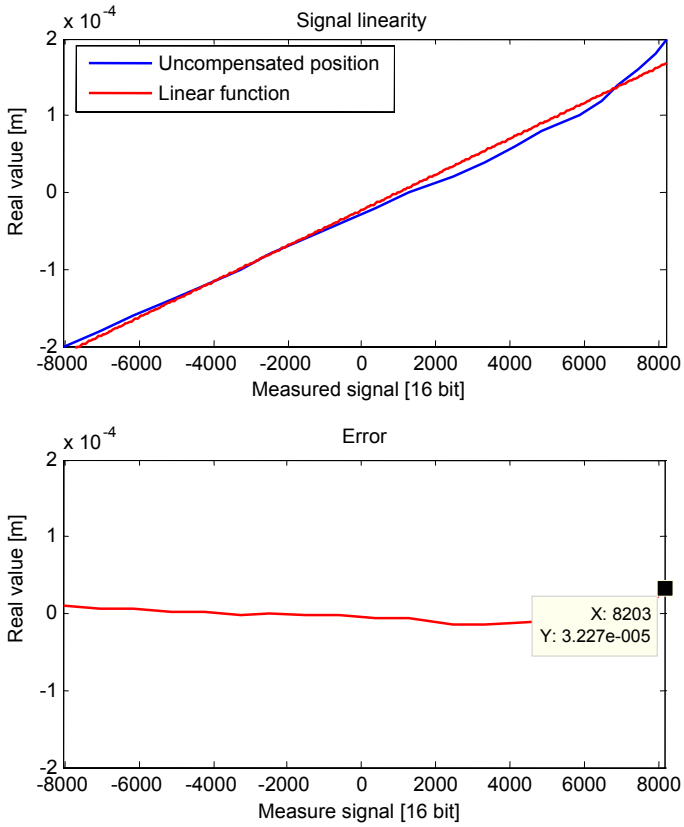


Figure 7-36 Signal linearity and error of the y-axis position signal of sensor 1

7.3.2.3 Sensor 2 x-axis

The plot of the measured value COMP_Dout3 against the real value for the x-axis of the second sensor is shown in Figure 7-37.

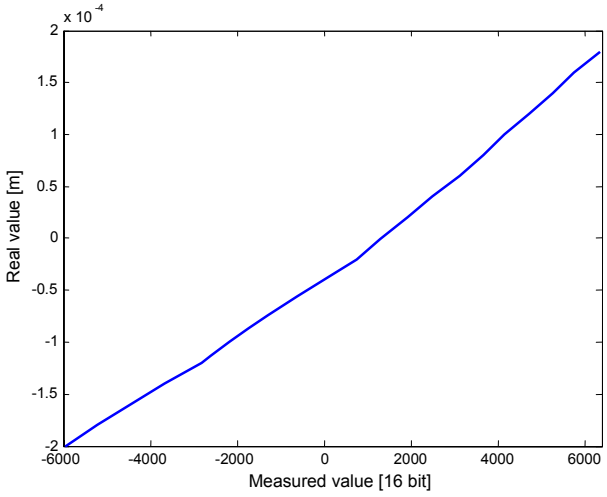


Figure 7-37 Measured value against real value for x-axis of sensor 2

This measured value is the most linear of all the measured axis, but is still not totally linear. Compensation is therefore still necessary in order to linearize the output of the measured signal. Figure 7-38 shows the fitting function required to linearize the output of the measured signal. The fitting function is determined to be quadratic, and is given by the following equation:

$$y = (6.5846e^{-13})x^2 + (3.041e^{-8})x - 3.9165e^{-5} \qquad (7.7)$$

Although it is possible to implement this quadratic fitting function on the FPGA, it is impractical to implement the linearization of some signals on the FPGA and others on the main controller. Therefore, the FPGA of the sensor driver will not perform any linearization of the uncompensated position signals.

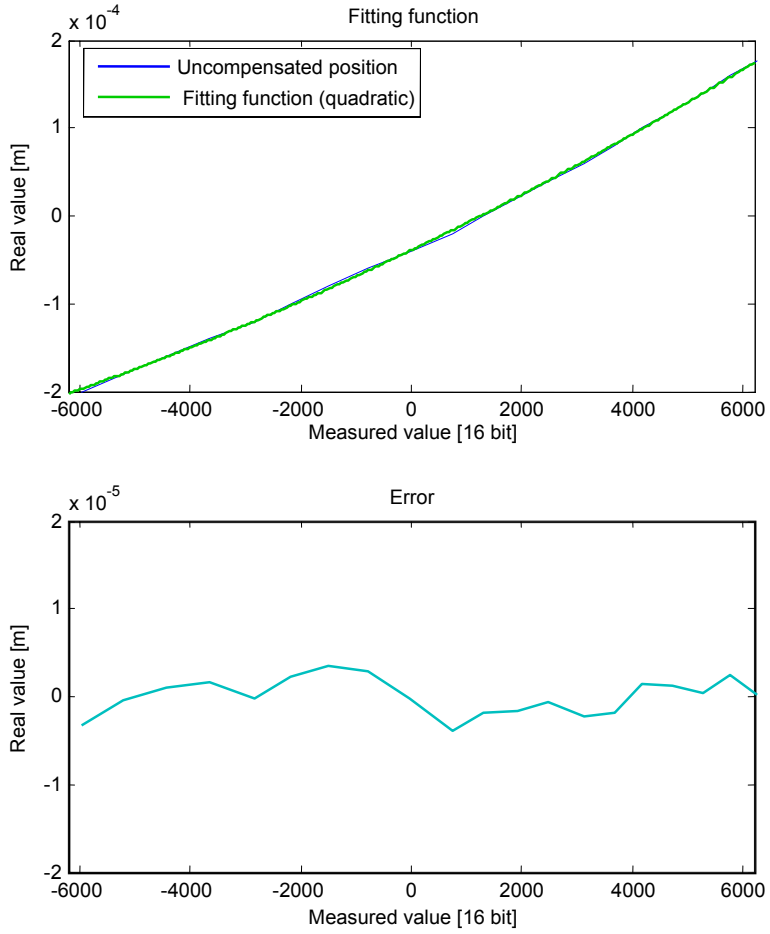


Figure 7-38 Fitting function and error for uncompensated position of x-axis of sensor 2

- **Linearity of x-axis signal of sensor 2**

The linearity of the signal of the x-axis of the second sensor is shown in Figure 7-41. The FSO linearity of the x-axis signal of sensor 2 is calculated as follows:

$$\text{Linearity (\%)} = \frac{\text{Deviation (m)}}{\text{Output range (m)}} \times 100 \tag{7.8}$$

$$= \frac{1.456e^{-5}\ \text{m}}{380e^{-6}\ \text{m}} \times 100$$

= 3.8316 % FSO

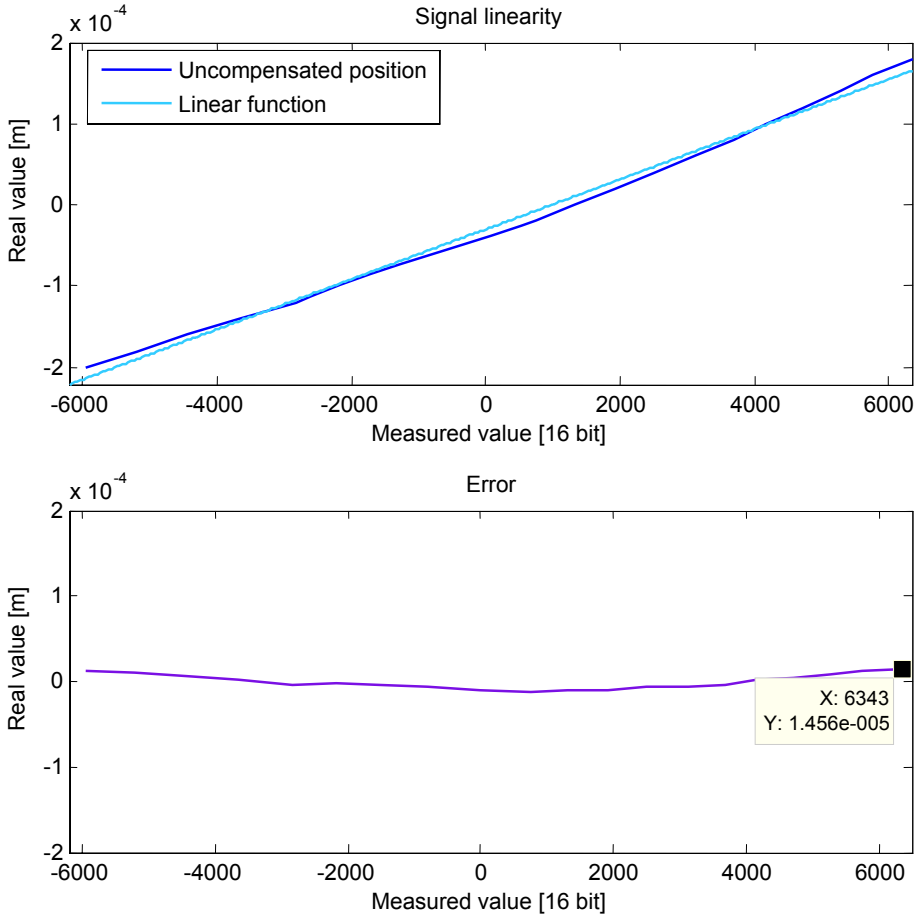


Figure 7-39 Signal linearity and error of the x-axis position signal of sensor 2

7.3.2.4 Sensor 2 y-axis

The y-axis of the second sensor's measured value is shown against the real value in Figure 7-40. It can clearly be seen that this signal is not linear, and must therefore be compensated in order to be linearized.

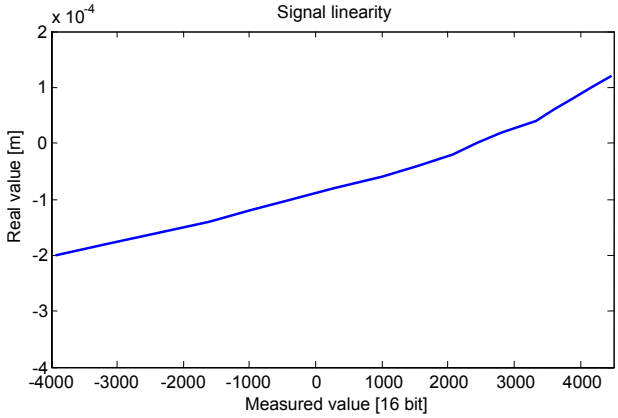


Figure 7-40 Measured value against real value for y-axis of sensor 2

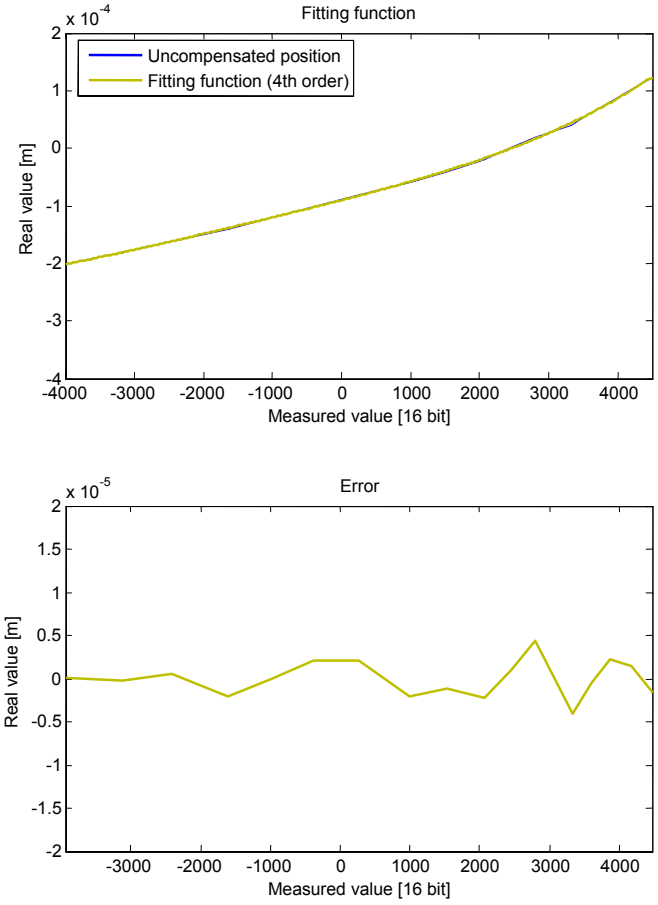


Figure 7-41 Fitting function and error for uncompensated position of y-axis of sensor 2

The compensating fitting function required to linearize the output signal is shown in Figure 7-41, and is determined to be a fourth order function given by the following equation:

$$y = (1.8515e^{-19})x^4 + (3.3575e^{-16})x^3 + (-9.1801e^{-13})x^2 + (3.0569e^{-8})x - 8.638e^{-5} \quad (7.9)$$

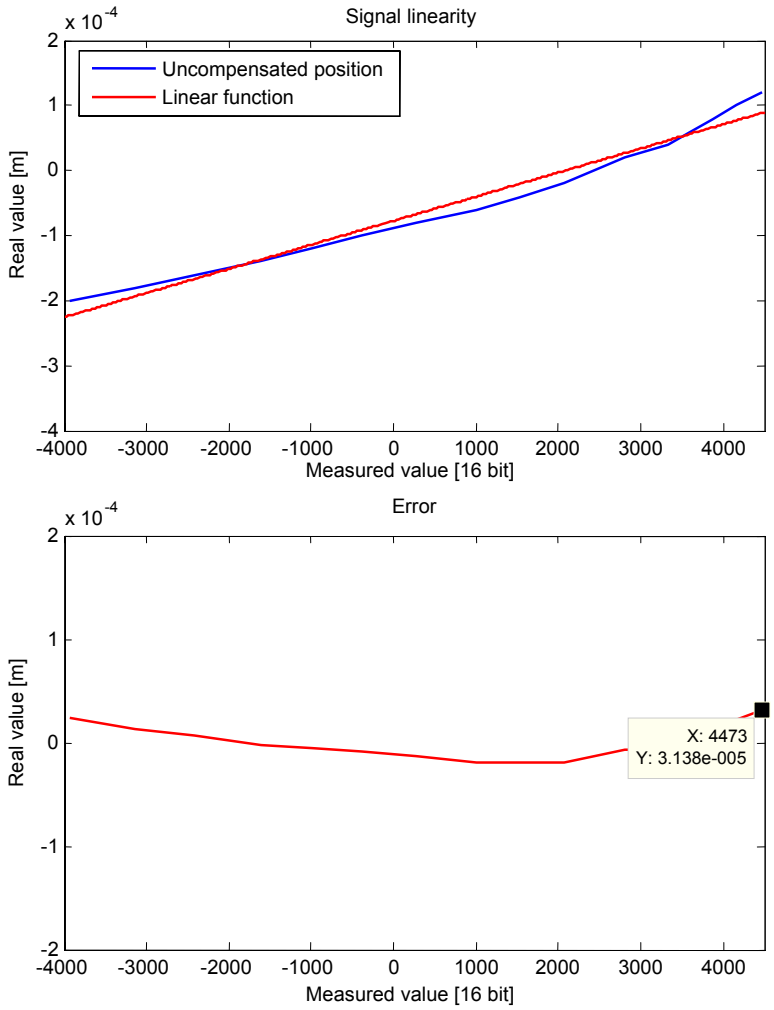


Figure 7-42 Signal linearity and error of the y-axis position signal of sensor 2

The FSO linearity of the y-axis position signal of sensor 2 is calculated as follows:

$$\text{Linearity (\%)} = \frac{\text{Deviation (m)}}{\text{Output range (m)}} \times 100 \quad (7.10)$$

$$= \frac{3.138e^{-5}\ \text{m}}{340\ e^{-6}\text{m}} \times 100$$

= 9.2294% FSO

7.3.2.5 Total linearity of sensor driver system

The linearity requirement specification determined in Chapter 3 was for a single-axis sensor in order for the specification to be comparable with the conventional eddy current sensors. As the PCB eddy current sensor each has two axis per sensor, the specification therefore applies to each axis. The linearity requirement specification determined in Chapter 3 was ±17.5 % FSO. The linearity of the uncompensated measured values for each axis is listed below.

- Sensor 1 x-axis: 8.8437 % FSO
- Sensor 1 y-axis: 8.0675 % FSO
- Sensor 2 x-axis: 3.8316 % FSO
- Sensor 2 y-axis: 9.2294 % FSO

Each axis therefore meets the required linearity specification, with the worst linearity being that of the y-axis of the second sensor at 16.745 % FSO.

7.3.3 Circuit sensitivity analysis

During the testing and evaluation process for the sensor driver board, it was noticed that the circuit displayed sensitivity towards certain factors that was not taken into consideration during the design process and that was not expected to have an influence on the circuit performance. The most prominent factors that the sensor driver circuit displays sensitivity to are the varying impedance effect of the sensor cables, and the circuit layout of the signal conditioning circuits. Each of these factors will now be discussed.

7.3.3.1 Varying impedance effect of sensor cables

During testing of the sensor driver board, it was discovered that any movement of the sensor cables influenced the output of the signal conditioning circuits. The circuit was particularly sensitive to the parting of a signal cable from it's return cable, and resulted in the signal conditioning circuit's output varying throughout its entire range. This meant that the output of the signal conditioning circuits were not usable while the sensor cables experienced any movement or physical disturbance. The solution for this project was to tie each sensor's cables together using spiral binding, thus limiting the movement and displacement of each sensor's cables with respect to each other. This provided enough cable stability to be able to take accurate measurements. A recommendation for future work and possible implementation of the sensor

driver system is to replace the ten single core cables of each sensor with one ten-core cable that is also externally shielded.

The sensitivity of the sensor driver circuit to cable movement can be explained by examining the impedance of the sensor cables during movement. An increase in distance between one cable and the other cables changes the impedance in that cable, therefore influencing the signal travelling in that cable. The change in the impedance of the sensor cable can be attributed to Faraday's law, given by (7.7)

$$\nabla \times E = -\frac{\partial B}{\partial t} \tag{7.7}$$

which states that the curl of the electrical field is equal to the rate of decrease of the magnetic field with time. This implies that a varying charge creates a magnetic field, which in turn results in an electric field when the magnetic field changes. By applying Faraday's law to the sensor cables, the change in impedance can for the most part be explained. Each cable encloses varying charges in the form of a high frequency sine wave, which results in a magnetic field surrounding the cable. Since the current flowing in the cable's conductor is not equal to the current flowing in the cable's shield, the magnetic field is not cancelled out [53]. When one cable is displaced in relation to another, the magnetic field surrounding the cable changes. This changing magnetic field in turn results in an external electric field that influences the electric field contained within the cable's conductor. Given that the impedance of the cable is the ratio of the electric field strength to the magnetic field strength, the changing electric field results in a change in the impedance of the cable as well.

Two major effects that must be investigated in future work regarding the sensor cables are signal leakage and ingress. Signal leakage can be described as the passage of electromagnetic fields through the shield of a cable, and ingress is the passage of an outside signal into the cable which can result in noise and disruption of the desired signal [54]. With regards to the sensor cables, the signal leakage of cable A produces ingress on cable B. The connection of the cable shield should also be investigated for optimal electromagnetic shielding. Figure 7-43 illustrates the sensor cable movement response for both sensor 1 and sensor 2 against the measured response when the cables are kept still.

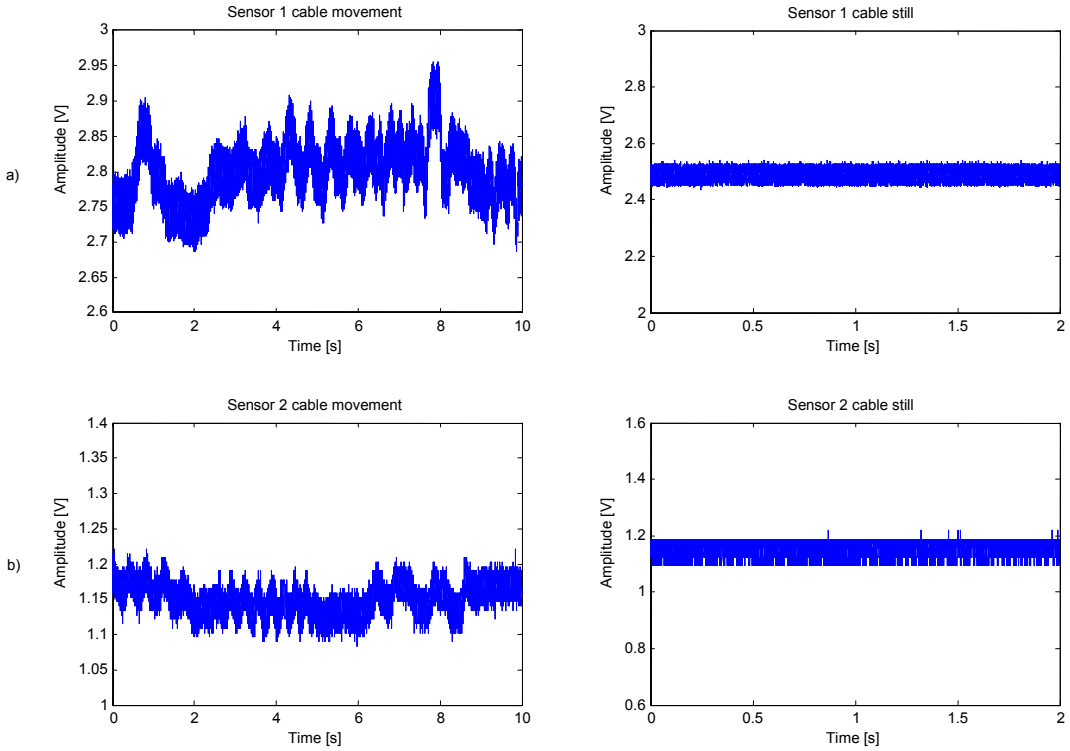


Figure 7-43 Sensor cable movement response for sensor 1 (a) and sensor 2 (b)

7.3.4 Board sensitivity

In order to obtain the desired output range for the signal conditioning circuits, the gains of the op-amps were adjusted using a constant amplitude 2.083 MHz sine wave from a signal generator as input. The amplitude of the sine wave was set to a maximum and minimum value corresponding to that measured on the previous PCB sensors used for the test circuit, namely 0.42 V minimum and 0.52 V maximum. The first signal conditioning circuit (x1) of sensor 1 was used as a template for the other signal conditioning circuits. After the gains of this circuit have been adjusted to result in an output signal range of ±3.8 V, the gain values were replicated for the other signal conditioning circuits. Even with an identical input signal applied to each signal conditioning circuit and identical gain values, the output signals still differed, with some stages of a few circuits even saturating while others did not.

As all other variables except the component placement, signal routing and component tolerances of these circuits were identical, the explanation for the difference in output signals must lie with these three variables. The component placement of the signal conditioning circuits

are not the same, with some components being mounted on the top layer while others are mounted on the bottom layer. The different mountings could contribute to the differing track lengths, as some signals are routed only in the top layer, while others are routed from the bottom layer to the top layer, therefore increasing the track length by at least the thickness of the board (2.4 mm).

The main explanation for the differing output values, however, is the large gain of the signal conditioning circuits (150 V/V), together with the tolerances of the components, especially the resistors. With each resistor used to set up the gain value of the op-amps having a tolerance of ±1 %, the total gain will be different for each circuit. For example, a +1 % deviation in the value of the first gain resistor of the signal amplifier circuit was calculated to result in a 0.1 V/V difference in the gain of the signal amplifier circuit. This means that it is not possible to obtain the same desired output from each circuit using fixed value resistors. This in turn implies that it is not feasible to use fixed value resistors to set the gain of all the amplifying stages of the circuit, especially the gain and scaling circuits, and that precision potentiometers should rather be used. This would allow the output values of the signal conditioning circuits to be adjusted more precisely, thereby also allowing for better utilization of the input range of the ADCs and improving the resolution of the sensor system.

7.4 Additional circuit characteristics

7.4.1 Signal to noise ratio

The signal to noise ratio is determined for a single axis of a sensor in order to obtain a general idea of the signal to noise ratio of the sensor system. This is only done to serve as a method of validation for the sensor system as a whole, and not as validation of the sensor system's requirement specifications. It is therefore assumed that the signal to noise ratio for the rest of the sensor system will be similar to that calculated for the single axis. The signal to noise ratio of the measured signal is determined by calculating the logarithm of the ratio of the signal power to the noise power. The signal power is calculated by taking the square of the signal range. The noise power is calculated by determining the square of the RMS noise value. During measurements it was noticed that the noise level of the signals varied with the displacement of the test rotor. The SNR is therefore calculated for increments of 100 µm rotor displacement.

The results are presented in Table 7-3.

Table 7-3 SNR measurements

Displacement (µm)	SNR (dB)
-200	55.5954
-100	54.6911
0	55.7814
100	54.0611
200	68.2521

As can be seen in Table 7-3, the measured signals showed good noise rejection with all the SNRs being greater than 50 dB. The worst-case scenario of 54 dB is used as the general signal to noise specification for the sensor system.

7.1.1 Sensor driver sensitivity and resolution

The sensitivity of the sensor driver is determined by dividing the output range of the signal by the displacement range of the test rotor. This is shown in (7.8).

$$S = \frac{output\ signal\ range}{total\ displacement} \tag{7.8}$$

$$= \frac{10.556\ \mathrm{V}}{400\ \mu\mathrm{m}}$$

$$= 26.39\ \mathrm{V/mm}$$

The requirement specification for the sensitivity of the sensor driver system was determined as 8 V/mm in chapter 3. The measured sensitivity for the sensor driver system is therefore more than three times better than that specified.

The average resolution of the sensor driver system is given as the minimum change in input signal (displacement) that can be detected by the sensor driver system in order to produce a change in output. The resolution is calculated by measuring the worst-case noise amplitude and multiplying it with the inverse of the sensitivity.
The equation used to determine the average resolution of the sensor driver system is shown in (7.9).

$$\begin{aligned} \text{Resolution} &= \frac{Noise}{Sensitivity} \\ &= \frac{0.020914\ \text{V}}{26.39\ \text{V/mm}} \\ &= 792.5\ \text{nm} \end{aligned} \tag{7.9}$$

The general resolution of the sensor driver system can therefore be approximated to 800 nm, which is more than sufficient for use in the control of an AMB system.

7.1.2 Thermal analysis

Due to the fact that the final sensor driver board cannot be tested for temperature stability over a varying temperature range, a thermal analysis of the board at it's normal operating temperature is performed instead. This thermal analysis documents which components are operating beyond 50 % of their rated maximum operating temperature, indicating that the power consumption of those components are higher than desired. Although the operating temperature of these components may be higher than desired, none of them are above 90 % of their maximum operating temperature and showed no signs of malfunctioning during operation as a result of the higher operating temperature. It is recommended that the power consumption and heat regulation of these component be investigated and improved in future work for better overall power consumption of the sensor driver board.

The thermal analysis diagram of the sensor driver board is shown in Figure 7-44, with the components situated on the top layer indicated in red, and the components situated on the bottom layer indicated in blue. The numbering of the components in the figure corresponds to that of Table 7-4, which lists the components exceeding their desired operating temperature along with the maximum operating temperatures for these components.

Table 7-4 Thermal analysis of components

No.	Components	Max operating temperature (ºC)	Possible explanation
1	TL750M05 regulators	125	Current output near maximum capability
2	UA7905 regulators	125	Current output near maximum capability
3	AD8099 op-amps	125	High gain output with insufficient heat-sinking
4	LT1568 BPFs	85	Low value resistors resulting in high currents
5	LM7372 op-amps	85	High current output with insufficient heat-sinking

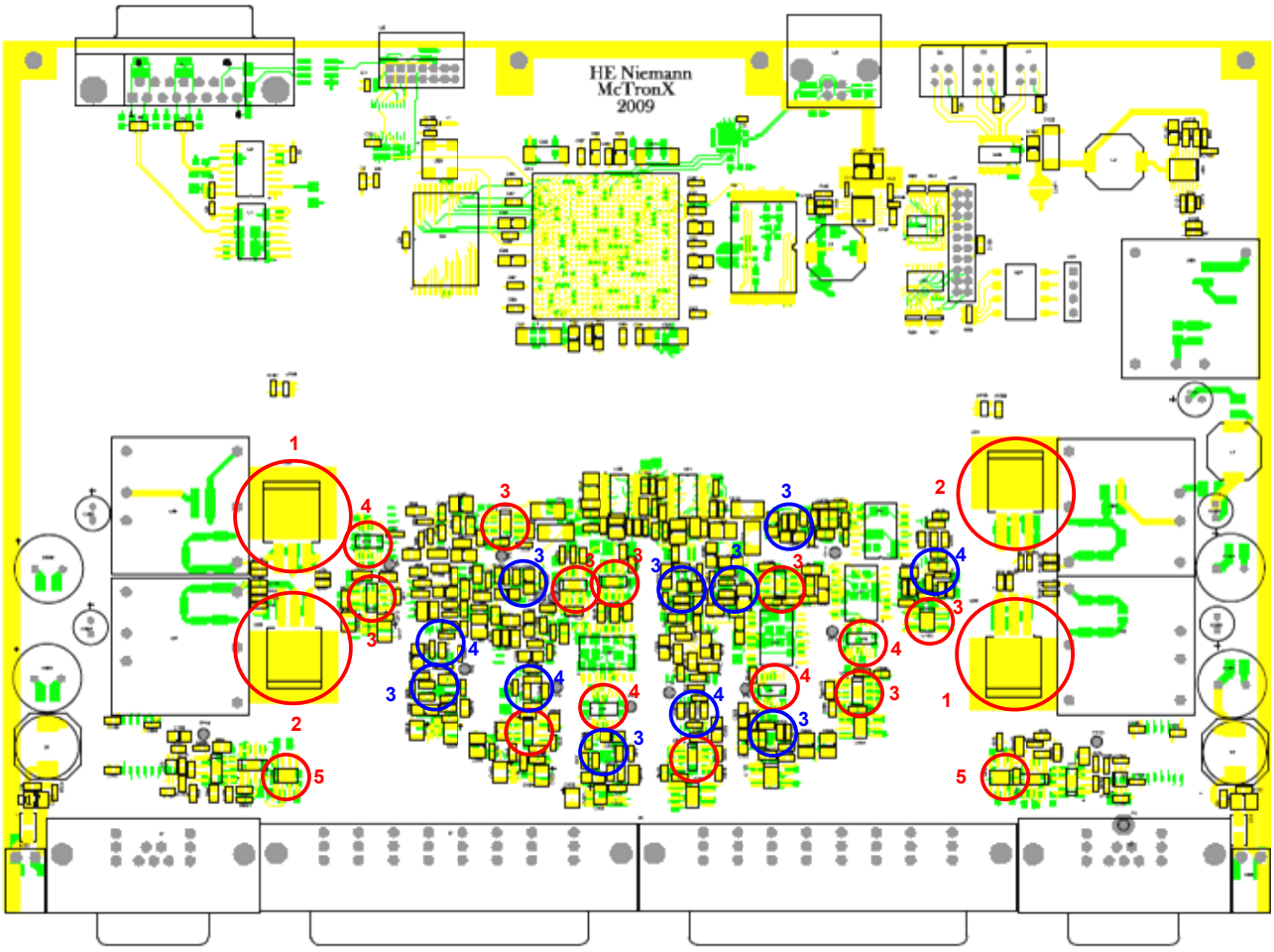


Figure 7-44 Thermal analysis of the sensor driver board.

Table 7-5 Component temperature measurements

	Sensor 1			Sensor 2	
Circuit	**Component**	**Temperature (ºC)**	**Circuit**	**Component**	**Temperature (ºC)**
Excitation 1			Excitation 1		
	AD8099	62.1		AD8099	62.6
	LM7372	66.3		LM7372	71.7
Signal conditioning 1			Signal conditioning 5		
	AD8099 (1)	65.8		AD8099 (1)	65.4
	LT1568	65.6		LT1568	64.5
	AD8099 (2)	66		AD8099 (2)	66.1
Signal conditioning 2			Signal conditioning 6		
	AD8099 (1)	66.1		AD8099 (1)	65.6
	LT1568	65.8		LT1568	62
	AD8099 (2)	65.7		AD8099 (2)	64.2
Signal conditioning 3			Signal conditioning 7		
	AD8099 (1)	62		AD8099 (1)	64.9
	LT1568	61.3		LT1568	66.6
	AD8099 (2)	60		AD8099 (2)	42
Signal conditioning 4			Signal conditioning 8		
	AD8099 (1)	64.2		AD8099 (1)	68.5
	LT1568	63.4		LT1568	66.5
	AD8099 (2)	63.8		AD8099 (2)	67.1
Power supply 1			Power supply 2		
	TL750M05	91.6		TL750M05	86.7
	UA7905	85.3		UA7905	88.4

Table 7-5 shows the measured temperatures of the individual components during normal operation of the sensor driver board at room temperature. These measurements confirm that these components are operating beyond the desired 50 % of their maximum operating temperatures, but that none of them are beyond 90 %. This indicates that all the components are still operating well within their safe operating ranges. It is however still recommended that the heat dissipation of the board be reduced, especially if the sensor driver system is to be implemented in an environment with a higher ambient temperature. Further investigation on this aspect should be conducted.

7.2 Conclusion

All the results obtained from the constructed circuits of the sensor driver were provided in this chapter. The oscillator test circuit was used to verify and select the best circuit design for the oscillator circuit to be implemented in the excitation circuit of the sensor driver. The sensor driver test circuit was used to verify the design concept of the sensor driver circuit, containing an excitation circuit, signal conditioning circuit and a power supply circuit. The results obtained from this circuit lead to the design of the final sensor driver board. The final sensor driver board was the main hardware deliverable of this project. This final circuit board was used to verify the digital circuit design, and the design of the sensor driver as a whole. The final sensor driver board was also used to validate the sensor driver system with regards to its set requirement specifications, as well as its performance in general. Some additional circuit characteristics and sensitivities that had an effect on the measurements taken were discussed and recommendations were made.

Chapter 8

Conclusion and recommendations

This chapter provides a summary of the conclusions made regarding all the main components of the sensor driver system. Recommendations regarding unresolved problems discovered during evaluation of the sensor driver are also given with regards to possible future work on the sensor driver project.

8.1 Conclusion

This project entailed the design and development of a high precision driver for an eddy current displacement sensor. The sensor driver supplemented and completed a PCB eddy current displacement sensor system. The main focus of the sensor driver design was on high accuracy and temperature stability of the electronic driver circuit.

In order to realize the functionality of the sensor driver, the design was divided into an analogue- and digital circuit. The analogue circuit of the sensor driver consisted of power supply circuits, excitation circuits, and signal conditioning circuits. The digital circuit of the sensor driver consisted of an FPGA processor, flash programming circuit, USB interface circuit, digital power supply circuit, and communication circuit.

The requirement specifications of the sensor system formed the basis of the system design to follow, and therefore constituted one of the main components of the project. The analogue design of the sensor driver formed the main field of study for the project, and can be considered the key component of the project. The circuit design of the digital circuit and the integration thereof with the analogue circuit was another main component of the project, leading to the final sensor driver board. The final sensor driver board constituted the hardware deliverable of the project. Conclusions for each of these main project components will now be given.

8.1.1 Sensor system requirement specifications

The requirement specifications for the sensor driver system were acquired by first researching and investigating the existing commercially available eddy current sensors, especially those used for research purposes within the research group. A functional analysis of the system was performed, followed by a functional allocation of the sensor system. Affine arithmetic was then used to obtain the requirement specifications for all the functional units of the sensor driver with regards to its performance parameters. These specifications were then used as the determining factor in the component selection process of the analogue design.

8.1.2 Sensor driver analogue design

The analogue design of the sensor driver system constituted the main design aspect of the project. The performance of the analogue system also directly determined the performance of the sensor driver system, and the choice of design had to be carefully considered. Various designs were therefore considered for each functional unit in order to select the most suitable one that adhered to the requirement specifications set for that functional unit. After a design had been chosen for a functional unit, an estimate for its performance parameters were calculated in order to verify that design with regards to the requirement specifications. In order to verify one of the key components of the excitation circuit, namely the oscillator circuit, an oscillator test circuit with three different circuit designs was designed, constructed and evaluated in order to decide on the best oscillator for implementation in the sensor driver circuit. The design concept of the sensor driver system was also verified by designing, constructing and evaluating a sensor driver test circuit. This test circuit consisted of a power supply circuit, excitation circuit and two signal conditioning circuits, and was connected to a single PCB sensor. The successful verification of the sensor driver design concept meant that the design for the final sensor driver board could commence.

8.1.3 Sensor driver digital circuit

The design of the digital circuit with regards to component selection and schematic design was done with the help of the iSensor design [26]. The circuit layout was also based on the circuit layout of the iSensor, but was altered to correspond to the sensor driver circuit with regards to component placement and signal routing. The signal routing between the FPGA and other components were especially critical. This is due to the fact that the very high frequency digital signals require track lengths to be as short as possible in order to avoid it reacting like

transmission lines. For the signal routing of differential signals it was essential to keep their track lengths as similar as possible. Since firmware design was not the focus of this project, it was based on that of the iSensor since the digital circuits were very similar in design and function. The integration of the digital circuit with the analogue circuit completed the final sensor driver circuit board

8.1.4 Final sensor driver

The final sensor driver board constituted the main hardware deliverable of the project. It was capable of driving two radial PCB eddy current sensors and of conditioning and processing their output signals. The final sensor board comprised a ten-layer PCB, which included four ground layers, two power layers and four signal layers. The sensor driver's analogue circuit provided each sensor with a power supply circuit, excitation circuit, four signal conditioning circuits and two ADCs. An alteration was made to the V/I converters of the excitation circuits in order for them to be able to generate the desired output signals. This alteration was discussed in chapter 6. The digital circuit was responsible for digitally filtering the output values of the ADCs before performing differential position extraction on the signals. The signals were then compensated so that the range of their position output was situated around zero. The linearization of the position output signals could not be realized on the FPGA itself due to timing constraint problems. Recommendations regarding this issue are given in the next section.

The main objective with the final sensor driver board was to verify the digital circuit design as well as the integrated sensor driver design as a whole. Another objective of the board was to validate the sensor driver system with regards to the requirement specifications set and the estimates determined for it, as well as its performance in general. The linearity of each axis of the sensor driver system met the required linearity specification of 17.5 % FSO. The worst linearity measured was that of the second sensor's y-axis, and was calculated as 9.23 % FSO. The signal to noise ratio of the sensor system in general was calculated as 54 dB, which indicated that the sensor driver system possessed good noise rejection properties. The sensor system also possessed excellent sensitivity of 26.39 V/mm, which was three times the sensitivity specified. The general resolution of the sensor system was calculated as 800 nm, which was also more than adequate. The performance parameters of the sensor driver system were in general very satisfactory.

8.2 Recommendations

This section presents recommendations for the improvement of the sensor driver system. All of these recommendations are possible without redesigning the sensor driver, and can be accomplished with either small firmware or hardware alterations. Due to time and budget constraints these improvements could not be implemented on the sensor driver system during this project.

8.2.1 Cables

The effects of cable movement were discussed in chapter 7. In order to significantly reduce these effects, it is recommended that the single core cables be replaced with multi-core cables. The displacement of the individual cables with regards to each other will then be eliminated.

8.2.2 Temperature improvements

The thermal analysis of the sensor driver board was done in chapter 7, section 7.4.3. The components of which the operating temperature was higher than 50 % of its rated operating temperature were identified. These were the AD8099 op-amp, LM7372 op-amp, LT1568 filter building block, TL750M05 regulator, and the UA7905 regulator. It is recommended that the heat dissipation of the circuit be reduced, and the heat distribution of these components be improved. This can be achieved by mounting a fan to the sensor driver board, or by fixing heat-sinks to the components. If the sensor driver board is reproduced, larger thermal pads beneath the components should be provided.

8.2.3 Linearization algorithm

The linearization of the position signals could not be implemented on the FPGA due to timing constraints that were not met. One recommendation to possibly resolve this problem is to rewrite the linearization algorithms in order to optimize the code for execution within the time constraint of the FPGA.

8.2.4 Low-pass filter on FPGA

In order to improve the SNR of the sensor driver system, it is recommended that the attenuation of the low-pass filter of the FPGA be increased by increasing the order of the filter used. The bandwidth-effects of the filter must also be investigated.

8.3 Future work

This section presents suggestions for future work on the sensor driver. These are suggestions that require modifications to either the hardware or software design of the sensor driver system.

8.3.1 MicroBlaze linearization implementation

The implementation of the linearization algorithm can be more effectively done by implementing the MicroBlaze processor core on the FPGA. MicroBlaze is a 32-bit soft processor or IP core that is implemented using the logic primitives of the FPGA. It has a RISC Harvard architecture with a rich instruction set that is optimized for embedded applications. The major advantage that the MicroBlaze will bring to this project is the fact that it has an optional integrated Floating-Point Unit (FPU). Floating point acceleration will create a significant improvement in the time constraints of the FPGA, making it possible to implement the linearization algorithm on the FPGA.

8.3.2 Cable and EMC effects

The effects of cable movement need to be investigated further, and more permanent and secure solutions need to be found and implemented. The effects of external electro-magnetic fields on the sensors and cables also need to be investigated further in detail to obtain an understanding of what kind of shielding of the sensor driver system would be sufficient. Standards for EMC also need to be identified and implemented on the sensor driver in order to make it suitable for use in industrial applications and environments.

8.3.3 Input signal testing for FPGA

The reliability of the sensor driver can be improved by providing a test-function for the input signals of the FPGA. The test-function will introduce fault-finding in the sensor system by determining which signal is faulty and alerting the user by means of a signal transmission to the main controller or the SCADA user interface. The distinction between an electronic fault on the sensor driver and a fault on the sensor itself must also be made.

8.3.4 Temperature compensation

The behaviour of the sensor with regards to temperature variation needs to be investigated further in order to determine if temperature compensation of the position signal is necessary. If it is deemed necessary, position measurements must be taken with the sensor at various set temperatures. A fitting function for the measured signals at each temperature must then be determined. A temperature sensor is also need to be installed on the sensor in order to measure the temperature at the sensor itself. This temperature measurement must then also be sent to the ADCs of the sensor driver and read into the FPGA. Depending on the temperature of the sensor, a corresponding compensation function will be implemented on the measured position signals to obtain linear position outputs. These linear position outputs will then be the same regardless of the temperature of the sensor.

8.3.5 Optimal sensor operation

The optimal operation of the sensor needs to be investigated in detail with regards to the excitation current. The optimal excitation current will produce the largest differential position signals from the sensing coils of the PCB sensor. If the sensor operates at its optimum, its sensitivity and resolution may be improved.

8.3.6 System implementation on test bench

Due to the fact that the sensor driver system was only implemented on a static test set-up, dynamic testing could not be performed. The dynamic characteristics of the sensor driver system could therefore not be determined. Further study on the sensor driver should therefore include implementation of the sensor driver system on a test bench capable of testing the bandwidth specifications of 10 kHz, as well as testing other dynamic characteristics.

8.4 Closure

The aim of this project was to design and develop a high precision driver for an eddy current displacement sensor. The project had been initiated to supplement the development of a low-cost PCB eddy current displacement sensor for AMBs.

The main focus of this project was the development of an eddy current sensor driver with high accuracy and temperature stability. It entailed the design and development of the electronic circuit necessary to drive the sensor, as well as the signal conditioning circuit, and also entailed the design of the digital signal processing to be done on an embedded digital controller.

The sensor driver consisted of several sub-systems, including a sensor excitation circuit, the PCB eddy current sensor, a signal conditioning circuit, and the digital processing circuit. The analogue design of the sensor driver formed the main study field for this project, as the implementation of the electronic circuits determined the success of the sensor driver.

The evaluation of the sensor driver indicated that the SNR of the sensor driver was satisfactory, with all the measured signals having a SNR greater than 50 dB, with the worst SNR being 54 dB. The linearity of the uncompensated measured signals was very satisfactory, with the worst linearity being around 9 %, which is an improvement of a factor of almost two to the measured linearity of the commercial eddy current sensors. The sensitivity of the sensor driver system is also three times that of the specified sensitivity. The resolution of the sensor driver system was determined as 792.5 nm, which was better than expected.

The overall outcome of the sensor driver project was exceedingly successful, with all the characteristics of the sensor driver adhering to the set requirement specifications. Both the sensor driver design and the sensor driver board was successfully verified and validated.

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Appendix A

Data CD

- Test circuit
  - Test_circuit.DBK
  - Test_circuit.DSN
  - Test_circuit.mrk
  - Test_circuit.opj
  - Layout.log
  - TEST_CIRCUIT_LAYOUT.MAX
- Final sensor driver schematics
  - Final_sensor_driver_schematic.pdf
  - Final_sensor_driver_schematics_Altium
- Conceptual layout
  - Conceptual_layout.vsd
- Final layout
  - Final_layout.pdf
  - Final_layout_Altium
- Photos
  - 1. Oscillator circuits
  - 2. Test circuit
  - 3. Final sensor driver
  - 4. Evaluation setup