

Development of an integrated co-processor based power electronic drive

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By

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DECLARATION

I hereby declare that all the material incorporated in this thesis is my own original unaided work except where specific reference is made by name or in the form of a numbered reference. The work herein has not been submitted for a degree at another university.

Signed:

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SUMMARY

The McTronX research group at the North-West University is currently researching self-sensing techniques for Active Magnetic Bearings (AMB). The research is part of an ongoing effort to expand the knowledge base on AMBs in the School of Electrical, Electronic and Computer Engineering to support industries that make use of the technology. The aim of this project is to develop an integrated co-processor based power electronic drive with the emphasis placed on the ability of the co-processor to execute AMB self-sensing algorithms.

The two primary techniques for implementing self-sensing in AMBs are state estimation and modulation. This research focuses on hardware development to facilitate the implementation of the modulation method. Self-sensing algorithms require concurrent processing power and speed that are well suited to an architecture that combines a digital signal processor (DSP) and a field programmable gate array (FPGA). A comprehensive review of various power amplifier topologies shows that the pulse width modulation (PWM) switching amplifier is best suited for controlling the voltage and current required to drive the AMB coils. Combining DSPs and power electronics to form an integrated co-processor based power electronic drive requires detail attention to aspects of PCB design, including signal integrity and grounding.

A conceptual design is conducted and forms part of the process of compiling a subsystem development specification for the integrated drive, in conjunction with the McTronX Research Group. Component selection criteria, trade-off studies and various circuit simulations serve as the basis for this essential phase of the project. The conceptual design and development specification determines the architecture, functionality and interfaces of the integrated drive. Conceptual designs for the power amplifier, digital controller, electronic supply and mechanical layout of the integrated drive is provided.

A detail design is performed for the power amplifier, digital controller and electronic supply. Issues such as component selection, power supply requirements, thermal design, interfacing of the various circuit elements and PCB design are covered in detail. The output of the detail design is a complete set of circuit diagrams for the integrated controller.

The integrated drive is interfaced with existing AMB hardware and facilitates the successful implementation of two self-sensing techniques. The hardware performance of the integrated co-processor based power electronic drive is evaluated by means of measurements taken from this experimental self-sensing setup. The co-processor performance is evaluated in terms of resource usage and execution time and performs satisfactorily in this regard.

The integrated co-processor based power electronic drive provided sufficient resources, processing speed and flexibility to accommodate a variety of self-sensing algorithms thus contributing to the research currently underway in the field of AMBs by the McTronX research group at the North-West University.

Keywords

Active magnetic bearing, co-processor, digital signal processor, field programmable gate array, power amplifier, pulse width modulation, self-sensing, signal integrity.

OPSOMMING

Die McTronX navorsingsgroep by die Noordwes Universiteit doen tans navorsing op selfwaarnemingstegnieke vir Aktiewe Magnetiese Laers (AMLs). Die navorsing is deel van 'n deurlopende poging om die kundigheidsbasis op AMLs binne die Skool vir Elektriese, Elektroniese en Rekenaaringenieurswese uit te brei om industrieë wat van die tegnologie gebruik maak, te ondersteun. Die doel van die projek is die ontwikkeling van 'n geïntegreerde hulpverwerker-gebaseerde drywingselektroniese omsetter waar die klem geplaas word op die vermoë van die hulpverwerker om selfwaarnemingsalgoritmes vir AMLs uit te voer.

Die twee primêre tegnieke vir die implementering van selfwaarneming in AMLs is toestandskatting en modulasie. Hierdie navorsing fokus op hardeware-ontwikkeling om die implementering van die modulasietegniek te fasiliteer. Selfwaarnemingsalgoritmes vereis parallelle verwerkingsvermoë en spoed; 'n behoefte wat goed aangespreek word met 'n argitektuur wat 'n digitale seinverwerker (DSV) en 'n veld-programmeerbare hekmatraks (VPHM) kombineer. 'n Omvattende oorsig van verkeie drywingsomsettertopologieë toon dat die pulswydte modulasie (PWM) skakelmodusversterker die mees geskikte omsetter is om die spannings en strome van AML spoel te beheer. Die kombinasie van DSVs en drywingselektronika om 'n geïntegreerde hulpverwerker-gebaseerde drywingselektroniese omsetter te vorm, verg dat spesifieke aandag gegee moet word aan aspekte van etsbaanontwerp, seinintegriteit en be-aarding.

'n Konsepontwerp is gedoen en vorm deel van die proses om 'n substelsel ontwikkelingspesifikasie vir die geïntegreerde omsetter saam te stel in samewerking met die McTronX navorsingsgroep. Komponentseleksiekriteria, vergelykende studies en verskeie stroombaansimulasies vorm die basis vir hierdie essensiële fase van die projek. Die konsepontwerp en ontwikkelingspesifikasie bepaal die argitektuur, funksionaliteit en intervlakke van die geïntegreerde omsetter. Konsepontwerpe van die kragversterker, digitale beheerder, elektroniese toevoer en meganiese uitleg van die geïntegreerde omsetter word gegee.

'n Detail ontwerp word gedoen vir die kragversterker, digitale beheerder en elektroniese toevoer. Aspekte soos komponentseleksie, kragtoevoerbehoefte, termiese ontwerp, koppeling van die verskillende stroombaanelemente en etsbaanontwerp word in detail bespreek. Die uitset van die detail ontwerp is 'n volledige stel stroombaandiagramme vir die geïntegreerde beheerder.

Die geïntegreerde omsetter word geïntegreer met bestaande AML hardeware en fasiliteer die implementering van twee selfwaarnemingstegnieke. Die gedrag van die geïntegreerde

hulpverwerker-gebaseerde drywingselektroniese omsetter word ge-evalueer deur middel van metings op die eksperimentele opstelling. Die gedrag van die prosesseerder word ge-evalueer in terme van hulpbronaanwending en verwerkingstyd en die gedrag is bevredigend.

Die geïntegreerde hulpverwerker-gebaseerde drywingselektroniese omsetter het voldoende hulpbronne, verwerkingspoed en buigbaarheid voorsien om 'n verskeidenheid selfwaarnemingsalgoritmes te akkommodeer. Die projek het dus sinvol bygedra tot die navorsing wat gedoen word op AMLs in die McTronx navorsingsgroep aan die Noordwes Universiteit.

Sleutelwoorde

Aktiewe magnetiese laer, hulpverwerker, digitale seinverwerker, veld-programmeerbare hekmatriks, kragversterker, pulswydte modulasie, selfwaarneming, seinintegriteit.

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"The gift of mental power comes from God, Divine Being, and if we concentrate our minds on that truth, we become in tune with this great power. My mother had taught me to seek all truth in the Bible."

Nikola Tesla (1856-1943)

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LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog-to-Digital-Converter
AM	Amplitude Modulation
AMB	Active Magnetic Bearing
ARCNET	Attached Resource Computer Network
BGA	Ball Grid Array
BPF	Band Pass Filter
CAN	Controller Area Network
CLB	Configurable Logic Block
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DAC	Digital-Analog-Converter
DC	Direct Current
DCM	Digital Clock Manager, Direct Current Measurement
DOF	Degree-of-Freedom
DPR	Dual Port RAM
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESR	Equivalent series resistance
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IIR	Infinite Impulse Response
JTAG	Joint Test Action Group
Kbps	Kilo bits per second
LPF	Low Pass Filter
LVC MOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signaling
LVTTL	Low Voltage Transistor-Transistor Logic
MAC	Multiply and Accumulate
Mbps	Mega bits per second
McBSP	Multi-channel Buffered Serial Port

List of Abbreviations

MIPS	Million Instructions Per Second
MLC	Multi-layer ceramic
MLP	Multi-layer polymer
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PBMR	Pebble Bed Modular Reactor
PCB	Printed Circuit Board
POR	Power On Reset
PWM	Pulse Width Modulation
ROM	Read Only Memory
SPI	Serial Peripheral Interface
SVPWM	Space Vector Pulse Width Modulation
TCK	Test Clock
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select
TRST	Test Reset
UART	Universal Asynchronous Receiver Transmitter
XPE	XPower Estimator

LIST OF SYMBOLS

A_e	Effective core area	[m ²]
A_g	Cross sectional area of air gap	[m ²]
B	Magnetic flux density	[T]
C	Capacitance	[F]
D	Duty cycle	
E	Energy	[J]
f	Frequency	[Hz]
F	Electromagnetic force	[N]
g	Nominal air gap	[m]
$H(s)$	Analog transfer function	
$H(z)$	Digital transfer function	
i	Instantaneous current	[A]
I	Current	[A]
$\hat{I}$	Peak current	[A]
k	Thermal conductivity	[W/m °C]
L	Inductance	[H]
ℓ_c	Magnetic path length of core	[m]
ℓ_g	Magnetic path length of gap	[m]
ℓ_{rise}	Length of signal rising edge	[cm]
N	Number of turns	
P	Power dissipation	[W]
Q	Electric charge	[C]
R	Electrical resistance	[Ω]
$\mathfrak{R}_c$	Core material reluctance	[H ⁻¹]
$\mathfrak{R}_g$	Air gap reluctance	[H ⁻¹]
$\mathfrak{R}_t$	Total reluctance	[H ⁻¹]
R_Θ	Thermal resistance	[°C/W]
t_{rise}	Signal rise time	[s]
T_s	PWM switching period	[s]
T	Temperature	[°C]

List of Symbols

τ	Time constant	[s]
v	Instantaneous voltage	[V]
V	Voltage	[V]
$\vec{V}$	Voltage vector	[V]
ϕ	Magnetic flux	[Wb]
ε_0	Permittivity of free space	[V.m]
ε_r	Relative permittivity of material	
μ_0	Permeability of free space	[H/m]
μ_r	Relative permeability of material	
x	Change in air gap length	[m]

Chapter 1

Introduction

This chapter provides background information on the active magnetic bearing (AMB) principle, self-sensing, signal processing, algorithm requirements and power amplifiers. The problem statement, issues to be addressed and the research methodology are also stated. Finally, the layout of the document is presented.

1.1 Background

Active magnetic bearings (AMBs) provide low loss, maintenance free magnetic levitation in applications such as vacuum pumps, blood pumps, machine tool spindles, electric drives and flywheel energy storage systems, to name a few. Contact free rotation is the main advantage of AMBs and this allows for high rotational speed without lubrication or mechanical wear. Active control of the AMB allows dynamic tuning of rotor characteristics such as damping and stiffness. The AMB is classified as a mechatronic device due to the combination of electrical, mechanical and software components.

The McTronX research group at the North-West University is currently researching self-sensing techniques for Active Magnetic Bearings (AMB). The research is part of an ongoing effort to expand the knowledge base on AMBs in the School of Electrical, Electronic and Computer Engineering to support industries that make use of the technology. AMB technology is currently being considered by PBMR for the next generation nuclear reactor.

1.1.1 Active magnetic bearing principle

The AMB consists of four basic components; a magnetic actuator, controller, power amplifier and a position sensor [1]. A simple, one degree-of-freedom (DOF) AMB is shown in Figure 1-1. The position sensor measures the displacement between the rotor and the electromagnet. The controller determines the error in the rotor position and issues a control command to the power amplifier. The power amplifier generates the drive current required by the electromagnet to establish the magnetic force that stably suspends the rotor in the desired position.

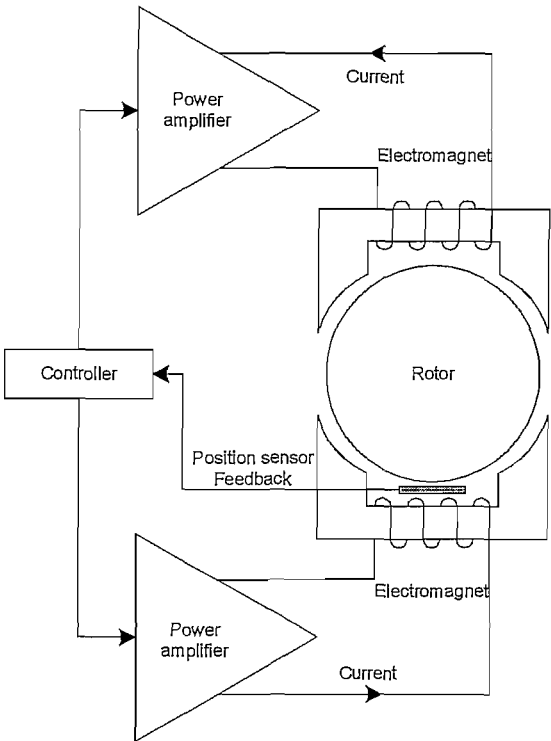


Figure 1-1 Basic AMB

1.1.2 Self sensing

The conventional AMB requires a position sensor to determine the rotor position. Instead of using a position sensor, a self-sensing AMB derives the rotor position information from the current and voltage signals that drive the electromagnet as shown in Figure 1-2 [2].

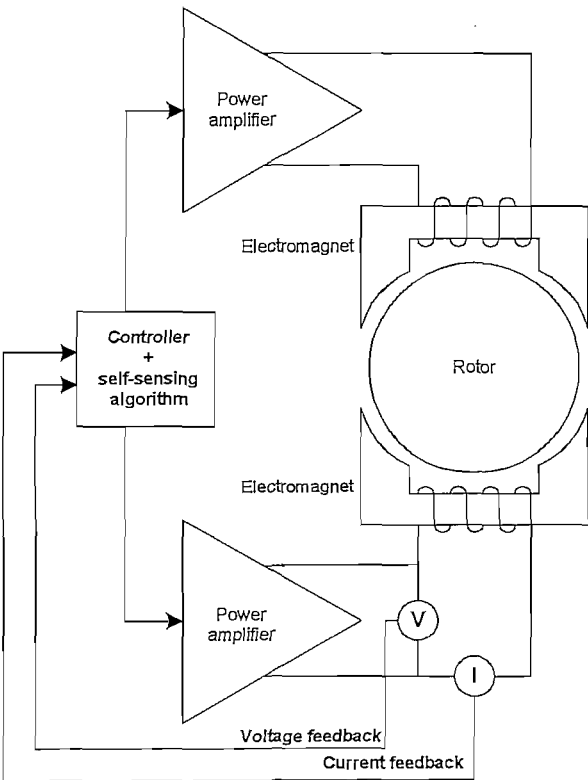


Figure 1-2 Self-sensing AMB

The advantages of self-sensing are a higher level of system integration, reduced cost, increased reliability and the ability to use the AMB in a harsher environment than would have been possible with position sensors. Self-sensing can be divided into two main categories namely state estimation and modulation [3]. More detail regarding self-sensing approaches are contained in section 2.2.

1.1.3 Signal processing

Implementation of modulation based self-sensing requires real time, high speed, computationally intensive digital signal processing of the measured current and voltage. The current and voltage signals have to be demodulated so that the necessary position information can be extracted [3]. An analog synchronous demodulator may be implemented before the current and voltage signals are sampled by an analog-to-digital-converter (ADC) for further processing by the self-sensing algorithm in the digital domain. Alternatively the current and voltage signals may be ADC sampled immediately with all subsequent demodulation functions performed in the digital domain. Demodulation in the digital domain provides more flexibility with options to directly synthesize the analog demodulator or use Fast Fourier Transform (FFT) and synchronous sampling techniques. The signal processing power and speed that are required to implement self-sensing can be gauged by assessing the algorithm requirements.

1.1.4 Algorithm requirements

Conventional signal processing functions such as Finite Impulse Response (FIR) filters, Infinite Impulse Response (IIR) filters and FFT's are used to implement the self-sensing algorithm. These functions are solved by repeating a number of multiply and accumulate (MAC) operations that can be executed by a DSP in a single instruction cycle [4]. The approximate computational intensity necessary to perform the self-sensing algorithm can be estimated by counting the DSP instruction cycles required to execute the various functions. Table 1-1 summarises the self-sensing algorithm requirements.

Table 1-1 Self-sensing algorithm requirements

Function	Order	MAC's	Function occurrences	Instruction cycles
IIR	2 nd	5	2	10
FIR	100 th	100	8	800
FFT	512 point	60 000	2	120 000
Nonlinear	4 th	12	1	12

For a 150 MIPS DSP the clock cycle time is 6.67 ns. At a typical data sample rate of 50 μ s the DSP will be able to execute approximately 7500 instruction cycles, which represents only 6% of

the required processing power. This clearly indicates the need for a co-processor to increase the computational throughput. The FPGA is an ideal choice as a co-processor since it excels in the area of multiple instantiation of functions such as FFT, FIR and IIR.

1.1.5 Power amplifier

The choice of power amplifier topology is an important consideration in the design of an AMB system since it plays a critical role in AMB performance. Design issues to consider are efficiency, slew rate and electromagnetic compatibility (EMC). Two types of power amplifiers are primarily used in AMB applications; the linear amplifier and the switching amplifier, of which the switching amplifier is most common. Each of these topologies has their associated advantages and disadvantages. The linear amplifier is very precise and doesn't generate any electromagnetic interference (EMI), however it is grossly inefficient. The switching amplifier is highly efficient and thus more compact but generates considerable EMI due to pulse width modulation (PWM) switching. Since PWM is also a requirement of the self-sensing algorithm, a switching amplifier is considered the appropriate choice of power amplifier. Figure 1-3 shows a switching amplifier configuration commonly used in AMB applications, two of which are necessary to suspend an AMB in one DOF.

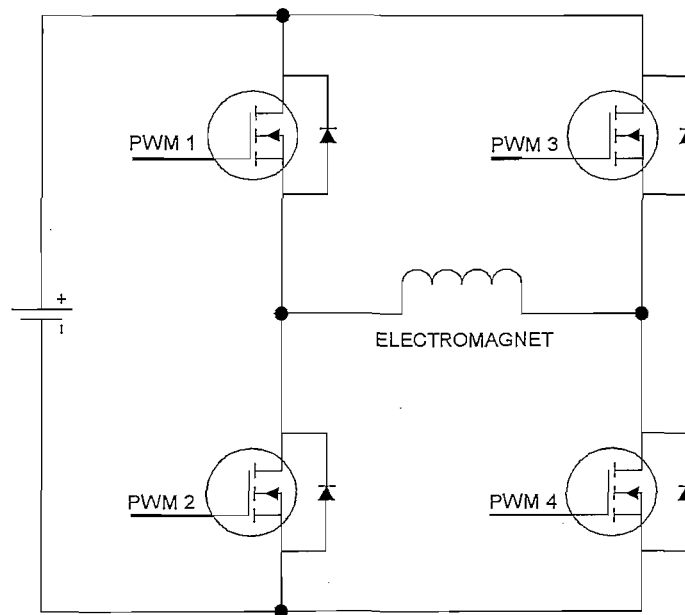


Figure 1-3 Switching amplifier

1.1.6 PCB design

The development of an integrated power electronic drive requires a combination of high speed digital circuitry, low noise analog signal conditioning and switching power electronics that requires careful attention to printed circuit board (PCB) design in order to minimize EMI and guarantee signal integrity.

1.2 Problem statement

The purpose of this project is to develop an integrated co-processor based power electronic drive, suitable for implementing self-sensing AMB techniques. To this end, a subsystem development specification was prepared by members of the McTronX research group to specify the required functional architecture of the integrated controller. The primary components of the integrated controller are analogue interface circuitry, digital control circuitry and power amplifiers.

1.3 Issues to be addressed and methodology

In order to successfully develop the integrated power electronic drive the development specification from the McTronX research group has to be analysed in detail to determine the architecture, interfaces and functional capability of the integrated drive. A comprehensive review of the related literature will also be completed before the system design is started. This information will be used to conduct the system design that will identify suitable components and topologies for the integrated drive. The system design will be followed by a detail design of the integrated drive hardware, including the PCBs. Component selection criteria, trade-offs and various circuit simulations of these primary components form the basis of the design of the integrated drive. Signal integrity and high-speed printed circuit board (PCB) design issues will also be addressed during the design process. Implementation of the design will involve ordering the components, building and testing the hardware, including integration with a magnetic bearing. After system integration has been successfully completed, the integrated controller will be verified according to measurements taken from an experimental self-sensing setup.

1.3.1 Literature study

The literature study will involve identifying, locating and evaluating potentially useful information sources. This information will help identify suitable components and topologies for the system design as well as the detail design of the integrated drive. The study will also provide an insight into current technology trends and similar existing work. Topics covered by the literature search will include self-sensing AMBs, digital signal processors, power electronic drives and high speed PCB design.

1.3.2 System design

Here the emphasis will be to identify the circuit architectures and topologies best suited to meet the specification. A thorough analysis of the system specification is a fundamental aspect of the system design. This is the key to establishing the required architecture, interfaces and

functional capability of the integrated drive. Various circuit simulations will also be done, using PSpice®, as part of the system design.

1.3.3 Design implementation

The design implementation will commence with a detail design that will concentrate on component level aspects of the digital circuitry and the power amplifier circuitry, including the PCB design. Issues to be addressed during this phase of the development will include specific component selection based on trade-off studies, device features and thermal considerations. Detail design of the PCBs will include identification of the optimal layer structure and routing of the PCB's to guarantee signal integrity.

The manufacturing drawings for the various PCBs will be submitted for quotations and the components will be ordered. The analog, digital and power amplifier PCBs that make up the integrated controller will be built-up and tested in-house. The functionality of the various sub-assemblies will be tested individually before combining them to form the integrated controller. Software must be written for the signal processors to enable appropriate testing of the digital PCB. The development of this software is beyond the scope of this dissertation. Once the integrated controller is functional, it will be integrated with a magnetic bearing in a self-sensing experimental set-up for design verification purposes.

1.3.4 Design verification

The performance of the integrated co-processor based power electronic drive will be evaluated in terms of hardware measurements and system performance. The various sub-systems that constitute the integrated co-processor based power electronic drive will be evaluated individually before the system performance is considered. The hardware measurements will be taken from an integrated co-processor based power electronic drive in a 1 DOF self-sensing experimental setup.

Since the integrated drive will be used as a platform to investigate and further research self-sensing, results obtained from such research will also be included in the evaluation of the integrated drive.

1.4 Overview of the dissertation

This section contains a brief overview of the remaining chapters of this dissertation.

Chapter 2 documents the study of the related literature. Topics covered by the literature search will include self-sensing AMBs, digital signal processors, power electronic drives and high speed PCB design.

In Chapter 3 the specification is analysed in order to determine the architecture, interfaces and functional capability of the integrated drive. Identification of suitable components and topologies form the basis of the system design process. Various circuit simulations will also be presented in this chapter.

Chapter 4 contains the detail component level design of the integrated drive. This will include component selection and de-rating, PCB layout and thermal design based on information from Chapter 2 and Chapter 3. The outcome of Chapter 4 is a set of manufacturing data, including detail circuit schematics.

Chapter 5 contains the measured test results and a discussion of the results whereas Chapter 6 states the conclusion of the research and makes recommendations for future work.

Chapter 2

Literature study

Chapter 2 consists of a detail literature study that covers the topics most relevant to this research. The operating principle and advantages of AMBs are discussed. Various categories of self-sensing are discussed with specific reference to the amplitude modulation approach of self-sensing AMBs. Aspects of digital signal processing including processor types and co-processor architectures are discussed. Power amplifiers used in AMB systems are also discussed. Finally various aspects of PCB design, including signal integrity and EMI are discussed.

2.1 Active magnetic bearings

2.1.1 Operating principle

A magnetic circuit model will be used to demonstrate the principle of electromagnetic force generation in an AMB. This simplified model consists of a U-I core with an air gap between the U and I sections of the core as shown in Figure 2-1. The subsequent analysis is based on the following assumptions:

- No flux leakage in the winding or flux fringing in the air gap
- The flux density remains linear and never saturates
- Eddy current effects are negligible
- Changes in the air gap are small compared to the steady state air gap dimension

It is acceptable to develop a simplified magnetic circuit for demonstrating the operating principles, however the presence of leakage, fringing, eddy currents and saturation can lead to significant discrepancies between circuit theory and practical performance of an AMB [5]. For this reason more complex techniques such as the finite element method are used in the formal design process.

The U-I shape electromagnet shown in Figure 2-1 has a winding with N turns and current i_m that produces a magneto motive force (MMF)

$$MMF = N \cdot i_m \quad (2-1)$$

Since the relative permeability μ_r of the core material is high, in the order of 1000 to 10000 for iron, the magnetic flux ϕ follows the path shown in Figure 2-1.

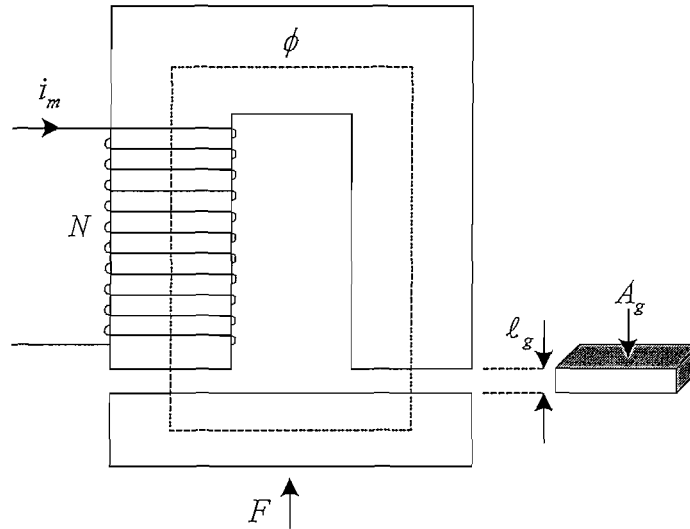


Figure 2-1 Electromagnetic force

The relative permeability of air is 1, so the permeability in the air gap l_g is the permeability of free space

$$\mu_o = 4\pi \times 10^{-7} \text{ [H/m]} \quad (2-2)$$

If the magnetic path length of the core is l_c and the gap length is l_g , the total reluctance of the magnetic circuit is

$$\mathfrak{R}_t = \mathfrak{R}_c + 2 \cdot \mathfrak{R}_g = \frac{l_c}{\mu_o \cdot \mu_r \cdot A_g} + \frac{2 \cdot l_g}{\mu_o \cdot A_g} = \frac{l_c / \mu_r + 2 \cdot l_g}{\mu_o \cdot A_g} \quad (2-3)$$

Since the reluctance of the air gap is significantly larger than the reluctance of the core, the reluctance of the core may be ignored and equation (2-3) can be simplified as follows:

$$\mathfrak{R}_g = \frac{2 \cdot l_g}{\mu_o \cdot A_g} \quad (2-4)$$

The equivalent magnetic circuit for the electromagnet is shown in Figure 2-2.

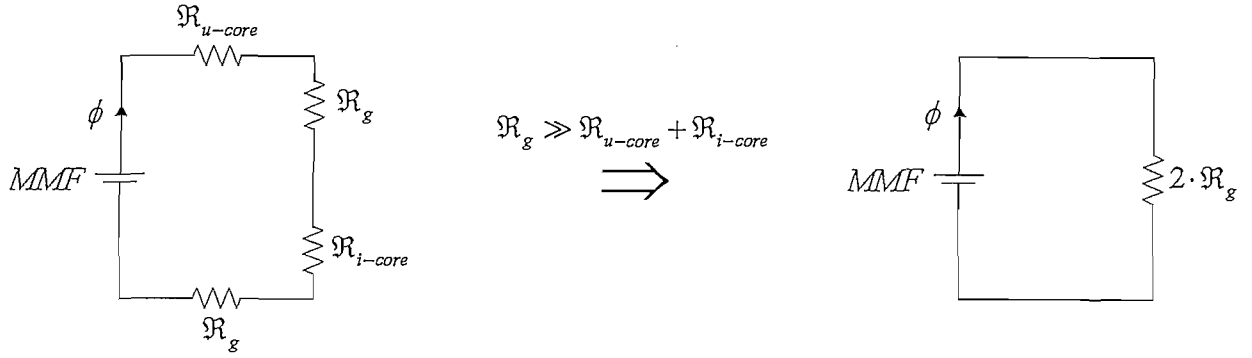


Figure 2-2 Magnetic circuit

Using Rowland's law to calculate the flux in the circuit

$$\phi = \frac{MMF}{\mathcal{R}} = \frac{N \cdot i_m}{\mathcal{R}_g} = \frac{N \cdot i_m \cdot \mu_0 \cdot A_g}{2 \cdot \ell_g} \quad (2-5)$$

The flux linkage in the coil is

$$\lambda = N \cdot \phi = \frac{N^2 \cdot i_m \cdot \mu_0 \cdot A_g}{2 \cdot \ell_g} \quad (2-6)$$

The inductance is the flux linkage divided by the current

$$L = \frac{\lambda}{i_m} = \frac{N^2 \cdot \mu_0 \cdot A_g}{2 \cdot \ell_g} \quad (2-7)$$

The energy stored in the magnetic circuit is

$$E = \frac{1}{2} L \cdot i_m^2 = \frac{N^2 \cdot \mu_0 \cdot A_g \cdot i_m^2}{4 \cdot \ell_g} \quad (2-8)$$

Finally the magnetic force can be expressed as a function of coil current and air gap length

$$F = \frac{E}{\ell_g} = \frac{N^2 \cdot \mu_0 \cdot A_g \cdot i_m^2}{4 \cdot \ell_g^2} \quad (2-9)$$

This result is valid for the U-I shape electromagnet shown in Figure 2-1, however for a heteropolar AMB configuration the poles are radially displaced from one another and this geometric difference needs to be accounted for in (2-9). [1].

The force generated by the electromagnet is directly proportional to the square of the coil current and indirectly proportional to the square of the air gap. From (2-9) it can be seen that as the air gap length decreases, the magnetic force increases, producing negative position stiffness, an open loop unstable mechanism. Thus a feedback stabilization action is required for successful active magnetic suspension [6], [7].

An important observation can be concluded from (2-7), that is the inductance of the electromagnet is inversely proportional to the air gap length. This characteristic is exploited in certain applications of self-sensing AMB technology [8].

2.1.2 Advantages of AMBs

Global warming is becoming an increasingly important issue due to the negative impact that CO₂ emissions have on the earth's atmosphere. Where feasible the energy consuming technologies responsible for CO₂ emission will have to be replaced with alternative energy resources or improvements will have to be made in their efficiency. AMBs are considered one of the key technologies in power mechatronic systems that will help improve system efficiency and thus assist in reducing CO₂ emission [9].

Contact free rotation is the main advantage of AMBs and this allows for high rotation speed without lubrication or mechanical wear and thus higher efficiency than conventional lubricated bearings. Active control of the AMB allows dynamic tuning of rotor characteristics such as damping and stiffness [7]. Another advantage of AMBs is their ability to operate in a vacuum and at extremely high and low temperatures [1]. AMBs provide low loss maintenance free magnetic levitation in a variety of applications.

The magnetically levitated Transrapid Maglev Train developed in Germany has been successfully commissioned in Shanghai, China. The fastest passenger train in the world, the Yamanashi Maglev, makes use of the same technology. The Yamanashi Maglev has a maximum speed of more than 580 Km/h due to magnetic levitation [9].

The application of AMBs in high-speed machine tools has been successfully demonstrated in [7]. In this application a high-speed precision cutting spindle has been developed for a 20 kg rotor that is capable of rotating at 40000 rpm. The maximum speed attainable for a machine using conventional bearings is approximately 15000 rpm. The improved machine performance results in reduced production time and cost, higher metal removal capability and improved surface quality of the end product.

Magnetic suspension is highly desirable in biomedical equipment such as blood pumps [9] and artificial hearts [10]. Conventional blood pumps are susceptible to blood clogging due to blood cells being destroyed in the pump mechanism. The destroyed cells may clog and eventually result in a thrombus. Supporting the blood pump and artificial heart impellers in a magnetic field using AMBs addresses this problem and increases reliability with extended maintenance free operation [9].

In the field of nuclear power generation, AMBs are the preferred means to support the gas turbine shafts in high temperature gas cooled reactors such as the pebble bed modular reactor (PBMR) in South Africa and the HTR-10GT in China. Both systems make use of helium to transfer heat in the closed Bryton cycle where the helium is heated in a reactor, circulated through turbines, compressors and heat exchangers to generate electrical energy. Since helium is chemically and radioactively inert, nuclear contamination is minimised. Conventional lubricated bearings pose a contamination risk since the lubricant may become contaminated. Conventional lubricated bearings require regular maintenance that is hazardous in a nuclear environment. Due to their numerous advantages over conventional bearings, it is predicted that the application of AMBs in the design of high temperature gas cooled reactors will become conventional in the future [11].

In summary, AMBs are a driving technology in the following mechatronic applications [9]:

- High efficiency, compact systems with high rotational shaft speed.
- Equipment operating in harsh temperature, chemical and nuclear environments.
- Ultra high speed rotating equipment with flexible shafts that require vibration control.

2.2 Self sensing AMBs

Magnetic bearings that extract the rotor position information from the signals that drive the electromagnets are referred to as self-sensing [2]. Various methods and associated advantages of self-sensing AMBs have been well documented in literature. Self-sensing methods include linear state-space observer based estimation of the gap displacement [12], estimating the gap displacement by measurement of the inductance of the AMB coil [8], [13], measuring the gap displacement by means of high frequency signal injection [2], [3], [14] and by means of the hysteresis switching amplifier where the switching frequency of the amplifier changes according to gap displacement [15]. The advantages of self-sensing AMBs include:

- Reduced system costs [3], [12].

- Increased reliability and a reduction in size due to the elimination of the sensor component [2], [13], [15].
- Reduced number of connections between the bearing and the controller such as the artificial heart application where the wires have to pass through the chest cavity [10].
- Reduced influence of switching amplifier noise and the elimination of sensor/actuator non co-location issues [2], [13].
- Elimination of the problems associated with implementing position sensors in hostile environmental conditions [13].

The disadvantage of self-sensing AMBs is that self-sensing performance in terms of sensitivity, bandwidth and linearity is inferior to that of a discrete variable reluctance sensor [2].

2.2.1 Categories of self sensing

According to the literature [2], [3], self-sensing can be divided into two main categories namely parameter estimation, also known as the modulation approach and state estimation; also referred to as observer based calculation. A schematic representation of the types of self-sensing is given in Figure 2-3. Combinations of these self-sensing techniques are also possible [9].

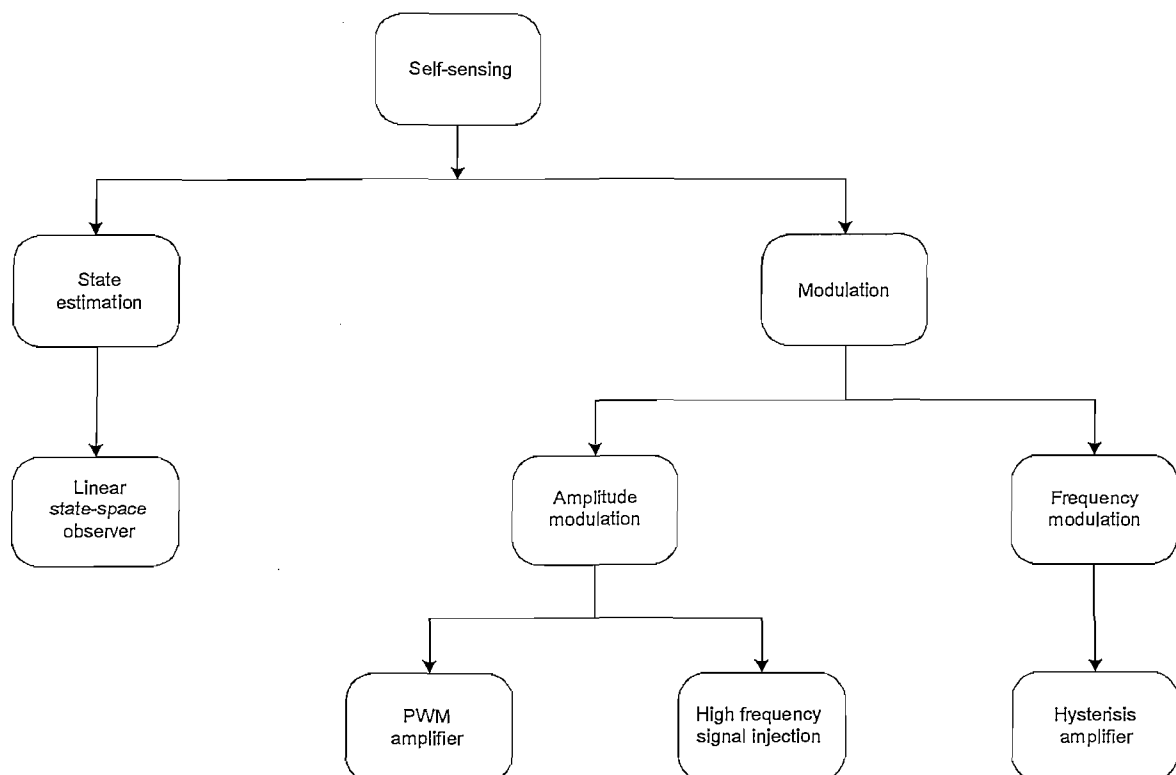


Figure 2-3 Self-sensing categories [3]

The principle of self-sensing AMBs based on the state estimation approach has been successfully demonstrated in [12]. Here a linear state-space observer was implemented to estimate the gap displacement. The state-space model that was used to describe the system was found to be observable and controllable and thus it was possible to design a suitable controller for the system. However the resulting closed loop system performance exhibits poor robustness and small parameter changes cause system instability [2].

The underlying principle applicable to the parameter estimation based self-sensing techniques is that the inductance of an AMB electromagnet is inversely proportional to the air gap [8].

Self-sensing based on the hysteresis amplifier is an example of the frequency modulation approach to self-sensing AMBs. The switching frequency of the hysteresis amplifier varies in sympathy with the gap displacement between the electromagnet and the rotor. Thus the rotor position can be estimated by measuring the frequency or the period of the switching amplifier signal [15].

The high frequency signal injection method of self-sensing involves intentionally injecting a signal into the system instead of relying on the current ripple as a function of PWM operation, to estimate the rotor position. This method of self-sensing, although not limited to, is well suited to AMBs driven by linear amplifiers [8]. The amplitude of the signals used to estimate the position can be controlled and thus improve the signal to noise ratio of this method. When high frequency signal injection is realised using switching amplifiers, no additional hardware is required to implement this method of self-sensing since the PWM amplifier used to control the bearing current, can generate the injection signal [14].

A self-sensing technique that uses the PWM current ripple to estimate the rotor position was proposed in [2]. This method makes use of a real-time simulated bearing model to eliminate the influence of the switching amplifier voltage and duty cycle variation on the estimated rotor position. The input to the bearing simulation is the estimated gap and the switching amplifier output voltage, the same voltage used to supply the actual bearing. Two identical filters are used to demodulate the PWM current ripple and the output of the bearing simulation. The discrepancy between the two filter outputs is used to correct the gap displacement. This self-sensing method has been successfully implemented in a centrifugal AMB heart pump [10]. A block diagram illustrating this self-sensing technique is shown in Figure 2-4.

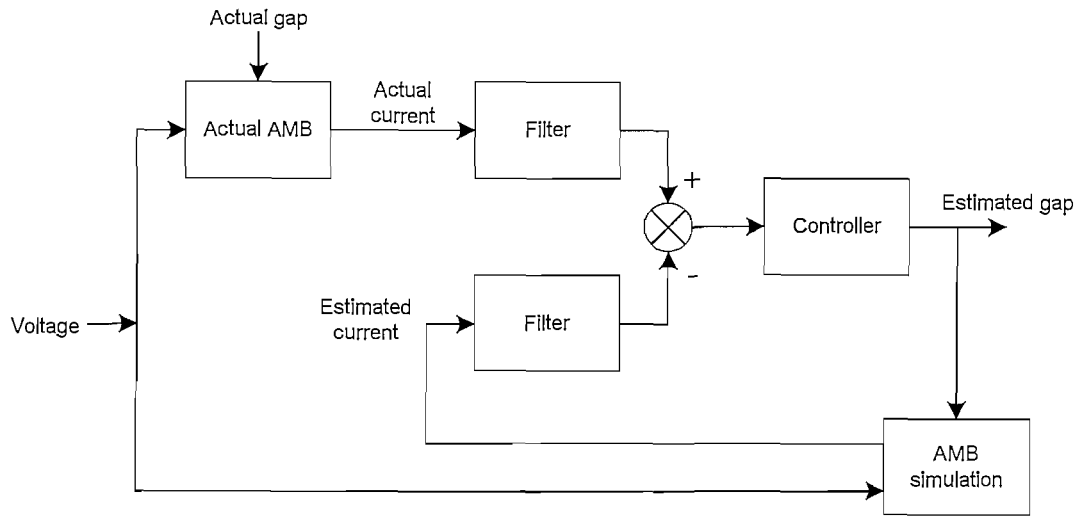


Figure 2-4 Parameter estimation self-sensing scheme [10]

Since this research will focus on hardware development of an integrated co-processor based power electronic drive to facilitate the implementation of the current amplitude modulation approach to self-sensing, adapted from the work done by Schammas et al [3], this method is discussed in more detail in the next section.

2.2.2 Self-sensing based on the current amplitude modulation approach

Referring to Figure 2-3, the current amplitude modulation method of self-sensing is categorized as parameter estimation. The high frequency coil current is directly proportional to the inductance of the coil and inversely proportional to the gap length. The AMB model in Figure 2-5 will be used to illustrate the relationship between the electromagnet coil current and the rotor position.

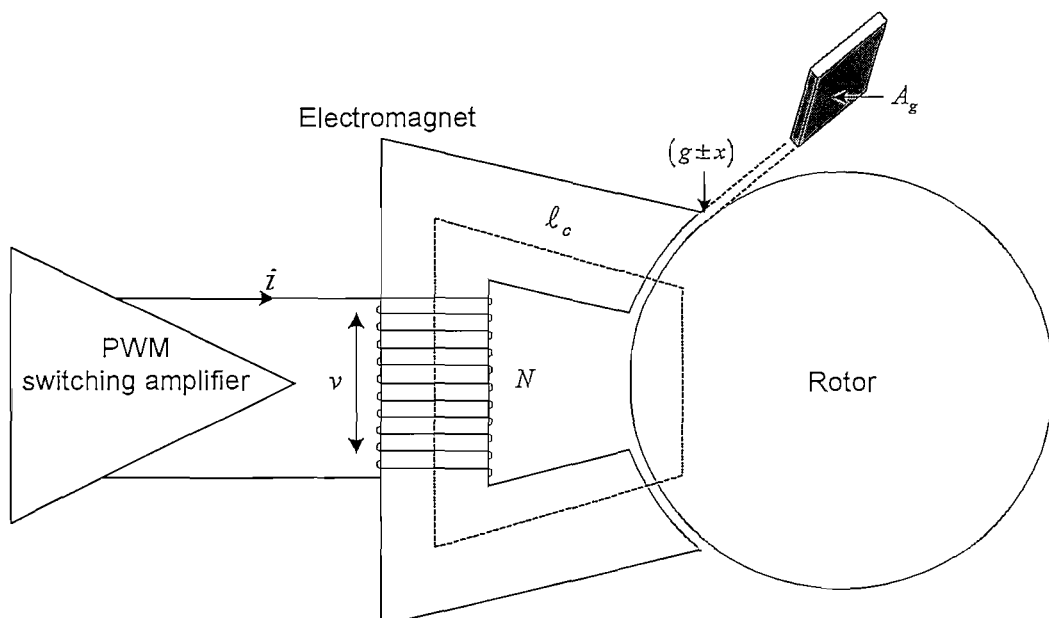


Figure 2-5 AMB model

Referring to Figure 2-5, the voltage v across the electromagnet coil is

$$v = N \frac{d\phi}{dt} + i \cdot R \quad (2-10)$$

where N is the number of coil turns, i is the current through the coil, R is the resistance of the coil and ϕ is the coil flux. Using (2-5) and including the effect of the core reluctance, the flux in the coil is

$$\phi = \frac{N \cdot i \cdot \mu_0 \cdot A_g}{2(g \pm x) + (\ell_c / \mu_r)} \quad (2-11)$$

where μ_0 is the permeability of free space, μ_r is the relative permeability of the core material, A_g is the cross sectional area of the air gap, ℓ_c is the magnetic path length of the core, g is the nominal air gap and x is the change in air gap. The inductance of the coil is

$$L = \frac{N \cdot \phi}{i} = \frac{N^2 \cdot \mu_0 \cdot A_g}{2(g \pm x) + (\ell_c / \mu_r)} \quad (2-12)$$

From (2-12) it is clear that the inductance of the electromagnet coil is inversely proportional to the rotor gap. Since Lenz's law and Faraday's law both describe the voltage across the electromagnet coil, (2-10) may be rewritten as

$$v = L \frac{di}{dt} + i \cdot R \quad (2-13)$$

The change in coil current is determined by substituting (2-12) into (2-13)

$$\frac{di}{dt} = \frac{2(g \pm x) + (\ell_c / \mu_r)}{N^2 \cdot \mu_0 \cdot A_g} \cdot (v - i \cdot R) \quad (2-14)$$

Equation (2-14) establishes the relationship between the electromagnet coil current and the position of the rotor. The PWM current signal contains the position information and the PWM voltage signal contains the duty cycle variation of the power amplifier. The switching frequency of the power amplifier is the carrier for the amplitude modulated current signal. The rotor position information can be determined by demodulating the high frequency component of the current and voltage signals. The demodulated current and voltage signals are the inputs to the self-sensing algorithm. A block diagram depicting the amplitude modulation self-sensing approach, as implemented by Schammas et al [3], is shown in Figure 2-6.

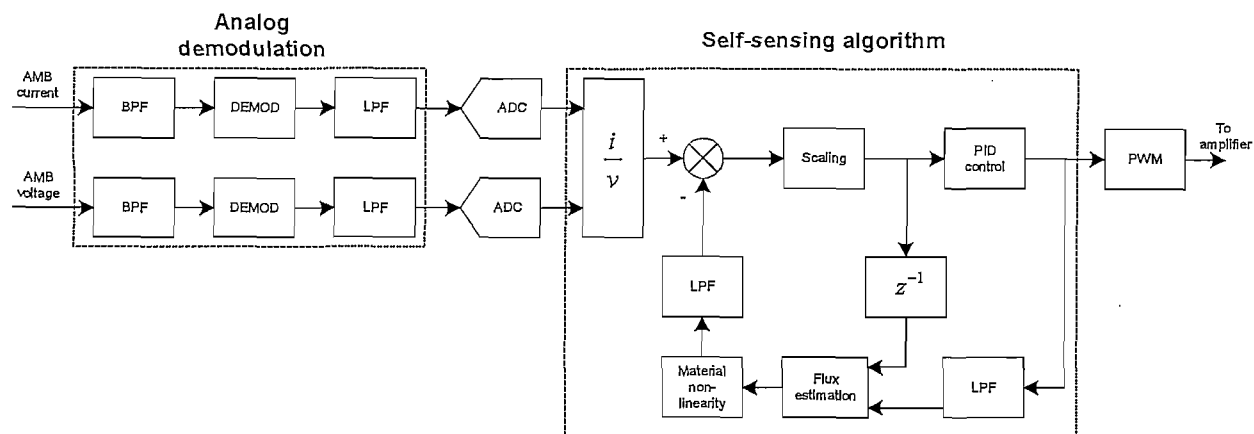


Figure 2-6 Amplitude modulation self-sensing [3]

The analog demodulation block in Figure 2-6 is an amplitude modulation (AM) demodulator that outputs the envelope components of the voltage and current signals. The fundamental component of the high frequency current and voltage is obtained by means of band-pass filtering (BPF). The filtered voltage and current signals are then full-wave rectified by a high speed, synchronous demodulator. The rectified output is then low-pass filtered (LPF) before being sampled by an ADC.

The analog demodulator in Figure 2-6 can be realized in various ways. The first case is where the analog components of the demodulator are replaced by an equivalent digital implementation as shown in Figure 2-7. The benefit of digital demodulation is the flexibility it offers in terms of scaling and demodulation options.

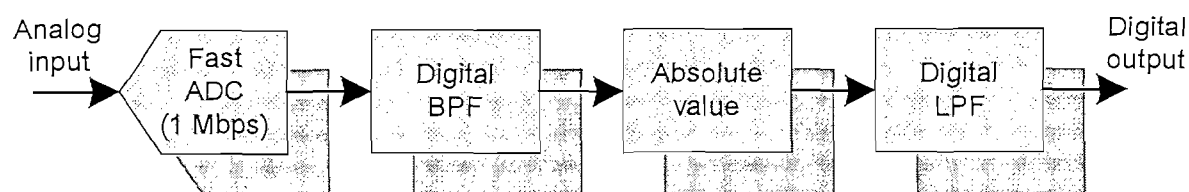


Figure 2-7 Digital demodulator

Figure 2-8 shows a variation where a FFT of the fundamental component of the current or voltage is calculated. The fundamental component is obtained by an analogue BPF filter. The demodulation is completed by determining the peak value of the FFT output.

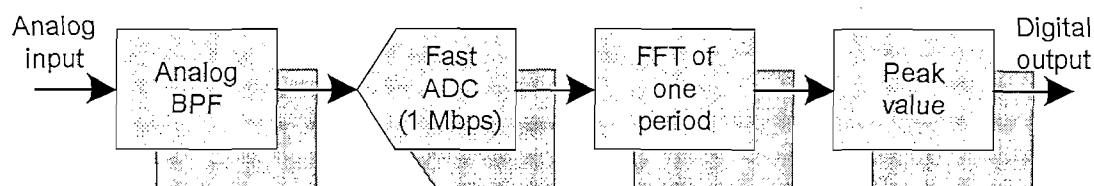


Figure 2-8 FFT demodulator

Figure 2-9 shows another demodulation variation that is based on the synchronous sampling method. Once again the fundamental component is obtained by an analogue BPF and sampled at the peak values. The fundamental is sampled at double the switching frequency of the power amplifier to obtain both the negative and positive peaks. Finally the absolute value is calculated.

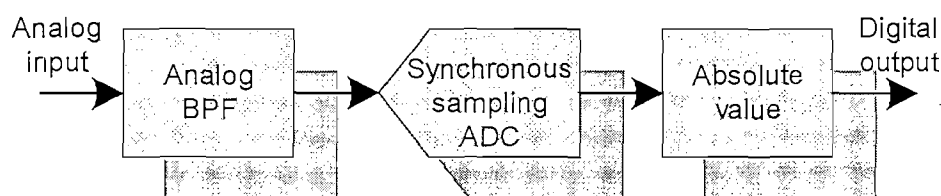


Figure 2-9 Synchronous sampling demodulator

The advantage of the current amplitude modulation algorithm is that the demodulated current and voltage signals are shifted in frequency and thus require low bandwidth for further processing [3]. Thus the self-sensing algorithm may be implemented in the digital domain. The demodulated current signal is divided by the demodulated voltage signal as shown in Figure 2-6. The result of the division already represents an estimated position, however this position is not scaled, nor does it include any compensation for nonlinear effects such as the relative permeability of the material. The algorithm compensates for the nonlinear material effects by using one delayed sample of the estimated position and the reference current. The reference current is passed through a digital LPF with the same transfer function as the power amplifier. The output of the LPF represents the simulated current output of the power amplifier. The simulated current and one delayed sample of the estimated position are used to estimate the flux in the magnetic material. The estimated flux is used in a quadratic equation that represents the material non-linearity. The coefficients of the quadratic equation are determined experimentally. The result of the quadratic equation is passed through a LPF and subtracted from the result of the demodulated current and voltage division. This signal, once scaled, represents the estimated position.

In order to realize the current amplitude modulation self-sensing scheme, a suitable digital signal processing architecture will have to be identified. The proposed architecture will need

sufficient bandwidth and processing speed to implement the self-sensing algorithm requirements including additional functionality such as system communications.

2.3 Signal processors

The argument in favor of digital control in AMB systems has been well documented in the literature [1], [6], [7], [16]. Digital control of AMBs offers the following advantages:

- Flexibility during the development stage to easily implement and compare various control strategies
- Implementation of complex control functions, especially in the case of self-sensing algorithms
- The ability to perform additional tasks such as system communication, start-up and shut-down procedures, system calibration, monitoring and diagnostics
- Respond in a safe and controlled manner in the case of an emergency.
- Easily implement subsequent changes or upgrades to the system

The challenge facing the designer of an AMB system is to identify the appropriate digital controller architecture to match the computational complexity of the intended control algorithm [6]. The decision will depend on various factors such as cost, development tools, speed, number format, environment and the type of processor [1].

2.3.1 DSP

The DSP is a specific type of digital processor with optimized hardware architecture for the efficient execution of signal processing algorithms such as FIR, IIR and FFT. The hardware features that allow DSPs to efficiently process these algorithms are [4]:

- Multiple, separate program and data busses: Multiple busses allow the DSP to simultaneously fetch and execute code.
- Fast on-chip memory: Access to on-chip memory requires less overhead than access to external memory and is thus faster and more efficient for storing coefficients and intermediate results.
- Multiply and accumulate (MAC) unit: The MAC unit consists of a hardware multiplier and accumulator capable of performing a MAC operation in a single central processing unit (CPU) cycle.
- Pipelined architecture: Pipelining involves dividing the instruction into sub-actions in order to minimize latency between the faster CPU and the slower memory. Figure 2-10

demonstrates how the pipelining process saves CPU cycles. The sub-actions required for pipelining are:

- Pre-fetch: Calculate the address of the next instruction via the program counter register.
 - Fetch: Retrieve the instruction from the memory at the calculated address.
 - Decode: Interpret the instruction.
 - Access: If an operand is required, determine the address of the operand.
 - Read: Retrieve the operand from the memory.
 - Execute: Perform the operation.
- Circular buffer addressing: Circular buffer addressing simplifies data access by moving a pointer through the data instead of moving the actual data.
 - Bit reversed addressing: Bit reversed addressing is used in FFT computation to reverse the order of the input and output bits efficiently.
 - Zero overhead looping: The overhead associated with looping through a process several times, is optimized by using zero overhead looping.
 - Overflow and saturation: In fixed-point systems overflow and saturation are automatically taken care of by the DSP.

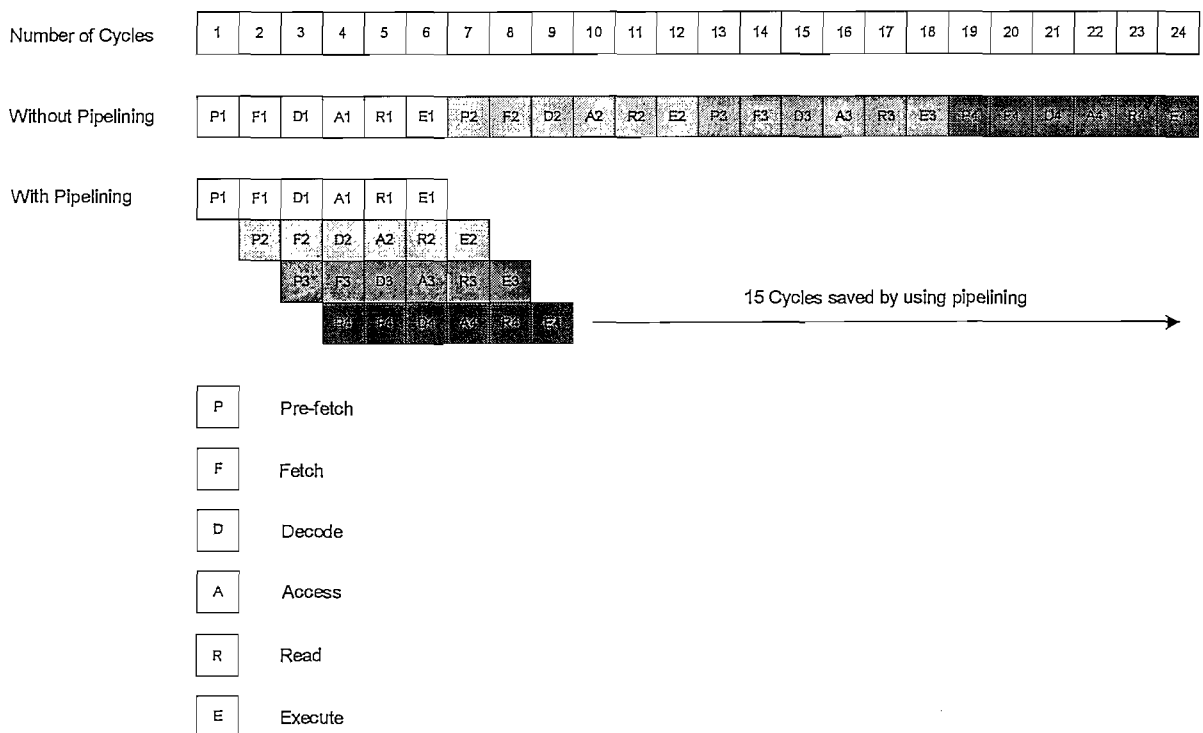


Figure 2-10 DSP Pipelining

DSP signal processing can be divided into two models, the single sample model or the block processing model. The goal for single sample processing is minimum latency. Single sample processing is interrupt driven with the current output data made available before the next input data is sampled. A digital control system is a good example of single sample processing.

Block processing accumulates a large number of samples via a direct memory access controller, buffers the data in a receive buffer and then processes the data. The processed data is output via a transmit buffer and the direct memory access controller. Block processing systems are computationally efficient for calculating algorithms such as FFT, however they increase the input-to-output latency. Block processing is used in video and telecommunications signal processing applications.

By exploiting the full advantage of DSP architectural features such as MAC and pipelining, a single DSP is capable of controlling a 5 DOF AMB as well as implementing additional filtering functions without adding unacceptable latency to the control system [7].

The DSP allows functional enhancement of an AMB system by facilitating remote access to the system via modem that enables remote monitoring of the operational status, fault history and diagnostics [16].

All controllers, notch filters and a position estimator have been implemented on a single DSP in a 4 DOF self-sensing application, based on the high frequency signal injection method, with rotor speeds up to 30000 rpm. No additional circuitry was required for the signal injection since this was done by the DSP [14].

The wide choice of hardware platforms and development software for DSP is also highlighted as a crucial advantage in favor of DSP for digital AMB control [7].

2.3.2 *FPGA*

A FPGA is an integrated circuit that contains arrays of configurable logic blocks (CLBs) and configurable interconnects between these blocks. The basic CLB consists of a multiple input lookup table, a D-type flip-flop and a multiplexer. The CLB is the primary logic resource for implementing combinational and synchronous logic functions as well as small amounts of distributed memory [17].

FPGAs contain large blocks of memory that can be configured as synchronous dual port RAM. Digital clock managers that provide frequency synthesis, multiplication, division and phase shifting of clock signals are included in modern FPGAs. Additional flexible logic resources include dedicated hardware multipliers, carry logic and support for a wide variety of input/output standards.

FPGAs are available as one-time-programmable devices, flash memory re-programmable devices and SRAM re-programmable devices. The SRAM FPGAs require a configuration memory device to program them at power-up. The flash memory re-programmable devices and SRAM re-programmable FPGAs can be programmed and debugged via a Joint Test Action Group (JTAG) port.

A direct comparison of a DSP and a FPGA based controller in an AMB system demonstrates that the FPGA controller out performs the DSP controller in several areas. The FPGA controller is two orders of magnitude faster than the DSP. The sample time of the FPGA controller is 100 ns versus 11 μ s for the DSP controller. The DSP controller is an interrupt driven sequential processor that doesn't allow any concurrent processing. The FPGA controller allows extreme parallelism since it can simultaneously multiply each term in a difference equation using its own hardware multiplier while initiating a new ADC sample [18].

The FPGA controller is more accurate and has less noise than the DSP controller. The DSP uses a fixed 16-bit representation for the coefficients and recursive terms throughout the calculations whereas the FPGA allows custom bit width of the data at any point in the computation, thus avoiding the negative effects of finite word length. This is especially important as the sample frequency increases since higher resolution coefficients are required as the sampling frequency increases [18].

The benefit of FPGA features such as dual port block RAM, customized number format and high level of parallelism is demonstrated in the application of a AMB with a flexible rotor. In this application the number of flexible modes in the plant model could be increased due to the capability of the FPGA [19].

2.3.3 Co-processing

In this context a co-processor may refer to an architecture that combines a DSP and a FPGA, two DSPs or two FPGAs, however combining the capabilities of FPGAs and DSPs increases the scope of a design solution and is a good model for enabling flexibility, programmability and computational acceleration of the system [4], [20], [21].

A FPGA may be used in a DSP system as a co-processor for the following reasons [4]:

- To extend the capability of a generic low cost DSP by off loading computationally intensive algorithms to the FPGA
- To eliminate the requirement for a high performance, high cost DSP

- To increase the computational throughput due to higher resolution or increased bandwidth
- For prototyping new signal processing algorithms
- To reduce system size, complexity and cost by consolidating glue logic and processor peripherals in a single FPGA

The FPGA and DSP co-processor architecture is used in various demanding power electronic applications such as high performance electric drives [22] to solve computationally intensive algorithms such as predictive uni-polar current control [23] and three level space vector PWM [24], to name a few.

A FPGA based floating point co-processor has been developed to improve the computational performance of a fixed point DSP [25]. For evaluation purposes a FFT algorithm was implemented on the DSP and the co-processor. The results show that the co-processor architecture is five times faster than the DSP, in spite of the fact that two thirds of the performance improvement is consumed by the time it takes to transfer data between the FPGA and the DSP.

The time taken to transfer data between processors is an important consideration in a co-processor environment. For this reason it is critical to partition the design so that the interaction required between the processors is minimized. Certain FPGA manufacturers make provision for embedding a soft processor core in the FPGA device, e.g. a Xilinx FPGA and an embedded Power PC processor, which optimizes data transfer between the processors and allows flexible partitioning of the design into programmable software and hardware [26].

The high density of modern FPGAs allows additional hardware such as encoder counters and PWM generators to be implemented on a co-processor FPGA resulting in fewer hardware parts which improves cost effectiveness, reduces power consumption, reduces system noise and PCB space utilization [20], [27]. The high density of FPGAs can be further exploited since they allow multiple instantiations of complex functions such as FFT to be implemented in a single FPGA. A price versus performance comparison shows that FPGA co-processors offer better performance for lower cost when compared to a single DSP approach [28].

Significant improvements can be made in the performance of a DSP system by taking advantage of the flexibility that a FPGA co-processor offers for implementing functions that require a high level of parallelism. By offloading operations that require high speed parallel processing onto a FPGA while handling operations that require high speed sequential

processing on a DSP, the performance and cost of a signal processing system are optimized while lowering system power requirements [29].

2.4 Power amplifiers

The purpose of the power amplifier in an AMB system is to regulate the amount of energy in the electromagnet by either adding energy, removing energy or maintaining energy in the electromagnet. Power amplifier characteristics such as current slew rate, bandwidth, harmonic distortion and efficiency play an important role in the performance of the AMB system. The power amplifier has a major influence on the reliability and dynamic characteristics of an AMB system and therefore requires careful consideration [37], [38]. There are a number of different amplifier topologies that are used to drive AMBs, however they can be classified as either linear, switching or hybrid [30].

Due to their poor efficiency, linear amplifiers are only used in low power AMB applications, thus switching amplifiers are used in the majority of AMB applications [1], [9], [31]. The switching amplifiers used in AMB systems make use of various modulation techniques such as current hysteresis, sample and hold, minimum pulse width, and PWM. Each of these methods have their advantages and disadvantages, however the PWM modulation techniques remain the most widely used for AMBs [32]. Although the space vector PWM technique is more common in AC motor drive applications, it has also been proposed for use in AMBs [33].

Hybrid amplifiers, as the name implies, share characteristics of both linear and switching amplifiers. The disadvantage of hybrid amplifiers is the complexity of the circuit and the control strategy required [9], [30], [31].

2.4.1 Linear power amplifiers

Linear power amplifiers are rarely used in high power AMB applications due to their poor efficiency that results in large heat sinks and thus increased cost [9]. However linear amplifiers do have certain advantages when compared to switching power amplifiers in low power AMB applications. For example the superior bandwidth and low noise performance of linear amplifiers makes them the preferred topology in low power space applications [8], [32]. An improved efficiency linear amplifier, the modified class-G linear power amplifier has been proposed for use in AMB systems [34]. Although improvements in efficiency over conventional linear amplifiers are reported in [34], this topology remains applicable to low power AMB applications.

Figure 2-11 shows the basic configuration of a push-pull linear amplifier output stage with an example operating point for transistor *TR1*. When *TR1* conducts, it adds energy to the load and

$TR2$ is off. When $TR2$ conducts, it removes energy from the load and $TR1$ is off. At the operating point for $TR1$ in Figure 2-11 the power dissipation in $TR1$ is 900 watts and the power dissipation in R_{load} is 100 watts.

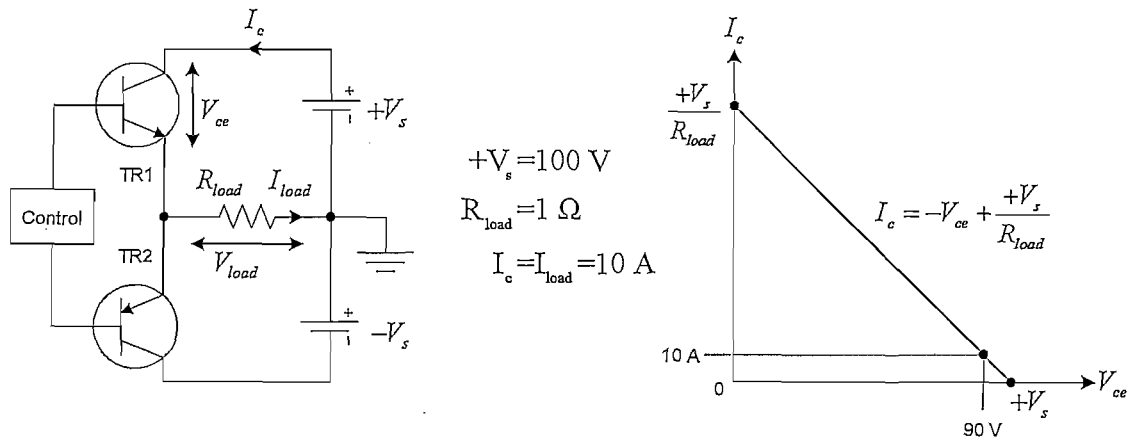


Figure 2-11 Linear amplifier

In this example the amplifier efficiency is only 10% which is typical in AMB applications where, in order to meet the dynamic performance requirements, $+V_s$ has to be a higher voltage than necessary for steady state operation. This voltage reserve is required to ensure a high force slew rate that is dependant on the maximum output voltage of the amplifier and the inductance of the electromagnet. However during steady state operation the output voltage of the amplifier only has to supply the voltage drop across the copper resistance of the electromagnet, resulting in extremely poor efficiency [30], [32]. A switching power amplifier may be used to improve the amplifier efficiency.

2.4.2 Switching power amplifiers

The single phase H-bridge converter and the modified H-bridge converter for unidirectional current flow are the two preferred switching amplifier topologies in AMB applications [9], [30], [32]. These two switching amplifier topologies are shown in Figure 2-12.

The single phase H-bridge converter can generate positive and negative output voltage as well as positive and negative output current, providing four quadrant operation. The switching power amplifier transistors are usually metal oxide semiconductor field effect transistors (MOSFET) or insulated gate bipolar transistors (IGBT). IGBTs are preferred in applications over 100 V and MOSFETs are preferred in applications under 100 V [9], [30]. Furthermore, as the voltage rating of the MOSFET increases so too does the reverse recovery charge and reverse recovery time of the integral reverse diode that causes an increase in switching loss.

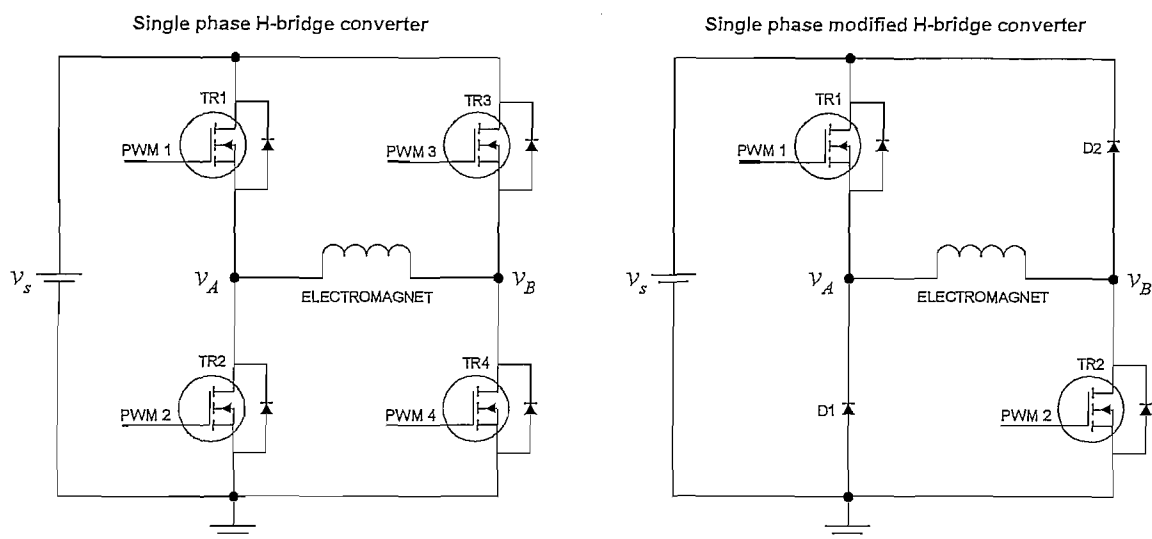


Figure 2-12 Single phase H-bridge converters

The modified H-bridge converter is used extensively in current controlled AMBs with differential mode drive [31]. In this configuration the amplifier output voltage is required to be positive or negative however the electromagnet current does not change direction, thus requiring only two quadrant operation. The advantage of the modified H-bridge converter is a simplified drive circuit since only two switching devices are actively controlled thus reducing the cost of this converter [32]. The modified H-bridge converter does not require any dead-band between switching transitions since no switching time overlap is possible due to the circuit configuration. The absence of dead-band improves the output linearity of the modified H-bridge converter [9]. The AMB high frequency dynamic performance must be thoroughly evaluated when using the modified H-bridge topology since this topology doesn't allow the load current to reverse [35].

A PWM modulation scheme regulates the amount of energy the switching amplifier adds, removes or maintains in the electromagnet. Bipolar PWM and uni-polar PWM are the most widely implemented PWM technique in AMB systems [32]. Both PWM techniques are shown in Figure 2-13.

Referring to the single phase H-bridge converter in Figure 2-12, for bipolar PWM the switches $TR1$ and $TR4$ are treated as a pair and are switched on and off simultaneously, as are switches $TR2$ and $TR3$. Uni-polar PWM controls the switches in each leg of the H-bridge independently of the other leg i.e. $TR1$ and $TR2$ are controlled independently of $TR3$ and $TR4$. With reference to Figure 2-13, in the case of bipolar PWM $+V_{control}$ controls both pairs of switches and in the case of uni-polar PWM, $+V_{control}$ controls switches $TR1$ and $TR2$, while $-V_{control}$ controls switches $TR3$ and $TR4$.

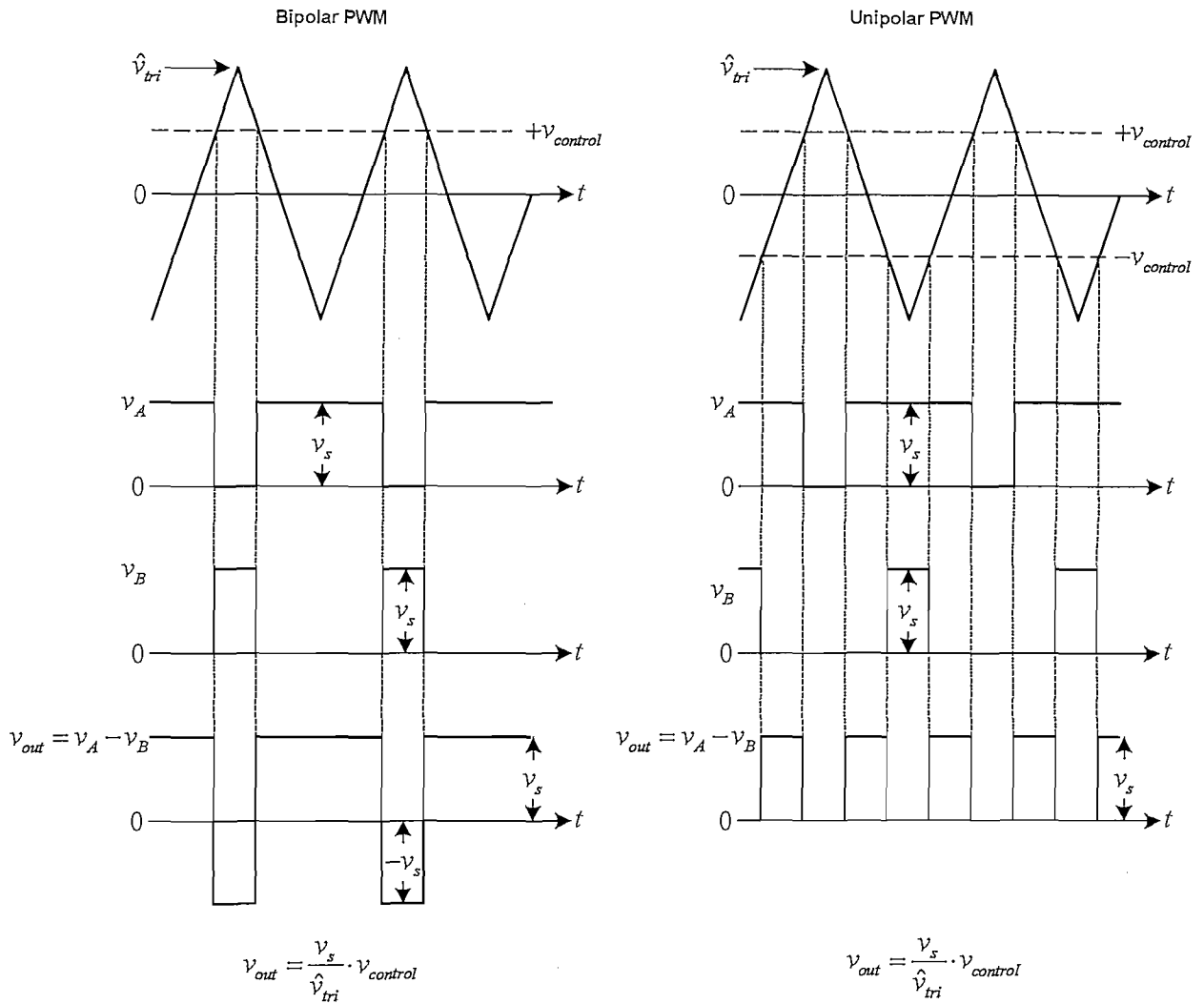


Figure 2-13 Bipolar and uni-polar PWM

It is interesting to note that the average output voltage V_{out} is identical for both of these PWM strategies. When operated at the same switching frequency the uni-polar PWM output is double the switching frequency compared to the bipolar PWM method [36]. The result is reduced output ripple, reduced current harmonics and increased bandwidth [30], [32]. When operated at the same output frequency, the uni-polar PWM method has half the switching loss compared to the bipolar PWM method.

Although it only has two switches, the modified H-bridge converter may also be operated with bipolar PWM or uni-polar PWM, the modes of operation are similar to those described for the conventional H-bridge converter. Referring to the modified H-bridge converter in Figure 2-11, for bipolar PWM the switches $TR1$ and $TR4$ are treated as a pair and are switched on and off simultaneously, $+V_{control}$ controls both pairs of switches. When the switches are on the current and voltage are both positive. When the switches are off the current decays through $D1$ and $D2$ and the voltage becomes negative. For the modified H-bridge converter operating with uni-polar

PWM, $+V_{control}$ controls switch $TR1$ while $-V_{control}$ controls switch $TR2$. When operated with unipolar PWM switching the modified H-bridge converter has an additional operating mode where one switch, either $TR1$ or $TR2$, is switched on while the other switch is off. During this mode the output voltage is clamped at zero and the current is maintained at a constant level.

2.4.3 Space vector PWM

The voltage and current in the two electromagnets of a 1 DOF AMB can be controlled independently using the space vector pulse width modulation (SVPWM) technique and a three-phase bridge [33]. Figure 2-14 shows the circuit configuration where $V1$ and $V2$ represent the AMB coil voltages and V_a , V_b and V_c represent the output voltages of the three-phase bridge.

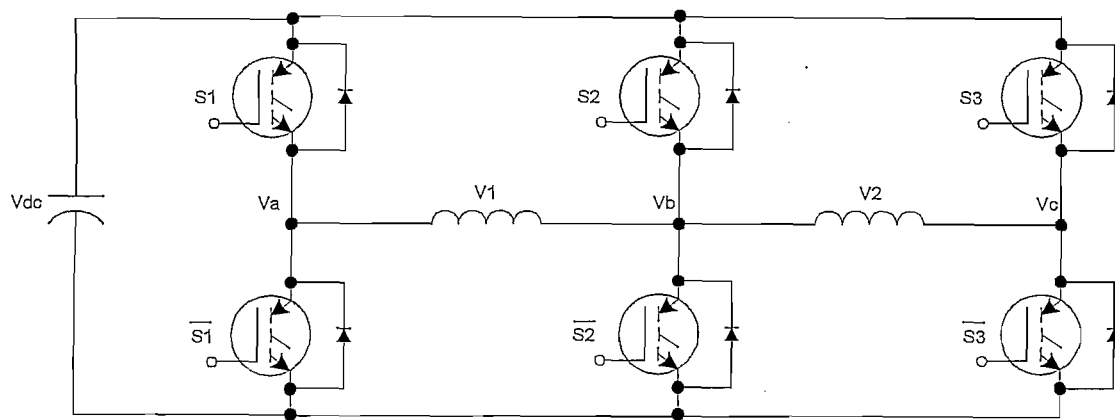


Figure 2-14 Three-phase bridge for a 1 DOF AMB

The upper switch in each leg of the three-phase bridge shown in Figure 2-14 can either be on or off. The corresponding lower switch in each leg is always the complement of its upper counterpart. This switching strategy gives eight possible switching states for the three switches $S1$, $S2$ and $S3$. Depending on the eight possible switching states, the coil voltages $V1$ and $V2$ are switched to $+V_{dc}$, $-V_{dc}$ or 0 V. Each of the eight switching states represents a basic voltage vector. Six of the basic voltage vectors are referred to as active voltage vectors while the remaining two are referred to as zero vectors. The relationship between the basic vectors, the switching states and the coil voltages is shown in Table 2-1.

Table 2-1 Basic voltage vectors and switching states

Basic vectors	Switching states			Coil voltages		Normalized coil voltages	
	S1	S2	S3	V1	V2	X	Y
$\vec{V}_0$	0	0	0	0 V	0 V	0	0
$\vec{V}_5$	0	0	1	0 V	$-V_{dc}$	0	-1

$\vec{V}_3$	0	1	0	-Vdc	+Vdc	-1	+1
$\vec{V}_4$	0	1	1	-Vdc	0 V	-1	0
$\vec{V}_1$	1	0	0	+Vdc	0 V	+1	0
$\vec{V}_6$	1	0	1	+Vdc	-Vdc	+1	-1
$\vec{V}_2$	1	1	0	0 V	+Vdc	0	+1
$\vec{V}_7$	1	1	1	0 V	0 V	0	0

The six active voltage vectors comprise six sectors in the two dimensional plain that represents the voltage region for the two AMB coils as shown in Figure 2-15.

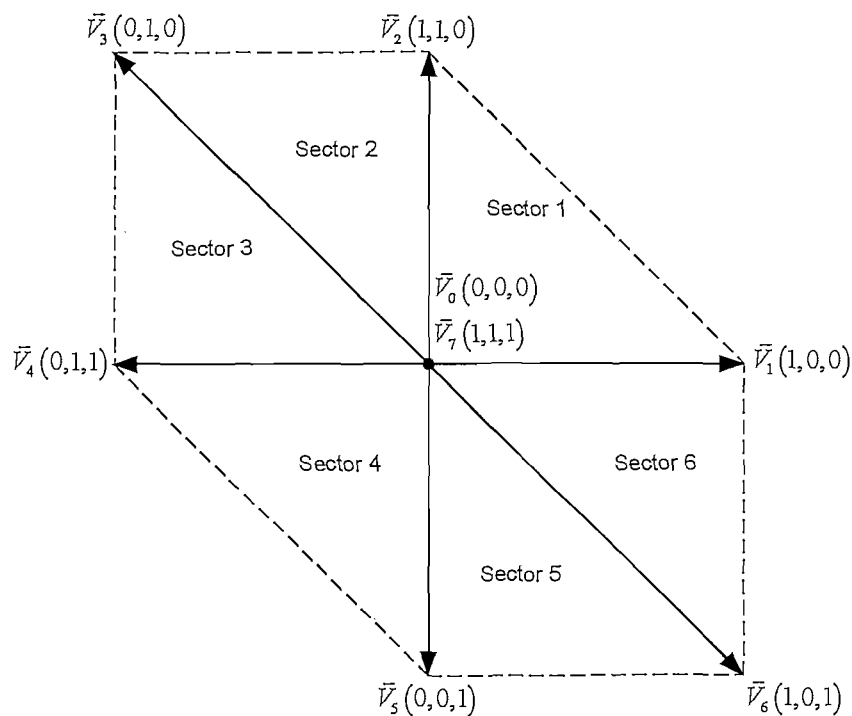


Figure 2-15 Voltage region for the two AMB coils

The zero vectors represent the condition where all three switches, S_1 , S_2 and S_3 are all on or all off. During these switching states the coil voltages V_1 and V_2 have zero voltage across them. The zero vectors are situated at the origin of the two dimensional plain as shown in Figure 2-15.

A reference voltage vector, that represents the two coil voltages V_1 and V_2 , is generated in a particular sector as the resultant of the time weighted average of the two adjacent basic vectors that form the sector. The zero vectors are applied for the time required to complete the remainder of the switching period.

The first half of a symmetric SVPWM switching period always starts with a zero vector and ends with a zero vector for the period T_0 . The first active voltage vector is applied for the period T_1 and the second active voltage vector is applied for the period T_2 . During the second half of the symmetric SVPWM switching period the sequence is repeated in reverse order. The PWM switching period T_s can be represented by (2-15)

$$T_s = T_1 + T_2 + T_0 \quad (2-15)$$

Consider sector 2 in Figure 2-15, bounded by vector $\vec{V}_2$ and vector $\vec{V}_3$. The resultant reference vector $\vec{V}_{ref}$ is represented in this sector as

$$\vec{V}_{ref} = \frac{T_1}{T_s} \cdot \vec{V}_3 + \frac{T_2}{T_s} \cdot \vec{V}_2 + \frac{T_0}{T_s} \cdot \vec{V}_0 + \frac{T_7}{T_s} \cdot \vec{V}_7 \quad (2-16)$$

Using the normalized coil voltages from table 2-1 where $x = \frac{V_1}{V_{dc}}$ and $y = \frac{V_2}{V_{dc}}$ equation (2-16)

can be represented as follows

$$T_s(x, y) = T_1(x, y) + T_2(x, y) + T_0(x, y) \quad (2-17)$$

Using (2-17) the resultant vector for each sector can be represented in terms of the normalized coil voltages and switching times for each leg of the three-phase bridge.

Sector 1

Sector 1 is bounded by vector $\vec{V}_1$ and vector $\vec{V}_2$. In this sector the voltage state in terms of the normalized coil voltages is (1,0) during T_1 , (0,1) during T_2 and (0,0) during T_0 . Using (2-17) this can be expressed as

$$T_s(x, y) = T_1(1, 0) + T_2(0, 1) + T_0(0, 0) \quad (2-18)$$

Using (2-15) and (2-18) T_1 , T_2 and T_0 are determined as follows

$$T_1 = x \cdot T_s \quad (2-19)$$

$$T_2 = y \cdot T_s \quad (2-20)$$

$$T_0 = T_s - T_1 - T_2 = (1 - x - y) \cdot T_s \quad (2-21)$$

The switching states and symmetric SVPWM waveforms for sector 1 over a full switching period is shown in Figure 2-16.

	$\frac{T_0}{2}$	T_1	T_2	$\frac{T_0}{2}$	$\frac{T_0}{2}$	T_2	T_1	$\frac{T_0}{2}$
S_1	0	1	1	1	1	1	1	0
S_2	0	0	1	1	1	1	0	0
S_3	0	0	0	1	1	0	0	0

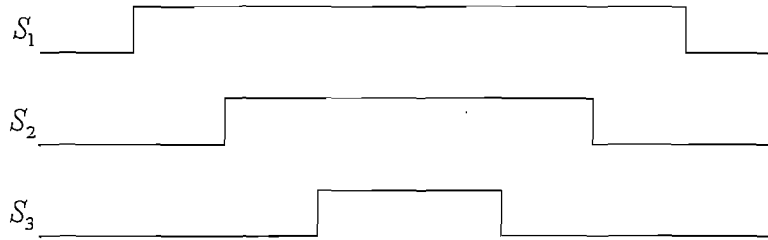


Figure 2-16 Sector 1 SVPWM

The switching time for each leg of the three-phase bridge is determined as follows

$$S_1 \Rightarrow T_1 + T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1+x+y)}{2} \quad (2-22)$$

$$S_2 \Rightarrow T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1-x+y)}{2} \quad (2-23)$$

$$S_3 \Rightarrow \frac{T_0}{2} = T_s \cdot \frac{(1-x-y)}{2} \quad (2-24)$$

Sector 2

Sector 2 is bounded by vector $\vec{V}_2$ and vector $\vec{V}_3$. In this sector the voltage state in terms of the normalized coil voltages is $(-1,1)$ during T_1 , $(0,1)$ during T_2 and $(0,0)$ during T_0 . Using (2-17) this can be expressed as

$$T_s(x, y) = T_1(-1,1) + T_2(0,1) + T_0(0,0) \quad (2-25)$$

Using (2-15) and (2-18) T_1 , T_2 and T_0 are determined as follows

$$T_1 = -x \cdot T_s \quad (2-26)$$

$$T_2 = x \cdot T_s + y \cdot T_s = (x + y) \cdot T_s \quad (2-27)$$

$$T_0 = T_s - T_1 - T_2 = (1 - y) \cdot T_s \quad (2-28)$$

The switching states and symmetric SVPWM waveforms for sector 2 over a full switching period is shown in Figure 2-17.

	$\frac{T_0}{2}$	T_1	T_2	$\frac{T_0}{2}$	$\frac{T_0}{2}$	T_2	T_1	$\frac{T_0}{2}$
S_1	0	0	1	1	1	1	0	0
S_2	0	1	1	1	1	1	1	0
S_3	0	0	0	1	1	0	0	0

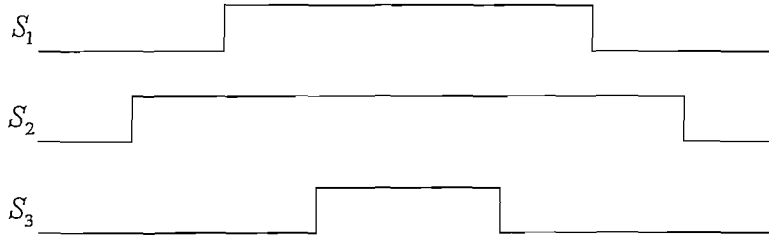


Figure 2-17 Sector 2 SVPWM

The switching time for each leg of the three-phase bridge is determined as follows

$$S_1 \Rightarrow T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1 + 2x + y)}{2} \quad (2-29)$$

$$S_2 \Rightarrow T_1 + T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1 + y)}{2} \quad (2-30)$$

$$S_3 \Rightarrow \frac{T_0}{2} = T_s \cdot \frac{(1 - y)}{2} \quad (2-31)$$

Sector 3

Sector 3 is bounded by vector $\vec{V}_3$ and vector $\vec{V}_4$. In this sector the voltage state in terms of the normalized coil voltages is (-1,1) during T_1 , (-1,0) during T_2 and (0,0) during T_0 . Using (2-17) this can be expressed as

$$T_s(x, y) = T_1(-1, 1) + T_2(-1, 0) + T_0(0, 0) \quad (2-32)$$

Using (2-15) and (2-18) T_1 , T_2 and T_0 are determined as follows

$$T_1 = y \cdot T_s \quad (2-33)$$

$$T_2 = -x \cdot T_s - y \cdot T_s = -(x + y) \cdot T_s \quad (2-34)$$

$$T_0 = T_s - T_1 - T_2 = (1 + x) \cdot T_s \quad (2-35)$$

The switching states and symmetric SVPWM waveforms for sector 3 over a full switching period is shown in Figure 2-18.

	$\frac{T_0}{2}$	T_1	T_2	$\frac{T_0}{2}$	$\frac{T_0}{2}$	T_2	T_1	$\frac{T_0}{2}$
S_1	0	0	0	1	1	0	0	0
S_2	0	1	1	1	1	1	1	0
S_3	0	0	1	1	1	1	0	0

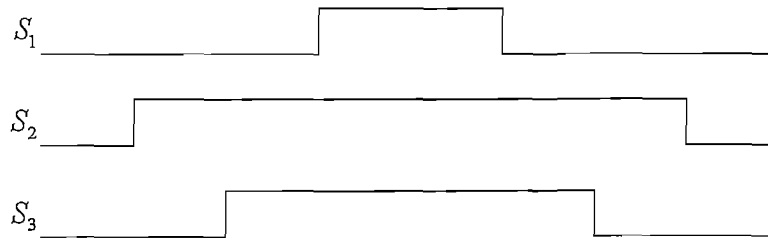


Figure 2-18 Sector 3 SVPWM

The switching time for each leg of the three-phase bridge is determined as follows

$$S_1 \Rightarrow \frac{T_0}{2} = T_s \cdot \frac{(1+x)}{2} \quad (2-36)$$

$$S_2 \Rightarrow T_1 + T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1-x)}{2} \quad (2-37)$$

$$S_3 \Rightarrow T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1-x-2y)}{2} \quad (2-38)$$

Sector 4

Sector 4 is bounded by vector $\vec{V}_4$ and vector $\vec{V}_5$. In this sector the voltage state in terms of the normalized coil voltages is $(0,-1)$ during T_1 , $(-1,0)$ during T_2 and $(0,0)$ during T_0 . Using (2-17) this can be expressed as

$$T_s(x, y) = T_1(0, -1) + T_2(-1, 0) + T_0(0, 0) \quad (2-39)$$

Using (2-15) and (2-18) T_1 , T_2 and T_0 are determined as follows

$$T_1 = -y \cdot T_s \quad (2-40)$$

$$T_2 = -x \cdot T_s \quad (2-41)$$

$$T_0 = T_s - T_1 - T_2 = (1 + x + y) \cdot T_s \quad (2-42)$$

The switching states and symmetric SVPWM waveforms for sector 4 over a full switching period is shown in Figure 2-19.

	$\frac{T_0}{2}$	T_1	T_2	$\frac{T_0}{2}$	$\frac{T_0}{2}$	T_2	T_1	$\frac{T_0}{2}$
S_1	0	0	0	1	1	0	0	0
S_2	0	0	1	1	1	1	0	0
S_3	0	1	1	1	1	1	1	0

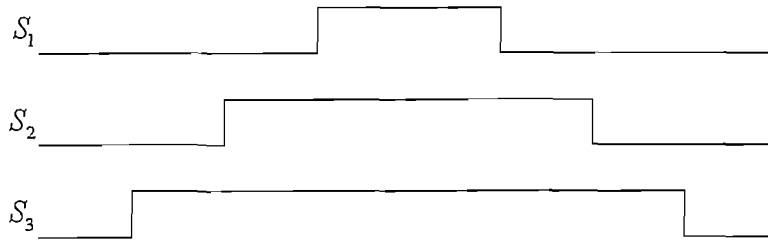


Figure 2-19 Sector 4 SVPWM

The switching time for each leg of the three-phase bridge is determined as follows

$$S_1 \Rightarrow \frac{T_0}{2} = T_s \cdot \frac{(1+x+y)}{2} \quad (2-43)$$

$$S_2 \Rightarrow T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1-x+y)}{2} \quad (2-44)$$

$$S_3 \Rightarrow T_1 + T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1-x-y)}{2} \quad (2-45)$$

Sector 5

Sector 5 is bounded by vector $\vec{V}_5$ and vector $\vec{V}_6$. In this sector the voltage state in terms of the normalized coil voltages is (0,-1) during T_1 , (1,-1) during T_2 and (0,0) during T_0 . Using (2-17) this can be expressed as

$$T_s(x, y) = T_1(0, -1) + T_2(1, -1) + T_0(0, 0) \quad (2-46)$$

Using (2-15) and (2-18) T_1 , T_2 and T_0 are determined as follows

$$T_1 = -(x + y) \cdot T_s \quad (2-47)$$

$$T_2 = x \cdot T_s \quad (2-48)$$

$$T_0 = T_s - T_1 - T_2 = (1 + y) \cdot T_s \quad (2-49)$$

The switching states and symmetric SVPWM waveforms for sector 5 over a full switching period is shown in Figure 2-20.

	$\frac{T_0}{2}$	T_1	T_2	$\frac{T_0}{2}$	$\frac{T_0}{2}$	T_2	T_1	$\frac{T_0}{2}$
S_1	0	0	1	1	1	1	0	0
S_2	0	0	0	1	1	0	0	0
S_3	0	1	1	1	1	1	1	0

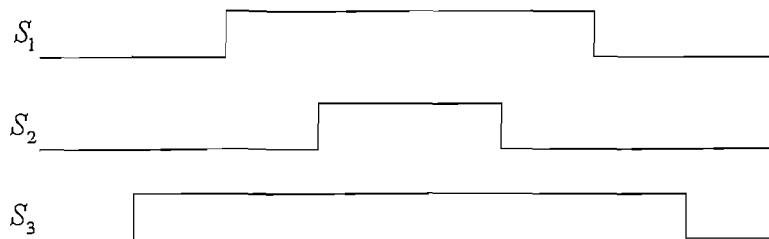


Figure 2-20 Sector 5 SVPWM

The switching time for each leg of the three-phase bridge is determined as follows

$$S_1 \Rightarrow T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1 + 2x + y)}{2} \quad (2-50)$$

$$S_2 \Rightarrow \frac{T_0}{2} = T_s \cdot \frac{(1+y)}{2} \quad (2-51)$$

$$S_3 \Rightarrow T_1 + T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1-y)}{2} \quad (2-52)$$

Sector 6

Sector 6 is bounded by vector $\vec{V}_6$ and vector $\vec{V}_1$. In this sector the voltage state in terms of the normalized coil voltages is (1,0) during T_1 , (1,-1) during T_2 and (0,0) during T_0 . Using (2-17) this can be expressed as

$$T_s(x, y) = T_1(1, 0) + T_2(1, -1) + T_0(0, 0) \quad (2-53)$$

Using (2-15) and (2-18) T_1 , T_2 and T_0 are determined as follows

$$T_1 = (x + y) \cdot T_s \quad (2-54)$$

$$T_2 = -y \cdot T_s \quad (2-55)$$

$$T_0 = T_s - T_1 - T_2 = (1 - x) \cdot T_s \quad (2-56)$$

The switching states and symmetric SVPWM waveforms for sector 6 over a full switching period is shown in Figure 2-21

	$\frac{T_0}{2}$	T_1	T_2	$\frac{T_0}{2}$	$\frac{T_0}{2}$	T_2	T_1	$\frac{T_0}{2}$
S_1	0	1	1	1	1	1	1	0
S_2	0	0	0	1	1	0	0	0
S_3	0	0	1	1	1	1	0	0

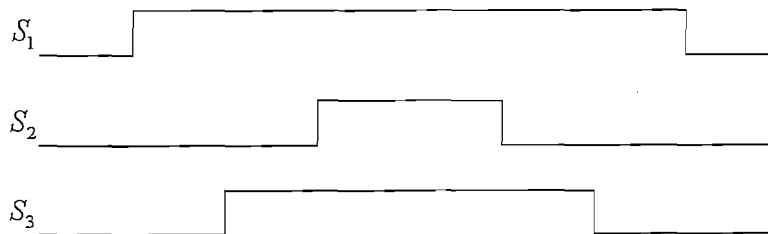


Figure 2-21 Sector 6 SVPWM

The switching time for each leg of the three-phase bridge is determined as follows

$$S_1 \Rightarrow T_1 + T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1+x)}{2} \quad (2-57)$$

$$S_2 \Rightarrow \frac{T_0}{2} = T_s \cdot \frac{(1-x)}{2} \quad (2-58)$$

$$S_3 \Rightarrow T_2 + \frac{T_0}{2} = T_s \cdot \frac{(1-x-2y)}{2} \quad (2-59)$$

An advantage of SVPWM when compared to other PWM strategies is that the adjacent voltage vectors only differ with one switch state, thus minimizing the IGBT switching loss. From Table 2-1 it is evident that the coil voltages $V1$ and $V2$ are never simultaneously at $+V_{dc}$ or simultaneously at $-V_{dc}$. This represents a reduction in voltage region when compared to a 1 DOF AMB that is driven by two H-bridges or two modified H-bridges with either bipolar or unipolar PWM schemes.

2.5 PCB design

In high speed PCB design parasitic circuit elements affect signal propagation in the form of ringing and reflections while the unintended interaction between signals results in cross talk that compromise the signal integrity in such a design [39].

The primary factors that classify a PCB design as high speed are the interconnect length and the signal rise time, not necessarily clock frequency. If the interconnect length is longer than one-sixth of the effective length of the signal 10% to 90% rise time, the design may be classified as high speed and interconnects have to be modeled as transmission lines and terminated correctly to preserve signal integrity. To model the transmission line accurately the distributed parameter model of the interconnect must be used, as opposed to the lumped parameter model in the case of low speed designs [40].

Signal integrity analysis of high speed designs require computational electromagnetic field solvers, input-output buffer information specification (IBIS) models of the transmitters and receivers, electrical network solvers and EMI analyzers [41], [42].

When designing a PCB the designer should determine to what extent signal integrity must be considered during PCB layout by addressing the following issues [43]:

- Is the PCB design high speed based on the signal 10% to 90% rise time?
- Can the PCB layout be adapted to avoid treating the signal as high speed?

- Can signal integrity simulation and transmission line models be avoided?

EMC control measures apply at three levels in electronic systems, primary, secondary and tertiary. Primary control of EMC involves circuit design measures such as power supply decoupling, signal bandwidth limitation, grounding and PCB layout. The secondary control of EMC focuses on looms and interfaces between circuits, while tertiary EMC control involves shielding equipment [44]. PCB design for good signal integrity and primary EMC control measures are thus complimentary functions.

2.5.1 Signal integrity

Inspection of a spectral power density plot of a random digital pulse train clocked at f_{clock} displays an overall -20dB/decade slope from f_{clock} up to a frequency known as the knee frequency, f_{knee} . At f_{knee} the spectral amplitude is reduced by -6dB after which the spectrum rolls off at more than -20dB/decade. The important time domain characteristics of a digital signal are determined by the signals spectrum below f_{knee} where most of the energy in the digital signal is concentrated [40].

The knee frequency of a digital signal is related to the 10% to 90% rise time of the signal and not to the clock frequency and is expressed as

$$f_{knee} = \frac{0.5}{t_{rise}} \quad (2-60)$$

Ideally a digital circuit should have a bandwidth equal to f_{knee} in order to process a digital signal without any distortion [40]. EMI generated by a high speed digital circuit will occur at frequencies two to three times beyond the knee frequency, thus f_{knee} can't be used to predict EMC [43].

The length of a signal's rising edge can be determined from the signals 10% to 90% rise time and the propagation delay experienced by that signal in a particular medium. The propagation delay of a signal traveling in air is 33.36 ps/cm. The signal propagation delay is proportional to the square root of the dielectric constant of the medium it travels in. The length of a signal rising edge is

$$l_{rise} = \frac{t_{rise}}{33.36 \cdot \sqrt{\epsilon_r}} \quad (2-61)$$

where:

- l_{rise} = Length of the signal rising edge in cm
 t_{rise} = 10% to 90% rise time of the signal in ps
 ϵ_r = Relative permittivity of the PCB dielectric material, 4.5 for FR4.

If the interconnect length on a PCB between a driver and a receiver is longer than $l_{rise}/6$, the interconnects have to be modeled as transmission lines and terminated correctly to preserve signal integrity. As an alternative the PCB tracks should be kept within the limit of $l_{rise}/6$ or the signal slew rate of the driver must be limited, thus avoiding the use of signal integrity simulation and transmission line modeling [43].

A set of accurate closed form expressions to determine characteristic impedance of microstrip transmission lines is given in [45], a simplified set of these equations are available in [40].

2.5.2 Layer structure

The layer structure of a multi-layer PCB specifies the type of signal for each layer and the sequence of the layers. The layer structure will be influenced by manufacturing process constraints, cost and the type of component packages used in the design. Mechanically the layers should be symmetrical with even numbers of layers and even areas of solid plane to prevent the PCB from warping [40].

Although the cost of the PCB is proportional to the number of layers and the board surface area, the design should not be forced into the fewest number of layers possible since the increased current density will reduce the power handling capacity of the PCB and the closer spaced tracks will be more susceptible to crosstalk. Specifications such as IPC-2221 and MIL-STD-275 contain data that can be used to estimate the temperature rise of a PCB track based on current density, however the use of these specifications is restricted to a specific PCB and track geometry and should not be regarded as universally applicable [46].

A dedicated layer of solid ground plane, without slots, provides the most effective grounding scheme to minimize cross talk. According to [40], crosstalk of 1% to 3% between adjacent PCB tracks is acceptable in a solid ground plane design. The crosstalk between two PCB tracks is a function of the distance between the tracks and their height above a solid ground plane, and may be expressed as [40]:

$$Crosstalk \approx \frac{1}{1 + \left(\frac{d}{h}\right)^2} \quad (2-62)$$

where d is the distance between the tracks and h is the height of the tracks above a solid ground plane, as shown in Figure 2-14. Equation (2-62) can be used as a guideline to determine the spacing between tracks in a high speed PCB design.

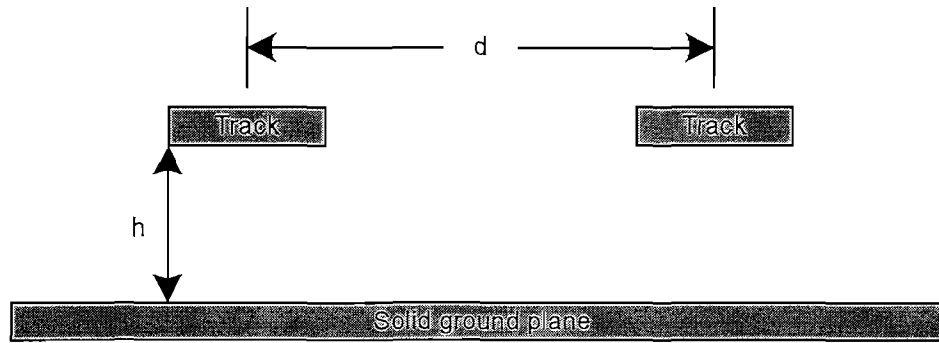


Figure 2-22 Crosstalk between two PCB tracks

A power plane situated immediately above or below the ground plane in the layer structure will maximize the capacitive coupling between these layers and form an effective high frequency decoupling capacitor according to the equation for capacitance between two plates [43]

$$C = \frac{\epsilon_0 \cdot \epsilon_r \cdot A}{d} \quad (2-63)$$

where:

- A = Common area between the ground plane and the power plane in m^2
- D = Thickness of PCB material between the ground plane and the power plane in m
- ϵ_r = Relative permittivity of the PCB dielectric material, 4.5 for FR4
- ϵ_0 = Permittivity of free space, 8.85×10^{-12} .

The capacitance created by the PCB power plane and ground plane may be small, however it forms a high quality decoupling component due to its relatively low impedance at high frequency [43].

For a component package such as a fine pitch (1 mm) ball grid array (BGA) the standard PCB process technology will allow 5 to 6 mil minimum track width and spacing between tracks (1 mil = 0,0254 mm). The PCB design rule shown in Figure 2-15 is typical for a BGA package using standard PCB process technology. The size of the BGA package will play a major role in determining the number of layers required to route the PCB effectively [47].

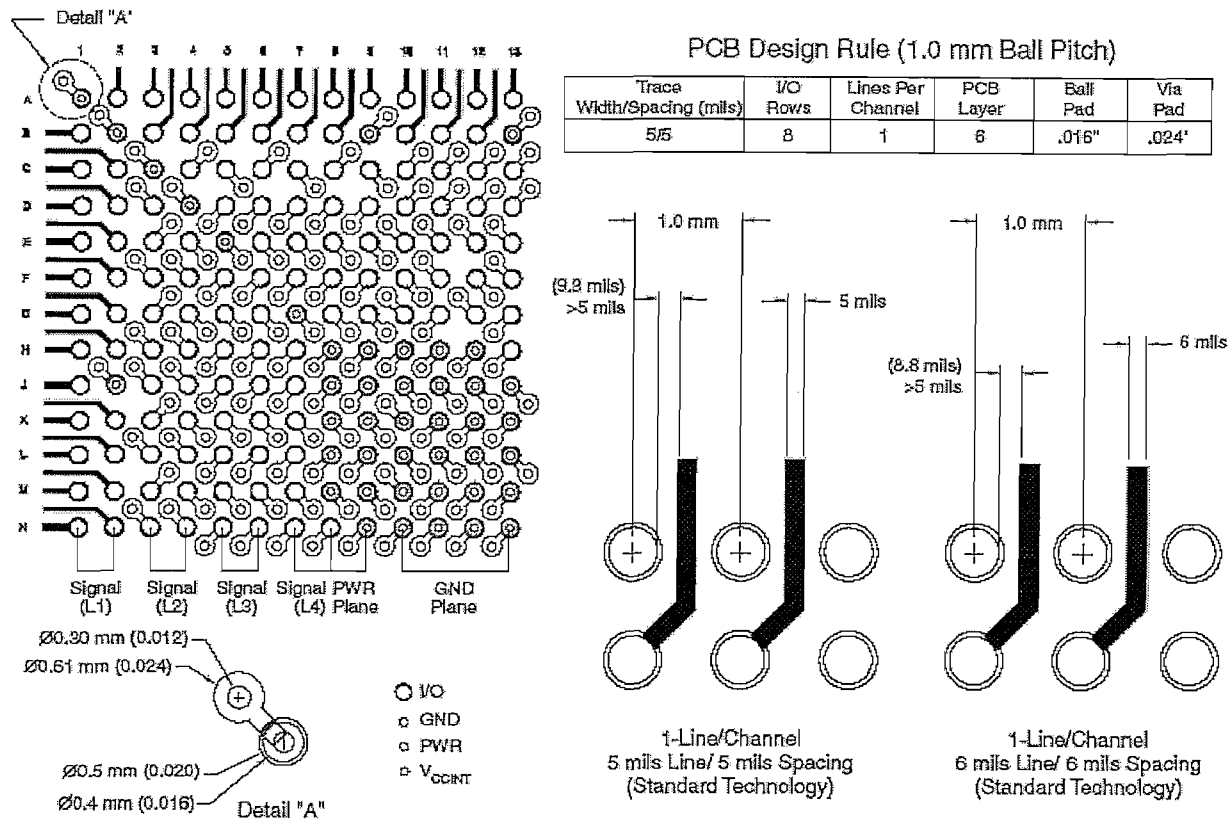


Figure 2-23 BGA design rule [47]

An example of a multilayer PCB layer structure with typical manufacturing dimensions is shown in Figure 2-16. The layer structure is based on a ten layer PCB with 35 μm copper and a 1.6 mm total thickness. The multilayer structure is composed of alternating layers of core material and prepreg epoxy [40].

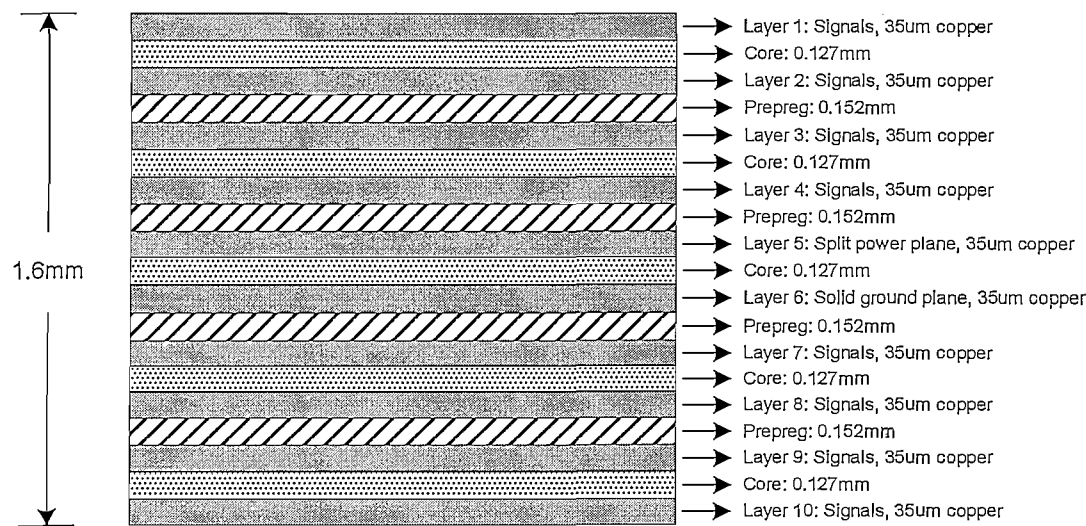


Figure 2-24 Multilayer PCB structure

2.5.3 Power amplifier layout

The power amplifier layout will require some form of heat sink to manage the power dissipated by the power components. The power components can be mechanically fastened to a heat sink and wired to the controller PCB or the power amplifier circuit can be routed on insulated metal substrate, allowing the use of surface mount devices (SMD) for the power components, similar to a PCB. The use of SMD power components on insulated metal substrate result in a smaller loop area and reduced lead inductance for the power amplifier circuit that reduces EMI coupling [44]. Insulated metal substrate is a three layer system consisting of a circuit layer, a dielectric layer and a base layer. The circuit layer consists of printed circuit copper ranging in thickness from $35\mu\text{m}$ to $350\mu\text{m}$. The dielectric layer bonds the circuit layer and the base layer together, providing electrical isolation between these layers with minimum thermal resistance. The base layer is made of aluminum and available in various thicknesses. The insulated metal substrate concept is shown in Figure 2-17.

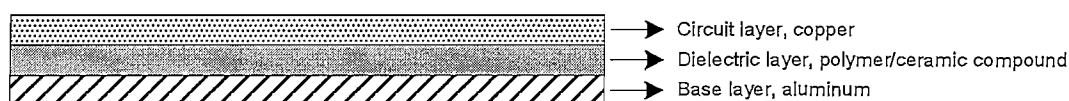


Figure 2-25 Insulated metal substrate

Insulated metal substrate benefits include reduced thermal impedance, more compact layout, increased power density, fewer interconnects and mounting hardware [48].

2.6 Conclusion

In Chapter 2 the operating principle and advantages of AMBs were discussed. The benefits of self-sensing AMBs were highlighted. The amplitude modulation approach of self-sensing was emphasized. The benefit of digital signal processing, in particular the FPGA and DSP co-processor architecture was discussed. Linear, switching and hybrid power amplifiers used in AMB systems were compared. Finally various aspects of PCB design, including signal integrity were highlighted. Chapter 3 addresses the conceptual design of the integrated co-processor based power electronic drive.

Chapter 3

Conceptual design

Chapter 3 relates the conceptual design of the integrated co-processor based power electronic drive. The integrated drive is a subsystem in a complete AMB system. The conceptual design forms part of the process of compiling a subsystem development specification for the integrated drive, in conjunction with the McTronX Research Group. Circuit simulations and trade-off studies will serve as the basis for the conceptual design. The conceptual design, and ultimately the development specification, will determine the architecture, functionality and interfaces of the integrated drive.

3.1 System architecture

The high level system architecture of the AMB, of which the integrated co-processor based power electronic drive is a subsystem, shall be capable of controlling an AMB in five degrees of freedom. The integrated drive subsystem shall consist of two power amplifiers and a controller, the minimum configuration required to suspend an AMB rotor in one degree of freedom since two electromagnets are required per axis. This system architecture is shown in Figure 3-1.

The co-processor based power electronic drive is a mixed signal assembly that contains power, digital and analog circuitry. The digital and power circuitry is noisy while the analog circuitry is highly susceptible to electronic noise. For this reason the power amplifier, digital controller and analog circuitry will be partitioned in an attempt to minimize the interference between these circuits [44].

The integrated drive will consist of the following major functional units:

- a power amplifier assembly that will make provision for two amplifier stages,
- a digital controller assembly, including an electronic supply and
- an analog interface assembly.

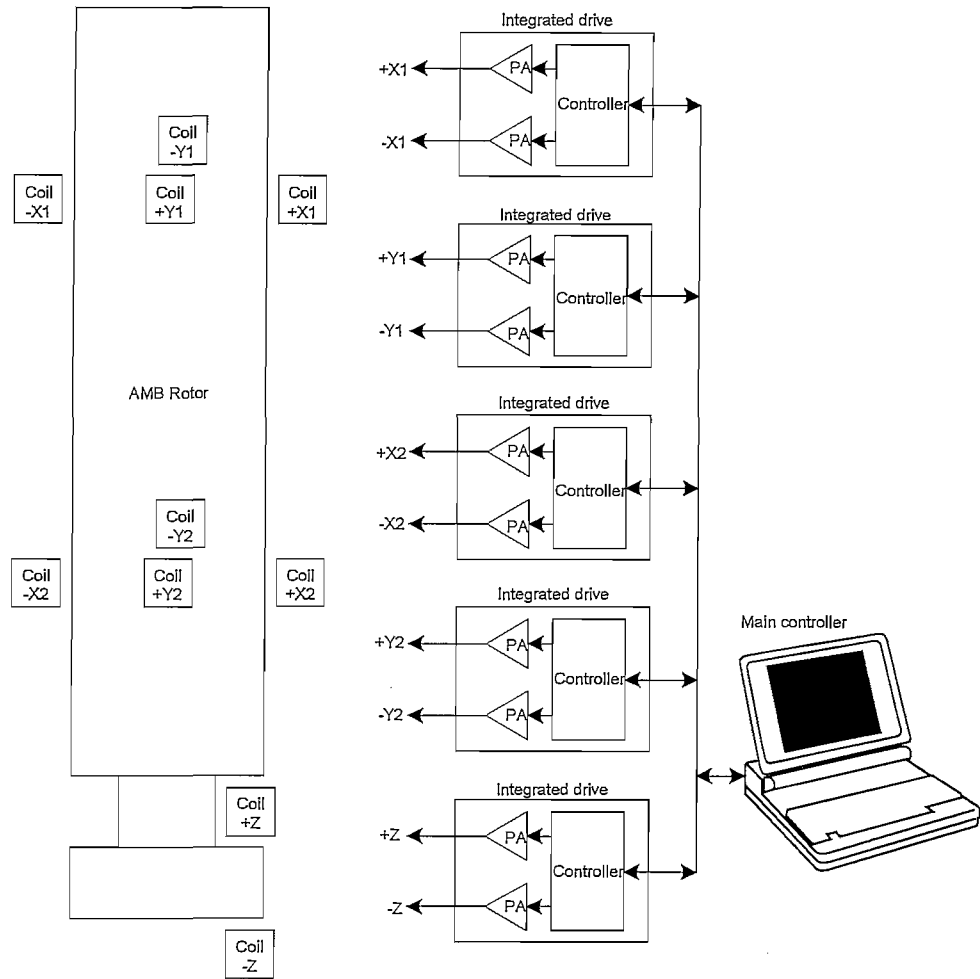


Figure 3-1 System architecture for a 5 DOF AMB

Although the integrated drive will be used primarily as a hardware platform to investigate self-sensing techniques for AMBs, it must also make provision to control a sensor based AMB implementation. The integrated drive architecture is shown in Figure 3-2.

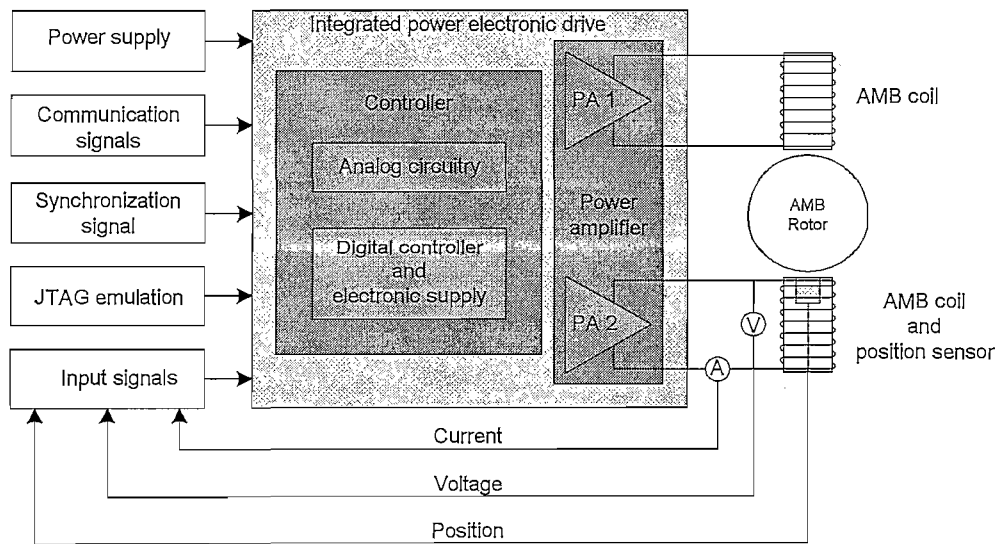


Figure 3-2 Integrated drive architecture

The integrated drive will be powered from an external power supply with a direct current (DC) input voltage of 50 V up to 310 V, with 150 V DC being the most likely supply voltage. The electronic supply that is part of the digital controller will step down and regulate the external supply into lower DC voltages required by the digital controller, analog circuitry and the power amplifier. Communication signals will facilitate communication between individual controllers and a main controller as shown in Figure 3-1. An external synchronization signal will ensure that clock domains between the integrated drives are synchronized, allowing digital sampling of sensitive analog signals to be less susceptible to switching noise. A JTAG emulation interface will provide a programming and debugging interface for the digital processors used on the digital controller assembly. The integrated drive requires the capability to interface to a variety of input signals such as current, voltage and position, from the AMB.

Members of the McTronX Research Group will do the detail component design of the analog interface circuitry. The interfaces, component placement and PCB design of the analog interface circuitry will form part of this work although the primary focus will be the development of the digital controller assembly and the power amplifier assembly.

3.2 Power amplifier

The power amplifier will be powered from an external power supply with a DC input voltage of 50 V to 310 V. The power amplifier will receive additional external input from the digital controller and electronic supply. The power amplifier will provide the necessary current and voltage to the AMB electromagnets as well as voltage and current sensor outputs to the analog circuitry. A functional block diagram of the amplifier is shown in Figure 3-3.

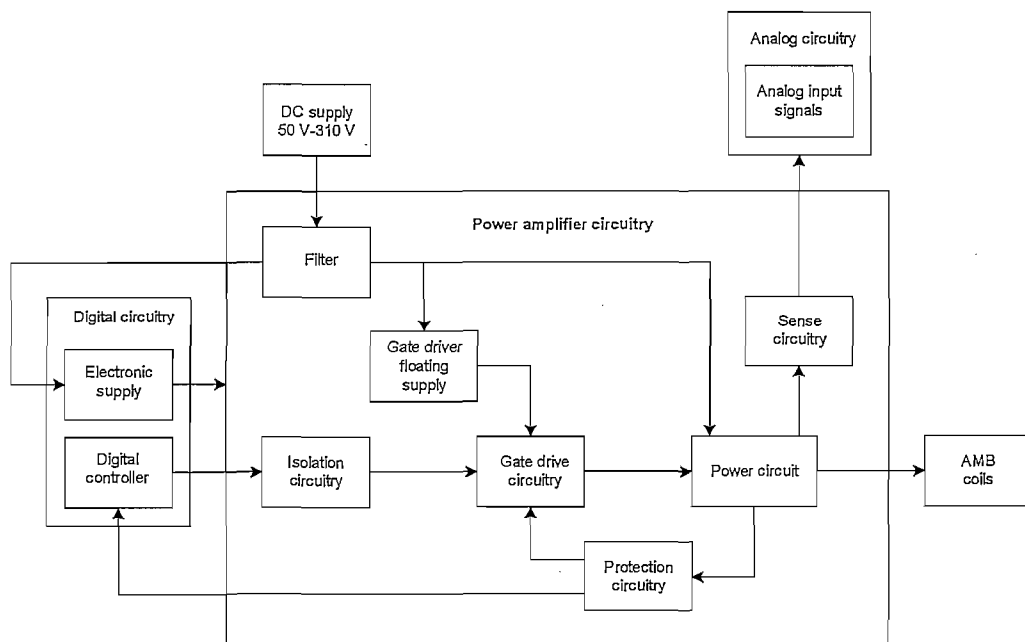


Figure 3-3 Power amplifier block diagram

The power amplifier will consist of the following functional units:

- Isolation circuitry
- Gate drive circuitry
- Power circuit
- Sense circuitry
- Gate driver floating supply
- Protection circuitry
- Filter

In the following sections a conceptual design will be proposed for each of the power amplifiers functional units. This information will assist in developing the integrated drive specification and subsequently performing the detail design.

3.2.1 Isolation circuitry

Isolation circuitry is required to establish an isolation boundary between the digital controller circuitry and the power amplifier gate drive circuitry with minimum signal propagation delay. The function of the isolation circuitry is two fold. Firstly it protects the digital circuitry in case of a power amplifier catastrophic malfunction and secondly it provides isolation between the power amplifier ground and the digital circuit ground in order to control signal return paths. The isolation may be galvanic by means of a transformer or optical by means of an opto-coupler or fiber optics depending on the characteristics of the signal to be isolated and the physical distance between the circuits to be isolated [36]. Figure 3-4 shows a schematic example of optical isolation between two grounds, GND 1 and GND 2, by means of an opto-coupler integrated circuit (IC) shown within the dashed lines.

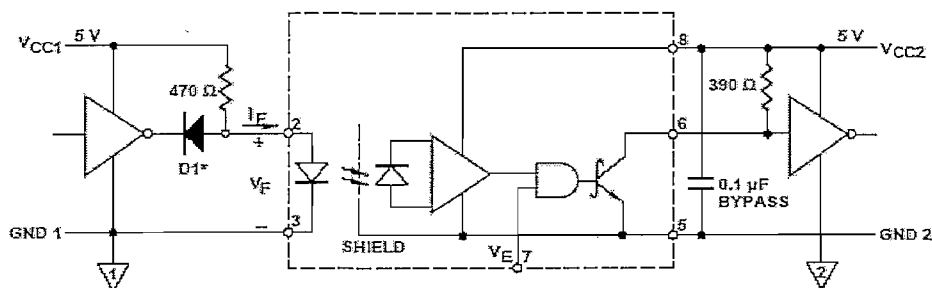


Figure 3-4 Optical isolation

The shield between the emitter and receiver in Figure 3-4 minimizes the capacitance between these components within the opto-coupler thus avoiding possible retriggering at turn-on and turn-off of the power amplifier switching devices.

If the gate drive signal is required to remain active for an extended period of time, as would be the case for 100% duty cycle condition, isolation by means of a transformer will require additional circuitry to satisfy this requirement. In such a case the opto-coupler isolation may be the preferred means to implement the isolation circuitry.

3.2.2 Gate drive circuitry

The type of gate drive required for the power amplifier will depend on the type of switching device used. IGBTs are preferred in applications over 100 V and MOSFETs are preferred in applications under 100 V [9], [30]. Since the supply voltage requirement for the integrated drive is 50 V to 310 V DC, the power amplifier switching devices will be IGBTs.

The function of the gate drive circuit is to provide the necessary voltage and current required to properly drive the IGBTs, including the level shift requirements for the gate drive signal to the upper IGBT in a bridge configuration as listed below [49]:

- The gate voltage must be 10 V to 15 V higher than the IGBT collector potential that is connected directly to the 310 V DC supply voltage.
- The ground referenced gate control signal has to be level shifted to the IGBT emitter potential that is connected to the mid point of the bridge.
- The power dissipated in the gate drive circuitry should not significantly affect the overall efficiency of the power amplifier.

Given these requirements two options exist to realize the gate drive circuit. The gate drive circuit may be designed using discrete components or an integrated gate drive IC may be used. The discrete design will consume more area on a PCB and be less reliable than an integrated component.

Integrated gate drive ICs offer additional features such as under voltage lockout, pulse-for-pulse shutdown and Schmitt triggered input for improved noise immunity. Integrated gate drivers are available that contain circuitry to drive a ground referenced power transistor and a high side power transistor. A functional block diagram of a typical integrated gate drive IC is shown in Figure 3-5 within the dashed lines. A bootstrap supply is required to generate a gate drive voltage higher than the supply voltage for the high side power transistor. This function is provided by the external diode and capacitor C_{BOOT} in Figure 3-5. The capacitor charges to V_{cc} through the diode every time the bottom power transistor switches on. This simple bootstrap supply has limitations in applications that require 100% duty cycle operation and may have to be replaced with a more reliable floating supply.

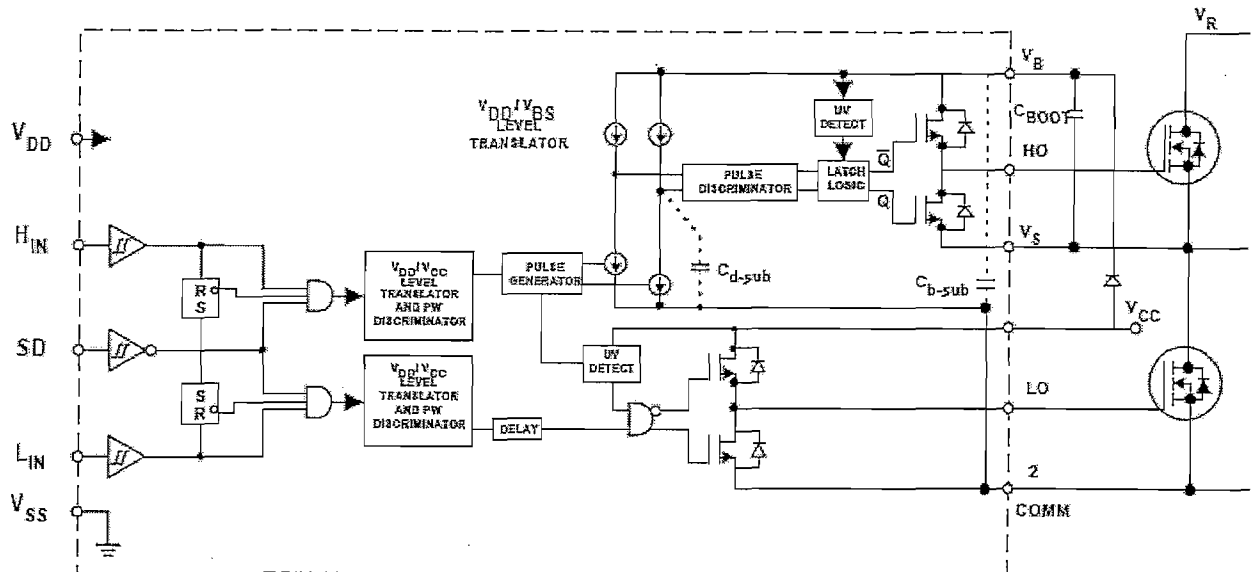


Figure 3-5 Integrated gate driver [49]

An integrated gate drive IC is considered the preferred option for the gate drive circuitry.

3.2.3 Power circuit

As stated in Chapter 2 the single phase H-bridge converter and the modified H-bridge converter for unidirectional current flow are the two preferred switching amplifier topologies in AMB applications [9], [30], [32]. The space vector PWM technique has also been proposed for AMBs [33]. The power circuit will make provision for three-phase functionality in order to fully exploit all of these options. Since two power amplifiers are required for each integrated drive, the power circuit will consist of dual three-phase bridges as shown in Figure 3-6. The power handling capability required of the power amplifier is a nominal bridge voltage variable between 50 V and 150 V with a nominal output current of $7.5 A_{\text{rms}}$ and a peak output current of $15 A_{\text{peak}}$.

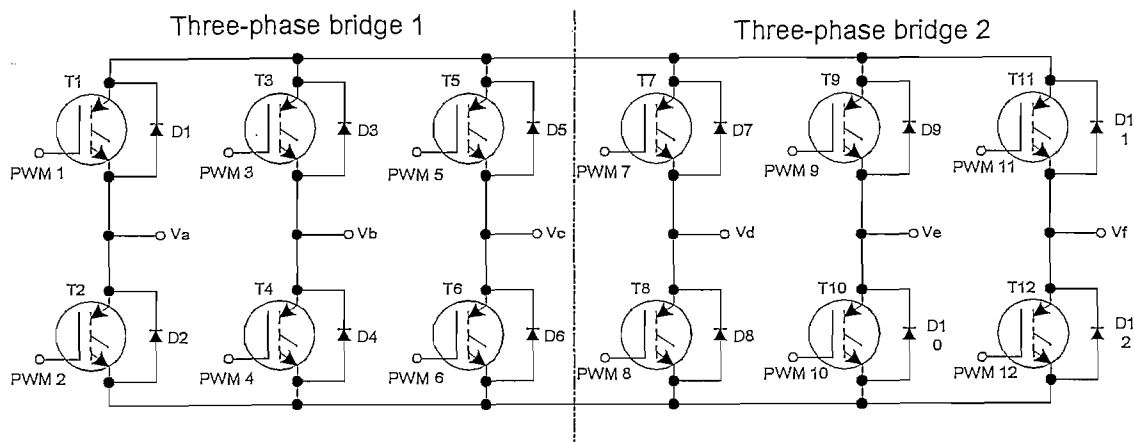


Figure 3-6 Power circuit

The power circuit topology in Figure 3-6 can be configured to drive two AMB electromagnets by combining any two half bridge legs to form an H-bridge or modified H-bridge stage. Referring to Figure 3-6, a modified H-bridge can be formed by combining IGBT $T1$ and diode $D2$ to form one leg of the bridge and IGBT $T4$ and diode $D3$ to form the other leg of the bridge. Similarly an H-bridge can be formed by combining IGBTs $T9$ and $T10$ to form one leg of the bridge and IGBTs $T11$ and $T12$ to form the other leg of the bridge. Numerous IGBT and diode combinations are possible for both H-bridge or modified H-bridge stages.

PSpice® simulation models were used to compare the functional performance of a modified H-bridge circuit with an H-bridge circuit when driven with uni-polar PWM and bipolar PWM schemes. The parameters for all the simulation runs are identical and listed below:

- Switching frequency: 20 KHz
- Supply voltage: 50 V
- Duty cycle: 53 %
- Electromagnet resistance: 0.2Ω
- Electromagnet inductance: 7.2 mH

Modified H-bridge with bipolar PWM

The modified H-bridge with bipolar PWM is the most widely used topology for industrial AMB power amplifiers [32]. The modified H-bridge simulation schematic is shown in Figure 3-7.

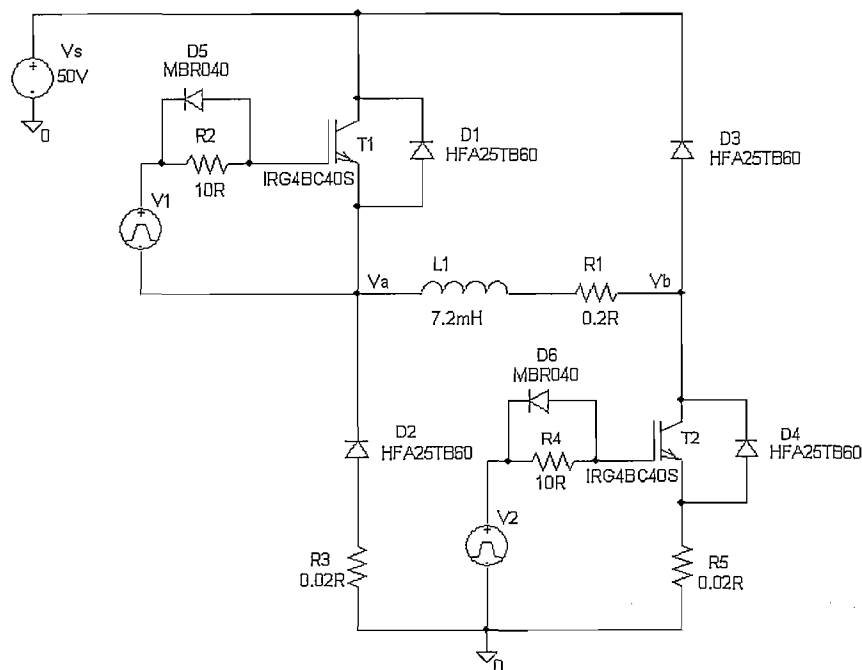


Figure 3-7 Modified H-bridge simulation circuit

For bipolar PWM modulation, the IGBTs $T1$ and $T2$ are switched simultaneously with the same pulse width and thus do not require any blanking time between switching transitions. This topology does not make provision for negative load current, however it does allow negative load voltage. There are two controlled switching states applicable to this topology, during the first state, IGBTs $T1$ and $T2$ are switched on simultaneously and current increases through the load. The load current during the first state is

$$i(t) = \frac{V_s - 2 \cdot V_{on}}{R_L + R_s} \left(1 - e^{\frac{-t R_L}{L}} \right) + I_0 \cdot e^{\frac{-t R_L}{L}} \quad (3-1)$$

During the second state IGBTs $T1$ and $T2$ are switched off simultaneously and current decreases through the load. The load current during the second state is

$$i(t) = -\frac{V_s - 2 \cdot V_{on}}{R_L + R_s} \left(1 - e^{\frac{-t R_L}{L}} \right) + I_0 \cdot e^{\frac{-t R_L}{L}} \quad (3-2)$$

The simulated load current for this mode of operation is shown in Figure 3-8. The positive and negative slopes of the load current are not identical due to the finite difference in voltage applied to the load during the on and off time.

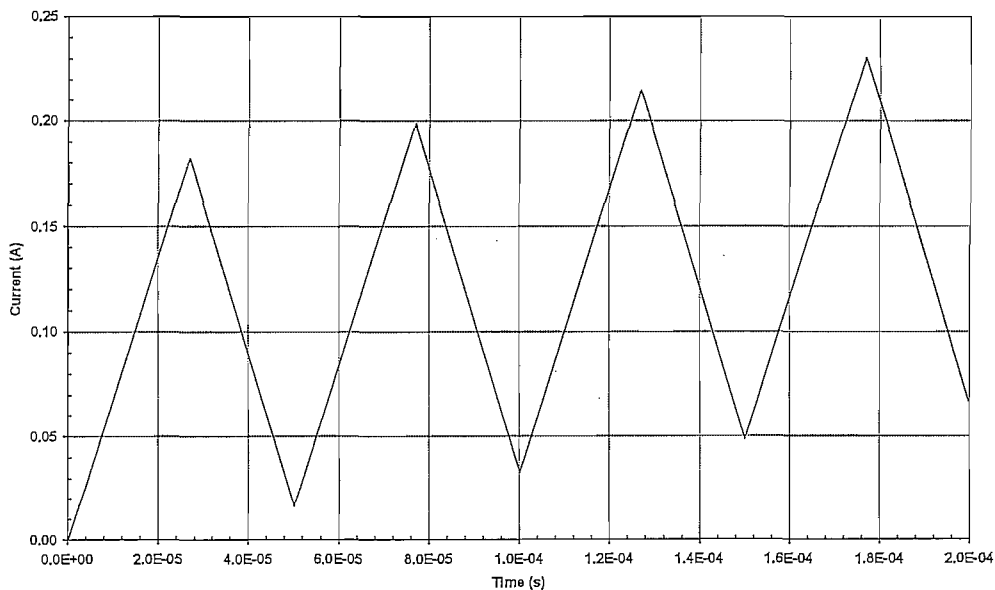


Figure 3-8 Modified H-bridge load current with bipolar PWM

The difference in voltage is due to the conduction volt drop of the IGBTs and the diodes, the voltage drop across the resistance of the electromagnet and the sense resistors. The simulated load voltage for this mode of operation is shown in Figure 3-9. During the first switching state,

when IGBTs $T1$ and $T2$ are switched on simultaneously, the voltage across the load is positive. During the second switching state, when IGBTs $T1$ and $T2$ are switched off simultaneously, the voltage across the load is negative. When the load voltage is positive energy is added to the load, conversely when the load voltage is negative energy is removed from the load. The duty cycle determines how much energy is added or removed from the load every switching cycle.

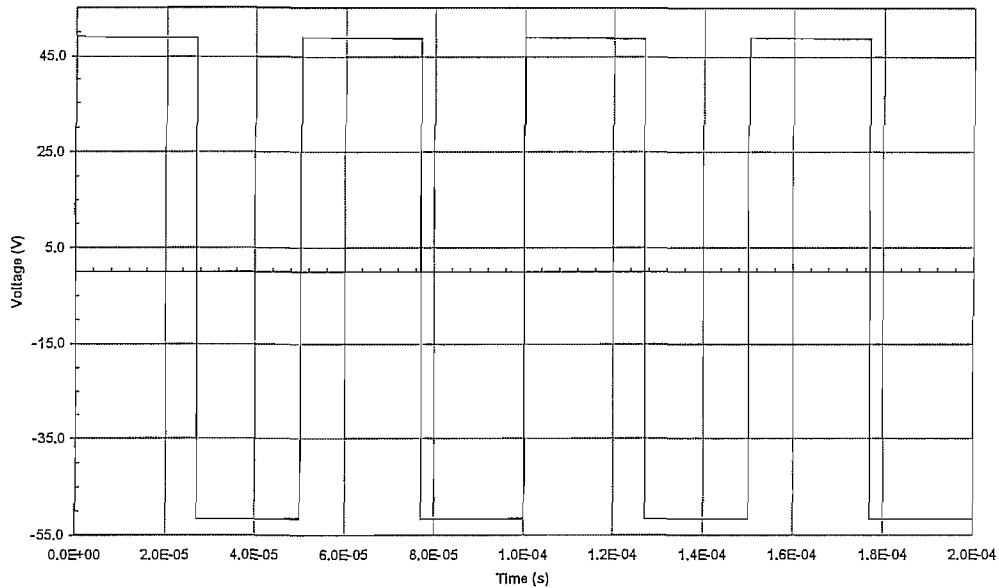


Figure 3-9 Modified H-bridge load voltage with bipolar PWM

This topology uses fewer components than the H-bridge and thus exhibits lower switching loss and improved reliability when compared to the H-bridge topology. The current harmonic spectrum for this topology with bipolar PWM is shown in Figure 3-10.

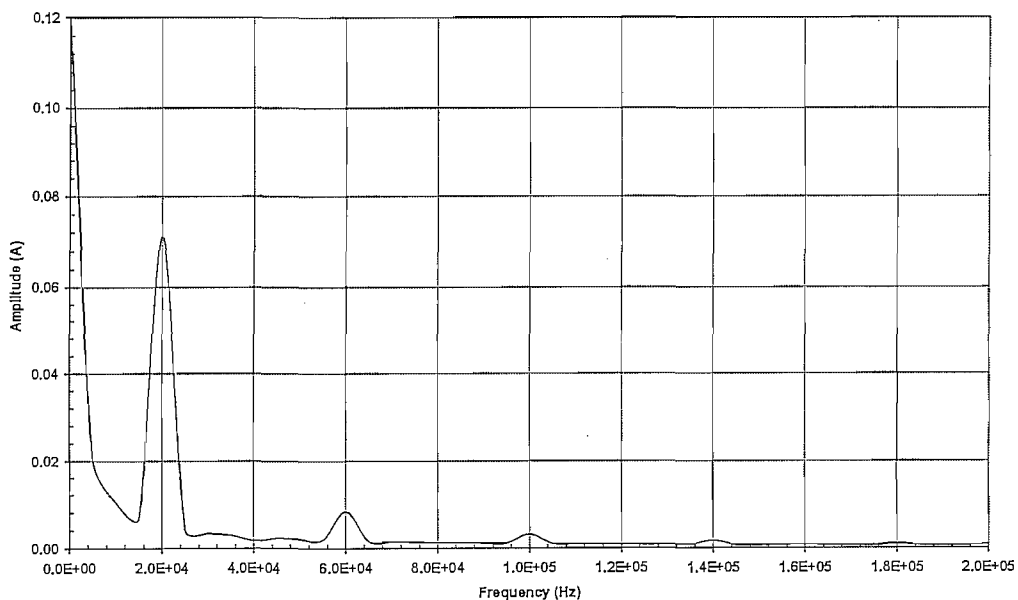


Figure 3-10 Current harmonic spectrum for modified H-bridge with bipolar PWM

The current harmonic distortion can be improved by using uni-polar PWM instead of bipolar PWM [30].

Modified H-bridge with uni-polar PWM

The modified H-bridge has four controlled switching states when operated with uni-polar PWM [30]. Referring to Figure 3-7, in the first state IGBTs $T1$ and $T2$ are switched simultaneously and current increases through the load according to (3-1). During the second state IGBT $T1$ is switched off while IGBT $T2$ remains switched on to form a free wheeling path with diode $D2$ and the load current remains constant. During the third switching state IGBT $T1$ is switched on while IGBT $T2$ remains switched on and current increases through the load according to (3-1). During the fourth switching state IGBT $T2$ is switched off while IGBT $T1$ remains switched on to form a free wheeling path with diode $D3$ and the load current remains constant. During switching states one and three energy is added to the load. During switching states two and four energy is effectively maintained in the load. To remove energy from the load IGBTs $T1$ and $T2$ are switched off simultaneously. The simulated load current for this mode of operation is shown in Figure 3-11.

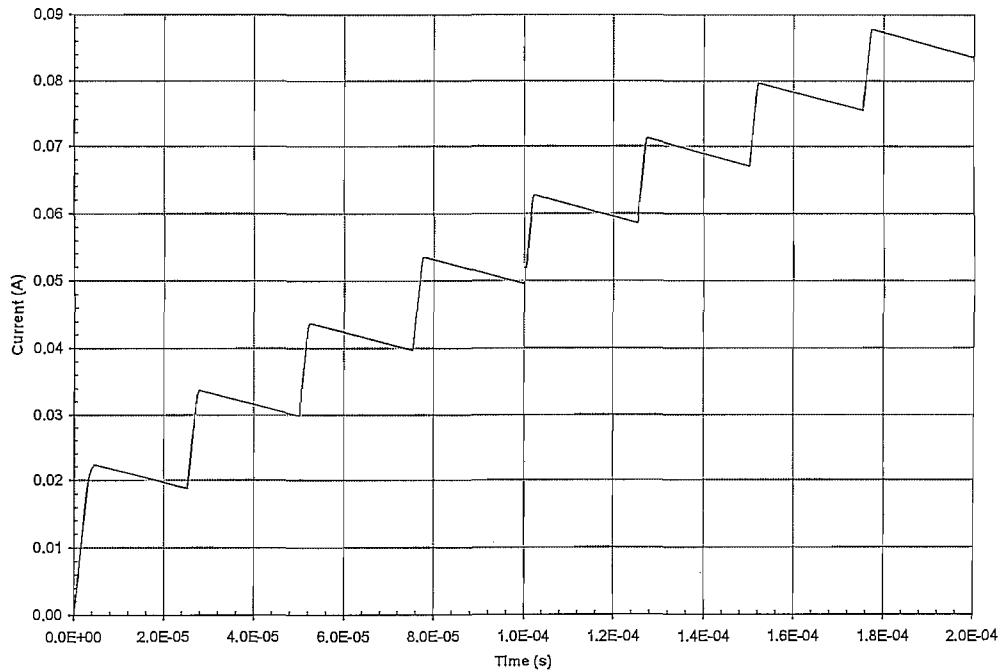


Figure 3-11 Modified H-bridge load current with uni-polar PWM

From Figure 3-11 it can be seen that the load current does not remain constant during switching states two and four but actually decays according to

$$i(t) = -\frac{2 \cdot V_{on}}{R_L + R_s} \left(1 - e^{\frac{-t R_L}{L}} \right) + I_0 \cdot e^{\frac{-t R_L}{L}} \quad (3-3)$$

This is due to the conduction volt drop of the IGBTs and the diodes, the voltage drop across the resistance of the electromagnet and the sense resistors. The simulated load voltage for this mode of operation is shown in Figure 3-12.

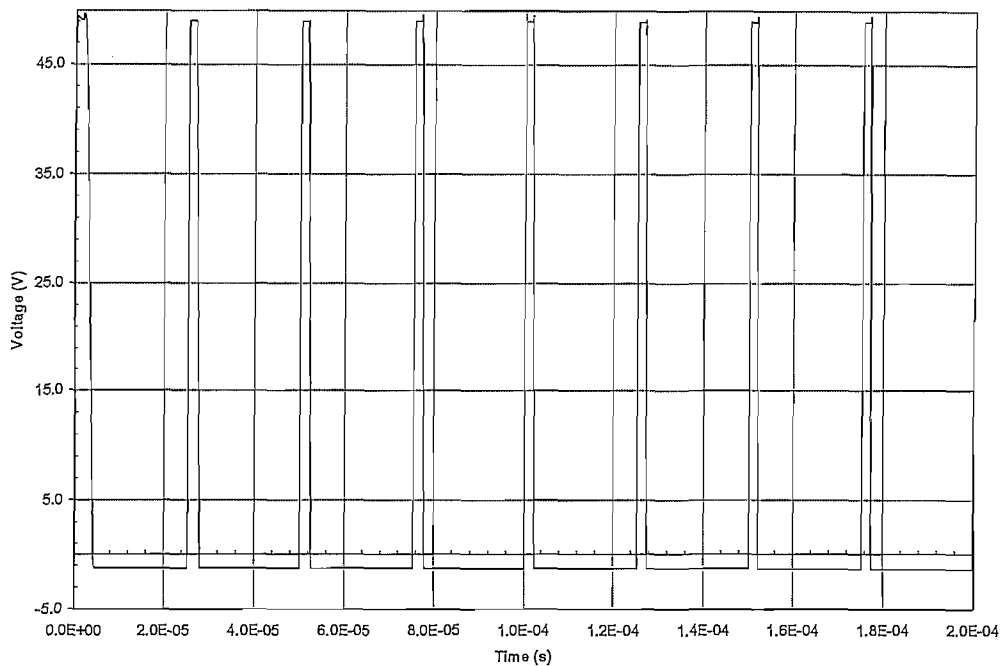


Figure 3-12 Modified H-bridge load voltage with uni-polar PWM

From Figure 3-12 and Figure 3-11 it can be that the frequency of the load voltage and current is 40 KHz, double the switching frequency of the IGBTs. The result is reduced load current ripple for the same switching frequency compared to bipolar PWM. The current harmonic spectrum for this topology with uni-polar PWM is shown in Figure 3-13

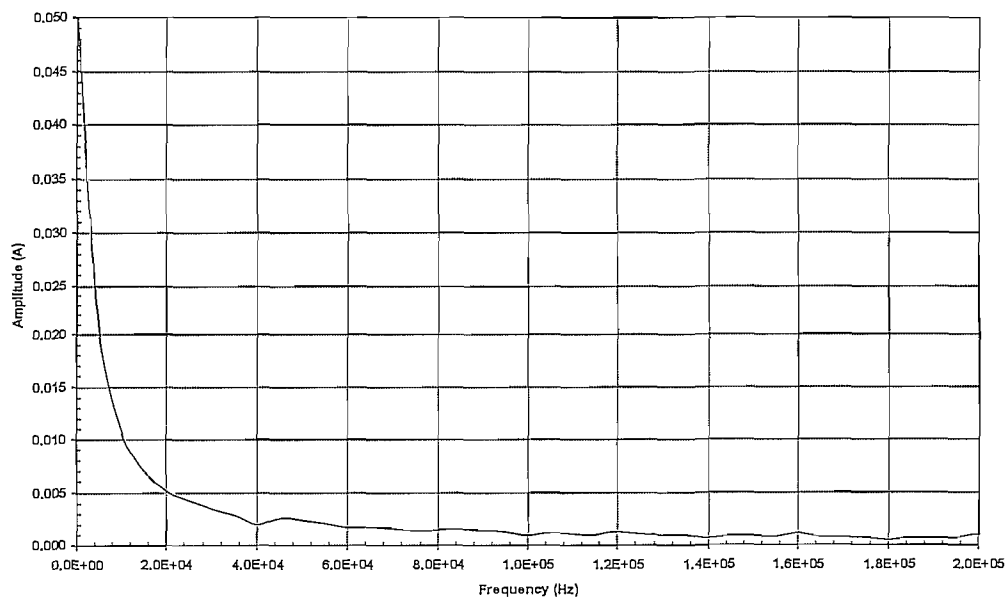


Figure 3-13 Current harmonic spectrum for modified H-bridge with uni-polar PWM

By comparing Figure 3-10 and Figure 3-13 it can be seen that uni-polar PWM exhibits less current harmonic distortion compared to bipolar PWM [30].

H-bridge with bipolar PWM

The H-bridge simulation schematic is shown in Figure 3-14. This topology makes provision for four quadrant operation, i.e. positive and negative load current as well as positive and negative load voltage.

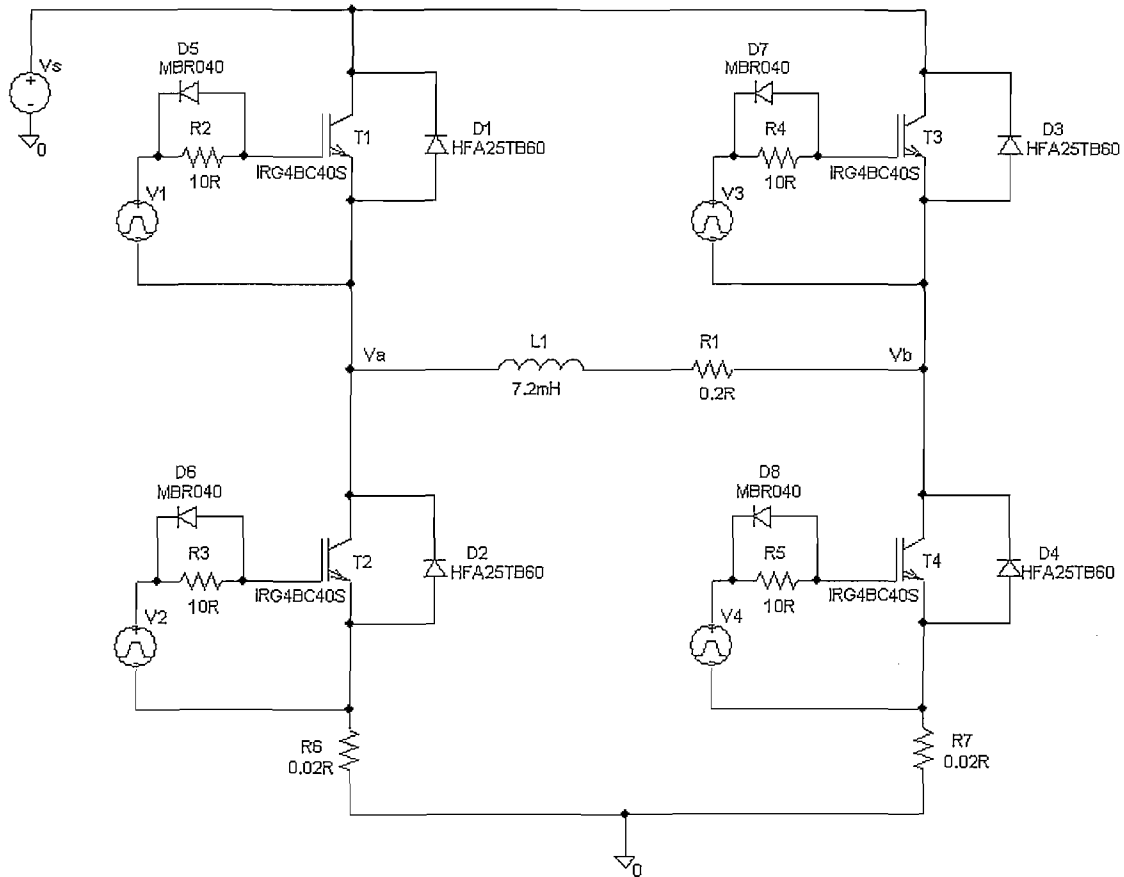


Figure 3-14 H-bridge simulation circuit

There are two controlled switching states applicable to this topology, during the first state, IGBTs $T1$ and $T4$ are switched on simultaneously while IGBTs $T2$ and $T3$ are switched off simultaneously and current increases through the load according to (3-1). During the second state, IGBTs $T1$ and $T4$ are switched off simultaneously while IGBTs $T2$ and $T3$ are switched on simultaneously and current decreases through the load according to (3-2). The polarity of the average load current will depend on the conduction period of IGBTs $T1$ and $T4$ versus the conduction period of IGBTs $T2$ and $T3$. The switching transition between IGBTs in the same leg of the H-bridge requires a short blanking period in the switching transition to prevent cross

conduction current through the leg [36]. The simulated load current for this mode of operation is shown in Figure 3-15.

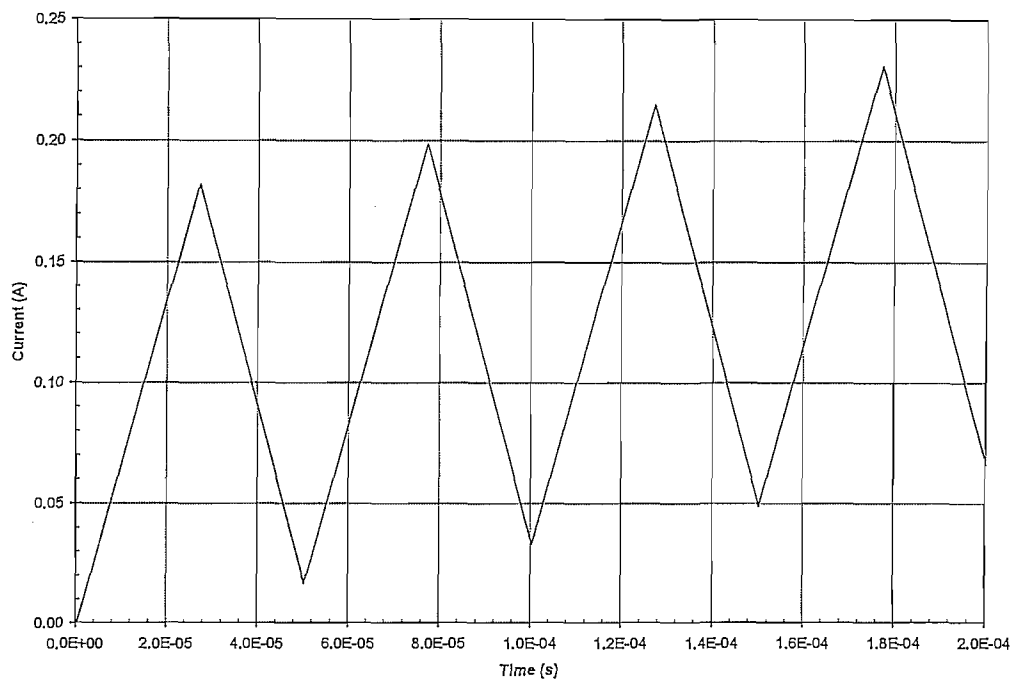


Figure 3-15 H-bridge load current with bipolar PWM

The simulated load voltage for this mode of operation is shown in Figure 3-16. During the first switching state, when IGBTs $T1$ and $T4$ are conducting, the voltage across the load is positive.

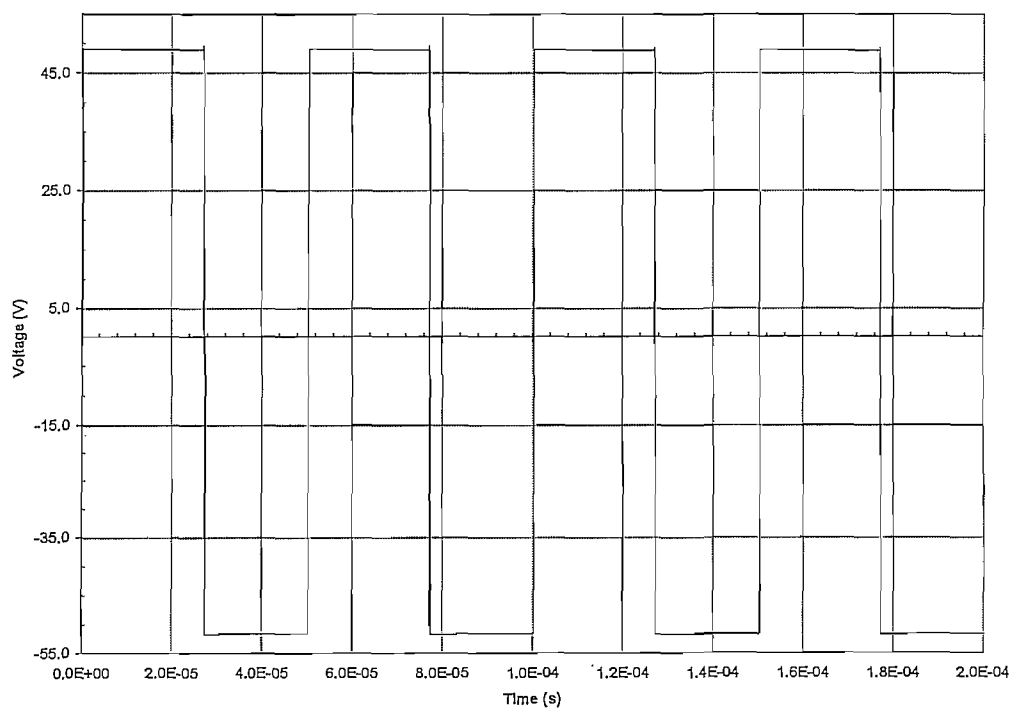


Figure 3-16 H-bridge load voltage with bipolar PWM

During the second switching state, when IGBTs $T2$ and $T3$ are conducting, the voltage across the load is negative. When the period that IGBTs $T1$ and $T4$ are conducting is longer than the conduction period of IGBTs $T2$ and $T3$, the average load voltage is positive. Conversely if IGBTs $T2$ and $T3$ conduct for a longer period than IGBTs $T1$ and $T4$ the average output voltage is negative. If IGBTs $T1$ and $T4$ conduct for the same period as IGBTs $T2$ and $T3$ the average load voltage is zero. The current harmonic spectrum for this topology with bipolar PWM is shown in Figure 3-17

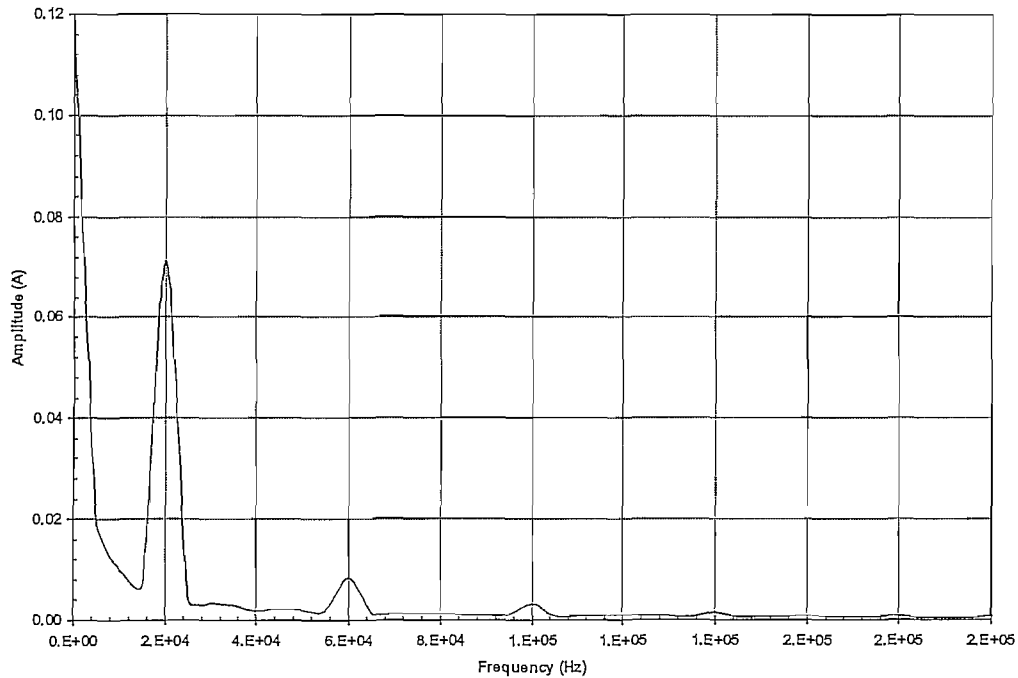


Figure 3-17 Current harmonic spectrum for H-bridge with bipolar PWM

A comparison of Figure 3-10 and Figure 3-17 shows that the current harmonic spectrum for the modified H-bridge and H-bridge topology are very similar when switched with bipolar PWM. The PWM switching scheme has a greater influence on the current harmonic spectrum than the switching topology.

H-bridge with uni-polar PWM

The H-bridge has four controlled switching states when operated with uni-polar PWM [36]. Referring to Figure 3-14, in the first state IGBTs $T1$ and $T4$ are on simultaneously and current increases through the load according to (3-1). During state two IGBT $T4$ remains on while IGBT $T2$ is switched on after a short blanking period subsequent to switching IGBT $T1$ off. In this mode the load is shorted by IGBTs $T2$ and $T4$ while the load current decays slightly according to (3-3). During the third switching state IGBT $T4$ remains on while IGBT $T1$ is switched on after a short blanking period subsequent to switching IGBT $T2$ off and current increases through the load according to (3-1). During switching state four IGBT $T1$ remains on while IGBT $T3$ is

switched on after a short blanking period subsequent to switching IGBT *T4* off. In this mode the load is shorted by IGBTs *T1* and *T3* while the load current decays slightly according to (3-3). The simulated load current for this mode of operation is shown in Figure 3-18.

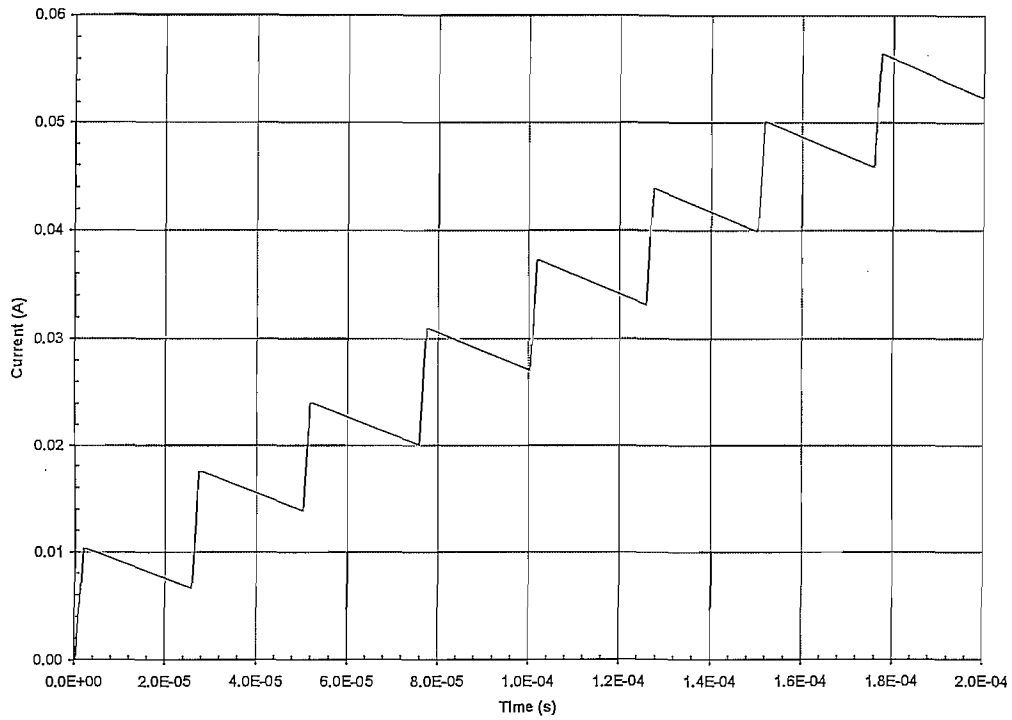


Figure 3-18 H-bridge load current with uni-polar PWM

The simulated load voltage for this mode of operation is shown in Figure 3-19.

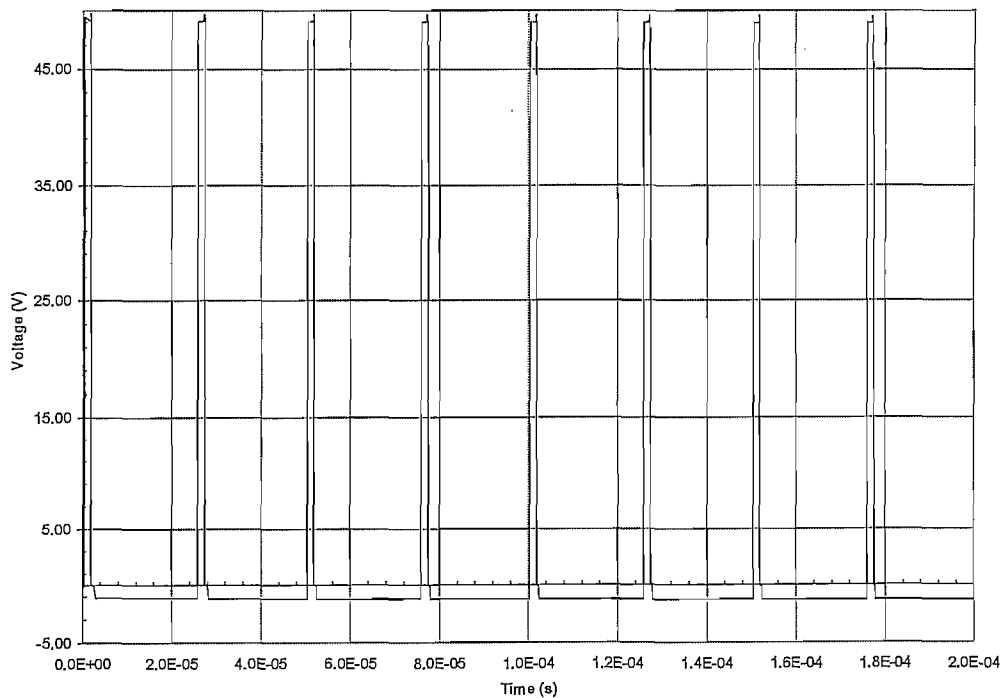


Figure 3-19 H-bridge load voltage with uni-polar PWM

For uni-polar PWM the two legs of the H-bridge are operated as two independent half-bridges and thus the polarity of the output voltage depends on the conduction time of each leg. Referring to Figure 3-14, if the period that IGBT *T1* conducts is longer than the conduction period of IGBT *T3*, the average load voltage is positive. Conversely if IGBT *T3* conducts for a longer period than IGBT *T1* the average output voltage is negative. If IGBTs *T1* and *T3* conduct for the same period the average load voltage is zero.

The current harmonic spectrum for this topology with bipolar PWM is shown in Figure 3-20

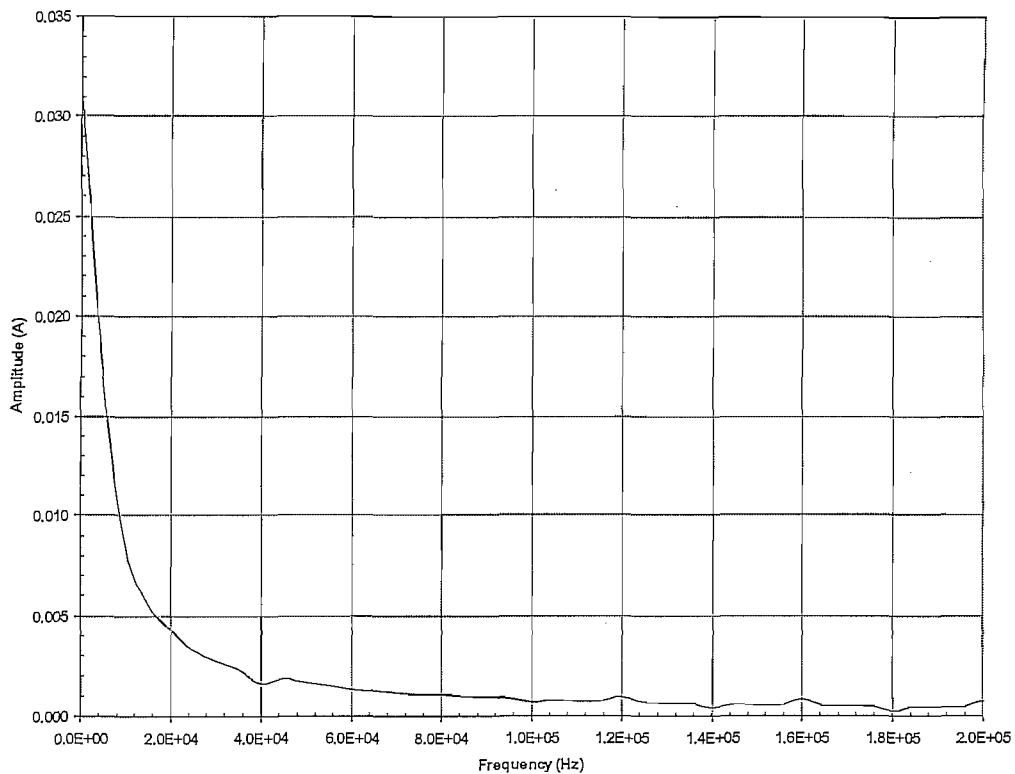


Figure 3-20 Current harmonic spectrum for H-bridge with uni-polar PWM

A comparison Figure 3-17 and Figure 3-20 again shows that uni-polar PWM exhibits less current harmonic distortion compared to bipolar PWM. A comparison of Figure 3-13 and Figure 3-20 shows that the current harmonic spectrum for the modified H-bridge and H-bridge topology are very similar when switched with uni-polar PWM. The PWM switching scheme has a greater influence on the current harmonic spectrum than the switching topology.

Conclusion from the simulation results

The H-bridge and modified H-bridge topologies are very similar, however the uni-polar PWM switching scheme offers superior performance compared to the bipolar PWM switching scheme. The key differences between these topologies and PWM methods are:

- The H-bridge requires blanking time and the modified H-bridge does not.
- The H-bridge can generate negative load current while the modified H-bridge can not.
- The H-bridge and modified H-bridge circuits provide identical results when operated with the same PWM switching scheme and load condition.
- The uni-polar PWM switching scheme has double the output ripple frequency when compared to the bipolar PWM switching scheme for the same switching frequency.
- The uni-polar PWM switching scheme has greater bandwidth and reduced ripple current amplitude when compared to the bipolar PWM switching scheme for the same switching frequency.
- The uni-polar PWM switching scheme has an improved current harmonic spectrum compared to the bipolar PWM switching scheme.

The proposed power circuit shown in Figure 3-6 consisting of dual three-phase bridges will allow for H-bridge or modified H-bridge configurations operated with either bipolar PWM or uni-polar PWM switching schemes. The dual three-phase bridge also makes provision for implementing the space vector PWM technique [33].

3.2.4 Sense circuitry

The purpose of the sense circuitry is to measure the AMB coil voltage and current. The measured voltage and current will be used in self-sensing algorithms to extract rotor position information. The sense circuitry concept is shown in Figure 3-11.

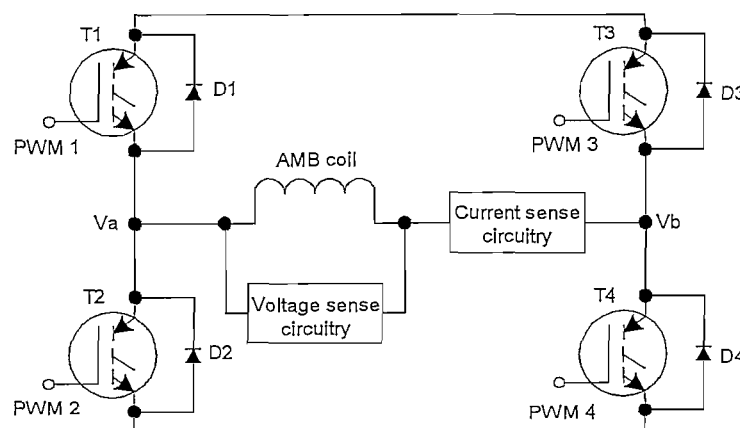


Figure 3-21 Sense circuitry

The sense circuitry should not adversely influence the voltage or current being measured. Ideally the sense circuitry should not dissipate excessive power, nor limit the bandwidth or influence the accuracy of the measured signal. The sense circuitry shouldn't contravene the grounding strategy or violate any isolation boundary. The current and voltage sense circuits

both have a significant common mode voltage component that has to be considered. Additional factors that warrant consideration are power supply to the sense circuitry and the mechanical characteristics of the sense circuitry. An isolation amplifier is regarded as an extreme solution in terms of cost and size and will thus not be considered feasible for the current and voltage sense functions.

The AMB coil current measurement will have a significant DC component with a smaller ripple component at the switching frequency, or double the switching frequency in the case of unipolar PWM modulation. Full duty cycle (100%) operation may also result in continuous coil current. A current sense transformer will not tolerate the 100% duty cycle operating condition, so the remaining fundamental current sensing techniques that can be used for the sense circuitry are a power metal film resistor and an integrated current transducer.

The simplest and cheapest method to sense this current would be to use a non-inductive power metal film resistor in series with the AMB coil to produce a sense voltage representing the coil current. The power resistor allows DC, AC and pulsed current measurement. This is an elegant solution since the power resistor doesn't require any external power supply, nor will it influence the bandwidth of the measured current. These resistors are available in SMD packaging and thus exhibit very low inductance, typically 1 nH, and excellent frequency response. Power metal film resistors are available with accuracies of 0.5% and temperature coefficients of 75 ppm/°C. The disadvantages associated with this approach are the absence of isolation and the need for a high common mode voltage differential amplifier to condition the sensed voltage with sufficient common mode rejection and bandwidth.

An alternative method to sense the current would be to use an integrated current transducer. These devices allow for extremely accurate measurement of DC, AC and pulsed currents with galvanic isolation between the load and the subsequent signal conditioning circuitry. Integrated current sensors are active and make use of the Hall effect to measure current and thus require external power to operate. Additional benefits of integrated current transducers are:

- Excellent accuracy: $\pm 0.3\%$
- Good linearity: $< 0.2\%$
- Wide bandwidth: DC to 200 KHz
- High immunity to external interference
- Current overload capability

Although the integrated current transducer is a more complicated and expensive solution to sense current, it addresses all of the disadvantages associated with the power resistor option.

The integrated current transducer is considered the preferred means to implement the current sense function.

The AMB coil voltage measurement will be at least ± 50 V, possibly as high as ± 150 V, and alternating at the switching frequency, or double the switching frequency in the case of uni-polar PWM modulation. Full duty cycle operation may result in a continuous coil voltage, an operating condition a voltage sense transformer will not tolerate. Compared to the current sense case, the voltage sense circuit has the additional requirement of being able to measure large voltage swings.

The conventional method used to measure large differential voltages in the presence of large common mode voltages, is to use a voltage divider to attenuate the voltage to an acceptable level and then measure the voltage. Integrated differential amplifiers are available that have the attenuating resistors and the differential amplifier on the same die so that they are closely matched over a wide operating temperature range for good common mode rejection and improved accuracy. Alternatively the attenuator can be configured from discrete resistors and a conventional instrumentation amplifier. In order to preserve the accuracy and common mode rejection attainable with an integrated differential amplifier, the external resistors will have to be very accurate, 0.1% to 0.01%, and be placed very close together for thermal equilibrium.

Once again the problem here is the absence of isolation, this will be managed by measuring differentially, providing isolated power supplies where necessary and paying strict attention to the analog circuit PCB layout. The two solutions proposed here for the voltage sense function are similar. However the discrete resistors are preferred for the voltage sense function because they offer greater flexibility for scaling compared to the integrated differential amplifier solution.

3.2.5 Gate drive floating supply

As stated in section 3.2.2 a bootstrap supply is required to generate a gate drive voltage higher than the bridge supply voltage for the high side power transistor. In applications that require 100% duty cycle operation this simple bootstrap supply has to be replaced with a floating supply that can supply the high side gate drive circuitry with continuous voltage. The requirement exists that the power amplifier circuitry be capable of operating at 100% duty cycle and will thus require a floating supply for the integrated gate drive IC.

One method for generating a high side floating supply is to use a charge pump circuit that consists of approximately a dozen components [49]. A dual three-phase bridge will require six charge pump circuits that will result in an unnecessary high component count. The isolated transformer floating supply is a lower component count solution and thus more reliable than the bootstrap method. The transformer floating supply concept is shown in Figure 3-12.

Components $TX1$, $D3$, $C1$ and $R1$ constitute the floating supply. The high frequency oscillator voltage is transformed through $TX1$ and peak rectified by $D3$ and $C1$ to produce a voltage V_b . The function of resistor $R1$ is to provide a minimum load for the peak rectifier that may otherwise rise to an unacceptably high voltage level.

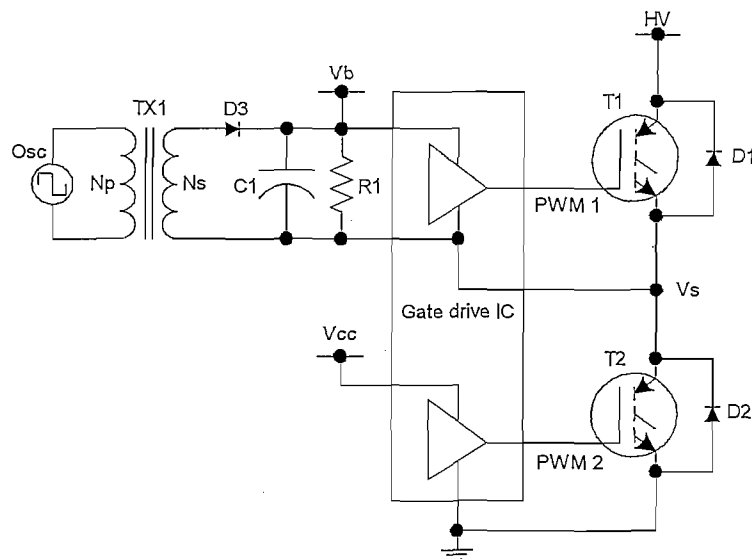


Figure 3-22 Gate drive floating supply

The circuit in Figure 3-12 can be extended to include multiple secondary windings for the remaining gate driver ICs of the three-phase bridge. The transformer isolated floating supply will be used for the gate drive floating supply function.

3.2.6 Protection circuitry

Protection circuitry is required to protect the power amplifier from the fault conditions of over temperature and over current including short circuit conditions. The fault condition, once detected, will either be reported to a digital controller or used to shutdown the power amplifier.

Factors to consider when selecting an appropriate temperature sensor are:

- Temperature measurement range
- Sensor accuracy
- Sensor power supply requirements
- Mechanical packaging and size
- Sensor output: analog, digital or set trip level

The over temperature fault condition can be measured with an appropriate temperature sensor IC, a semiconductor thermal switch or a bi-metal thermal switch. The thermal switch, bi-metal or

semiconductor, is a simple solution however these devices have a set trip temperature with associated hysteresis, thus they can't monitor temperature over a linear range.

A temperature sensor IC is capable of continuously measuring temperature and thus offers more flexibility in application. Temperature sensor ICs are available in a variety of output formats, measurement ranges, accuracies and mechanical packages. Temperature sensor ICs are available that generate measured temperature in digital format and thus are easily interfaced to a digital controller. A temperature sensor IC will provide the most versatile solution for the over temperature protection function.

The over current protection has two functions namely continuous over current protection and pulse-for-pulse current protection. The continuous over current protection can be derived from the AMB coil current measurement performed by the integrated current transducer. The AMB coil current measurement will be used in the high sample rate control algorithms and thus be available for continuous current limit implementation.

The pulse-for-pulse current limit occurs at the PWM switching frequency and thus requires extremely fast response time to be effective. For this reason pulse-for-pulse current limit should not be implemented in an interrupt driven software routine but rather in hardware. The integrated gate drive IC in Figure 3-5 has a shutdown pin for implementing the pulse-for-pulse current limit function with a maximum propagation delay of 140 ns. When driven high the shutdown pin is internally latched and turns off both the upper and lower IGBTs. The next PWM pulse after the shutdown pin goes low, clears the latch and activates the appropriate driver channel.

In order to implement the pulse-for-pulse current limit function the IGBT current has to be sensed. This is most conveniently achieved by placing a non-inductive power metal film resistor between the emitter of the bottom IGBT and the ground reference. The sensed voltage is filtered, compared to a reference and used to drive the shutdown pin of the integrated gate drive IC.

3.2.7 Filter

Filters are required to attenuate high frequency noise that exists as a result of stray inductance in the high current path of the half bridge legs of the power circuit. The stray inductances L_{e1} and L_{c2} between the emitter of $T1$ and the collector of $T2$ in Figure 3-13 can only be minimized by proper circuit layout. The stray inductances L_{c1} and L_{e2} in Figure 3-13 exist as a result of the connection between the IGBTs and the power supply [49]. These stray inductances can be

minimized with a high quality decoupling capacitor placed directly across the half bridge leg as shown in Figure 3-13.

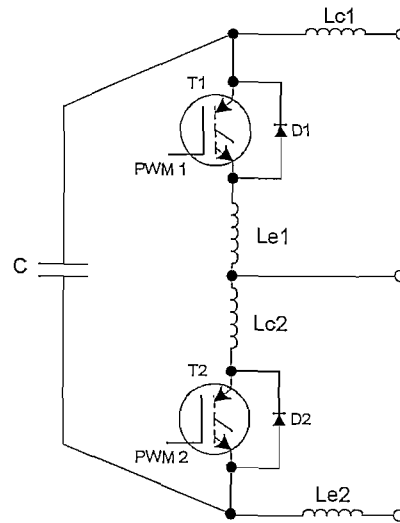


Figure 3-23 Half bridge stray inductances

In order to be effective the decoupling capacitor C in Figure 3-13, should be placed as close as possible to the half bridge switches. Since only SMD components can be mounted on the power amplifier substrate, the decoupling capacitor will have to be a SMD component. The capacitor should also be a high quality low equivalent series resistance (ESR) device.

Multi-layer polymer (MLP) capacitors and multi-layer ceramic (MLC) capacitors are both suitable high quality low ESR type decoupling capacitors. However MLP capacitors offer several advantages over MLC capacitors. MLP capacitors have substantially lower ESR and dissipation factor than MLC capacitors and can thus handle larger ripple current. A significant advantage of MLP capacitors is their ability to handle thermal shock due to the good thermal coefficient of expansion. MLC capacitors, especially SMD types, are notorious for cracking when exposed to mechanical or thermal stress.

The half bridge decoupling capacitor should be a MLP capacitor in a SMD package.

3.3 Digital controller

The digital controller must provide, by means of suitable embedded devices, the signal processing capability to implement the self-sensing and control algorithms for suspending a one DOF AMB. Additionally the digital controller shall make provision for communication interfaces, external memory and I/O expansion, including LEDs and tactile switches. Each embedded device will have a dedicated JTAG interface for debugging and programming purposes. The embedded devices will also generate the PWM control signals required to steer the dual three-

phase bridges. The electronic supply will generate all the low voltage supplies required by the digital controller circuitry. The conceptual design of the electronic supply is covered in section 3.4. A functional block diagram of the digital controller is shown in Figure 3-14.

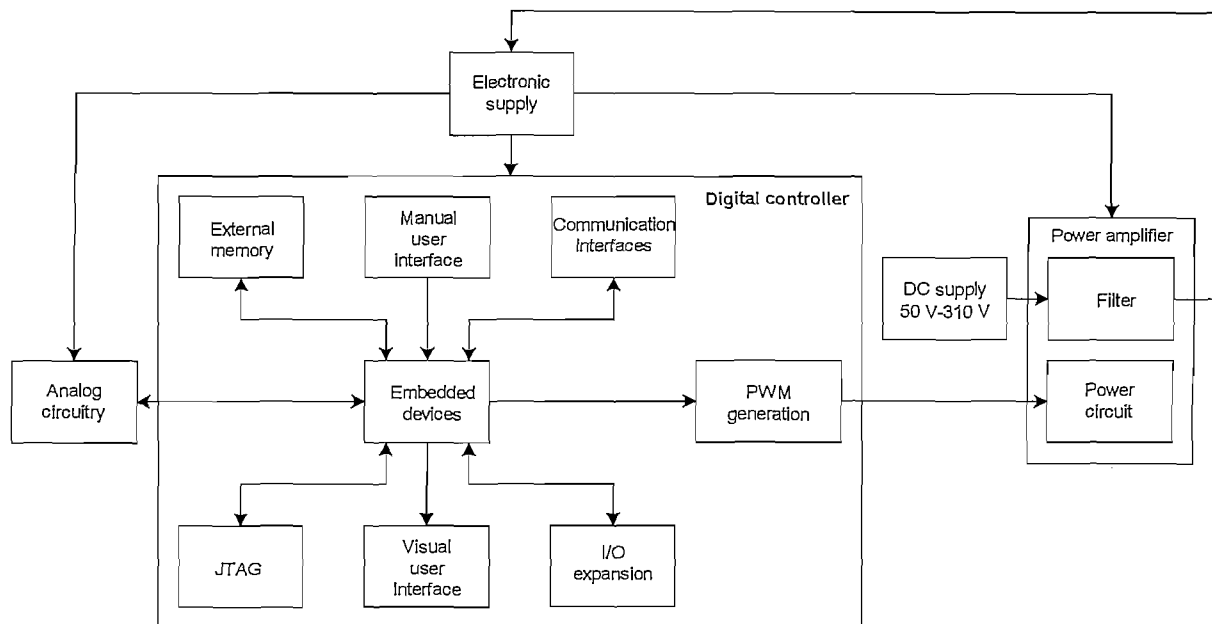


Figure 3-24 Digital controller block diagram

The digital controller will consist of the following functional units:

- Embedded devices
- External memory
- Manual user interface
- Communication interface
- PWM generation
- I/O expansion
- Visual user interface
- JTAG

In the following sections a conceptual design will be proposed for each of the digital controller functional units. This information will assist in developing the integrated drive specification and subsequently performing the detail design.

3.3.1 Embedded devices

The first step in the process of selecting suitable embedded devices is to identify the appropriate digital controller architecture to match the computational complexity of the intended control algorithm [6], [19]. A digital controller architecture that combines a DSP and an FPGA to

form a co-processor increases the scope of the design solution and is a good model for enabling flexibility, programmability and computational acceleration of the system [4], [20], [21]. The implementation of a co-processor architecture to form an integrated controller for solving computationally intensive algorithms in power electronic applications has been demonstrated in [22], [23], [25]. The increased speed and flexibility achievable with a FPGA based digital controller in an AMB application [18] can also be exploited in a co-processor based architecture. A digital controller that combines a DSP and an FPGA to form a co-processor is thus considered an appropriate architecture for self-sensing AMBs.

Suitable embedded devices have to be selected for the co-processor implementation. The selection of a suitable DSP processor will be influenced by, but not limited to factors such as:

- Speed
- Cost
- Packaging
- Power supply
- Number of I/Os
- On-chip peripherals such as communication interfaces, ADC and PWM
- Amount and type of on-chip memory, including memory addressing range
- Development tools including vendor and third party software libraries

One of the most important factors in selecting a processor is the development tools [29]. Since most manufacturers offer products with similar features and capabilities, familiarity with the development tools and the product often drive the decision making process. Familiarity with a particular processor and its development tools imply that a considerable investment in capital and time has already been made and a decision to reinvest in a new product should only be considered in extreme cases such as obsolescence.

The McTronX research group have experience with the Texas Instruments TMS320F2812 DSP since they have used this DSP in previous AMB research projects and have thus already invested in the development tools. Texas Instruments offer comprehensive software libraries for this DSP. The key features of this device are listed below [50]:

- High performance 32 bit integer CPU:
 - 150 MIPS operation
 - 1.8 V core and 3.3 V I/O power supply
 - 32 x 32 MAC
- On chip memory:

- 128 K x 16-bit Flash
 - 18 K x 16-bit single access RAM
 - 4 K x 16-bit boot read only memory (ROM)
- On chip peripherals:
 - 16 Channel, 12-bit, 12.5 million samples per second ADC
 - 16 PWM channels
 - Serial peripheral interface (SPI)
 - Dual universal asynchronous receiver transmitter (UART)
 - Multi-channel buffered serial port (McBSP)
 - Controller area network (CAN)
 - Watchdog timer
 - Programmable phase lock loop
- 56 general purpose I/O pins
- 1M external memory address range

The TMS320F2812 DSP is rich in on-chip peripherals, specifically customized for embedded control applications such as AMBs, the device is also familiar to the McTronX research group and thus considered a feasible embedded device for the DSP function in the co-processor architecture.

The selection of a suitable FPGA for the co-processing function will be influenced by, but not limited to factors such as:

- Speed
- Cost
- Packaging
- Power supply
- Static RAM or Flash based technology
- Number of I/Os and standards supported
- Number of gates or CLBs
- On-chip peripherals such as hardware multipliers and digital clock managers (DCM)
- Amount and type of on-chip memory
- Development tools, vendor and third party firmware libraries including core generation tools.

A comparison of low cost high performance FPGAs from the following leading manufacturers, Actel, Altera, Lattice and Xilinx, shows that the Spartan-3E FPGA from Xilinx is optimised for logic integration, DSP co-processing and embedded control [51]. The Spartan-3E family of

FPGAs offer logic densities ranging between 100 K gates and 1600 K gates in a variety of packaging options that allow easy migration between devices with the same package. The 500 K logic gate XC3S500E device in a 256-ball fine pitch ball grid array package allows migration up to a 1200 K device or down to a 250 K device, in the same package. The key features of the Spartan-3E XC3S500E device are listed below [52]:

- Device density:
 - 500 K system gates
 - 10476 equivalent logic cells
 - 1164 CLBs
- On-chip memory:
 - 73 K bits of distributed RAM (One K bit is equivalent to 1024 bits)
 - 360 K bits of block RAM
- On-chip resources:
 - 20 dedicated 18 x 18 multipliers
 - JTAG programming/debugging port
 - Differential input termination (120 Ω)
- Clocks:
 - 4 DCMs
 - Frequency range: 5 MHz to 300 MHz
 - Frequency synthesis: multiplication, division, phase shifting
 - Delay locked loop
- Single ended I/Os:
 - 190 user I/Os
 - Low voltage transistor-transistor logic (LVTTL) at 3.3 V
 - Low voltage CMOS (LVCMOS) at 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V.
- Differential I/O pairs:
 - 77 differential I/O pairs
 - Low voltage differential signalling (LVDS)
- Power supply:
 - Built-in power on reset circuitry
 - 1.2 V core and 2.5 V auxiliary power supply
 - 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V and 3.3 V I/O power supply

The resource utilization of the XC3S500E FPGA can be tested using the Xilinx CORE Generator™ tool. The CORE Generator is a design tool that generates parameterized IP optimized for Xilinx FPGAs. It provides a catalog of ready-made functions ranging in complexity from memories to high level system functions such as FIR filters and FFTs.

As a first order evaluation of the XC3S500Es resource utilization, a low pass FIR filter used in the self-sensing algorithm will be simulated in MATLAB® and implemented using the CORE Generator tool. The FIR filter specifications are given below:

- Response type: low pass
- Order: 400
- Design method: least squares
- Structure: direct form
- Sample frequency: 800 kHz
- Pass band edge frequency: 0.6 kHz
- Stop band edge frequency: 3.5 kHz

The filter design and analysis tool in MATLAB® is used to simulate the FIR filter and generate a set of filter coefficients that are used by the Xilinx CORE Generator tool to implement the low pass FIR filter. The magnitude response of the FIR filter simulated in MATLAB® is shown in Figure 3-15.

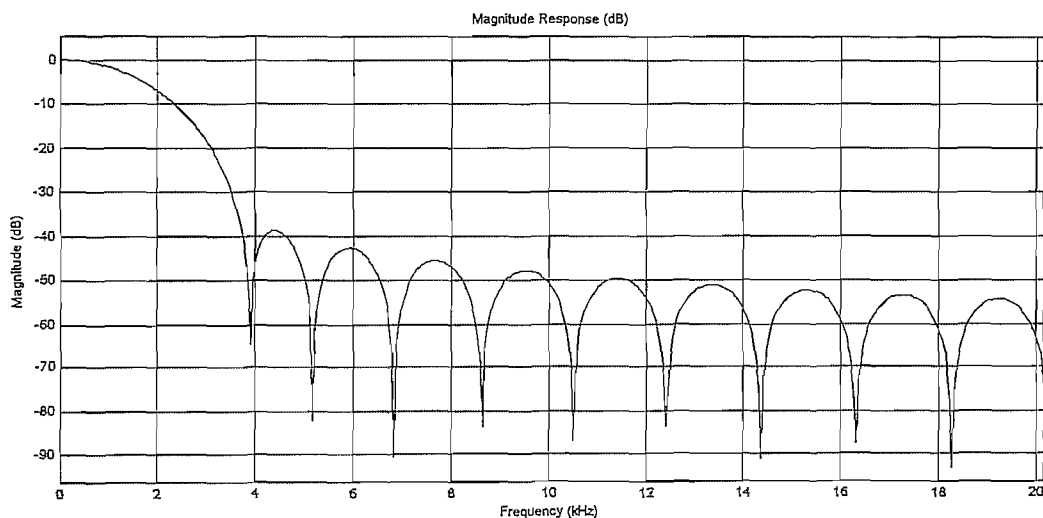


Figure 3-25 FIR filter magnitude response

The filter coefficient file generated in MATLAB® is imported into the Xilinx CORE Generator tool and used together with the filter specifications to generate a FIR filter core for the XC3S500E FPGA. The CORE Generator tool generates the resource utilization report shown in Figure 3-16. The resource report is only an estimate of the actual resource utilization and may vary when the core is implemented in a design. Multiple instantiations of the same filter will also have an affect on the resource utilization since resources can be shared instead of being duplicated. The method used to implement a particular function will also have an affect on the resource

utilization, for instance if no dedicated multipliers are available in a design a look-up-table based multiplier will be implemented.

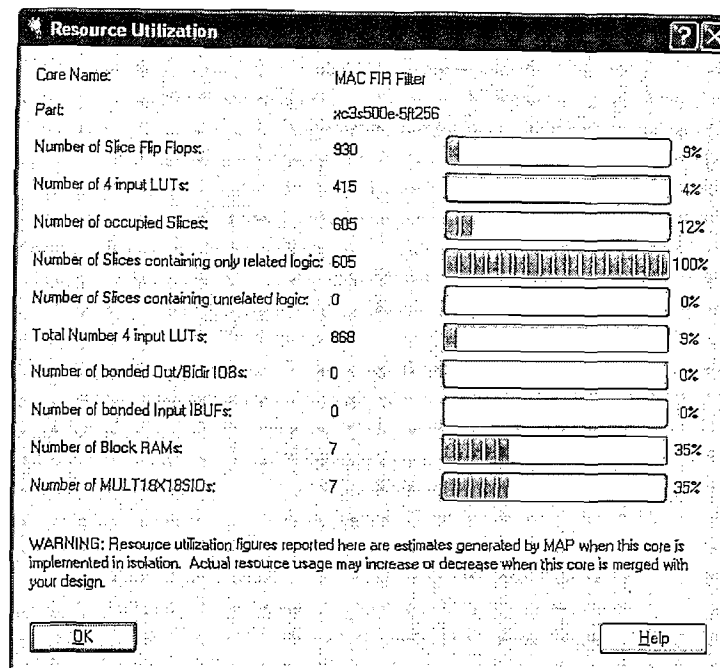


Figure 3-26 FIR filter resource utilization

The resource utilization report shows very low usage of the XC3S500E logic elements however a third of the block RAM and multipliers have been used due to the high order of the FIR filter. Although the block RAM and multiplier usage is high the XC3S500E appears to have sufficient resources as a co-processor. Additionally the XC3S500E device, in a 256-ball fine pitch ball grid array package, allows migration up to a 1200K device in the same package offering substantially more resources without any hardware changes to the design. The development tools for the XC3S500E FPGA, including the CORE Generator tool, are available free of charge from Xilinx, not necessarily the case for the other leading manufacturers. In light of these considerations, the XC3S500E FPGA is deemed a feasible embedded device for the FPGA function in the co-processor architecture.

The partitioning of the design into hardware (FPGA) and software (DSP) will affect the time taken to transfer data and the amount of data transferred between the processors and should be minimized [25]. There are various interfacing options for transferring data between the DSP and FPGA in asynchronous serial, synchronous serial or parallel mode. These options are listed below:

- DSP SPI peripheral to SPI instantiation on the FPGA (CORE Generator tool component)
- DSP McBSP peripheral to synchronous serial port instantiation on the FPGA
- DSP UART peripheral to UART instantiation on the FPGA

- DSP external memory interface to dual port RAM instantiation on the FPGA (CORE Generator tool component)

The option of interfacing the DSP external memory interface to a dual port RAM instantiation on the FPGA allows both processors to access the same data area at independent rates. This interface will benefit the partitioning of the design if the processes executing on the FPGA and DSP are running at different clock rates, which in all likelihood will be the case. This concept is shown in Figure 3-17.

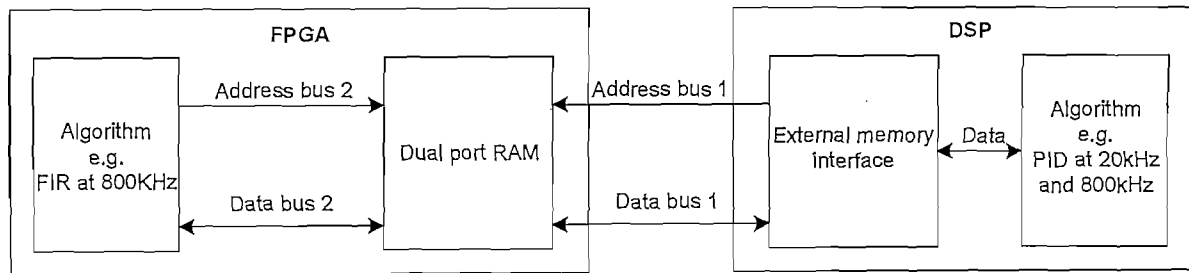


Figure 3-27 Dual port RAM co-processor interface

In summary the concept for the embedded devices is a co-processor architecture consisting of a TMS320F2812 DSP and a XC3S500E FPGA with a dual port RAM instantiation on the FPGA facilitating data transfer between the processors.

3.3.2 External memory

Since the DSP on-chip data memory, 18 K x 16-bit single access RAM, can be accessed faster than external memory it must be reserved for embedded software usage. An external data memory is thus required for data storage during debugging and data logging sessions. The external memory should be a static RAM capable of high speed access time, in the order of 10 ns to 20 ns. The external RAM should preferably be a 3.3 V CMOS device since this will allow direct interfacing to the DSP external memory interface. The external memory should be organized as N x 16-bit words where N is limited to the 1 M external memory addressing range of the DSP. The external memory chip select decoding can be implemented in the FPGA co-processor. External memory features such as three state outputs and data control for upper and lower bytes of the 16-bit words may be useful but not mandatory.

3.3.3 Manual user interface

A manual user interface is required between the integrated drive and the user. Tactile switches will provide a manual mode of switching to the user. The tactile switches should be interfaced to the embedded devices via Schmitt trigger input buffers.

3.3.4 Communication interface

The system architecture in Figure 3-1 shows that the integrated drives require the capability to communicate with a main controller via a control network. The data link protocol will be a master slave type protocol with the main controller as the master and the integrated drives as the slaves. A bit rate of 20 mega bits per second (Mbps) is necessary to support the control loop sample rate required for five integrated controllers. The DSP on-chip CAN module supports a maximum data rate of 1 Mbps and thus will not be suitable as a network controller [50]. The attached resource computer network (ARCNET) protocol is well suited for control applications because of its robustness and deterministic performance, however it only supports a maximum data rate of 10 Mbps. To satisfy the bit rate requirement of 20 Mbps, a propriety data link protocol for the integrated drive control network can be instantiated as a firmware component in the FPGA co-processor. A suitable TIA/EIA-485 transceiver capable of data transmission up to 20 Mbps can be used for the balanced differential data transmission in the half-duplex multi point network. The TIA/EIA-485 network must make provision for appropriate bus termination, fail safe biasing and transient protection.

The DSP has two on-chip UART peripherals that should be made available as communication interfaces via an appropriate TIA/EIA-232 transceiver. This asynchronous serial interface will be used for low speed single ended point-to-point communication between the integrated drive and a personal computer.

3.3.5 PWM generation

The embedded devices have to generate the PWM control signals required to steer the dual three-phase bridges. Three independent complimentary sets of PWM signals are required to drive each three-phase bridge, thus a total of twelve PWM signals are necessary for dual three-phase bridges. Programmable dead-band is required between complimentary PWM outputs to avoid short circuit conditions between upper and lower IGBTs in each leg of a three-phase bridge [36]. The PWM carrier frequency should be programmable and in the range of 20 KHz to 50 KHz with the duty cycle adjustable from 0 % to 100 %. The resolution of the PWM signal should be at least 10-bits. Synchronizing the PWM signals between the integrated drives will reduce the switching noise in the AMB system and can be achieved by using the same time base to generate all the PWM signals in the system.

The DSP on-chip PWM peripheral has the following characteristics [50]:

- Up to 16-bit resolution
- A total of 16 PWM outputs

- Programmable dead-band for PWM output pairs
- Compare and period registers are automatically updated thus minimizing CPU overhead
- Double buffered registers allowing on-the-fly updates of PWM carrier frequency and pulse widths
- Programmable asymmetric, symmetric and space vector PWM waveforms
- Internal or external clock source for PWM counter time base thus allowing external synchronization of PWM signals

The DSP on-chip PWM peripheral will be able to accommodate all of the requirements for PWM generation for the dual three-phase bridges. The on-chip functionality will limit CPU overhead and thus free the DSP to perform more important functions.

3.3.6 I/O expansion

Access to spare digital I/O pins on both the DSP and the FPGA is required. In the case of the DSP spare ADC channels will also be made available. Access to the spare digital I/Os will be made available in a separate area on the PCB to the spare analog I/Os in order to avoid possible interference between these signals [44].

3.3.7 Visual user interface

A visual user interface is required between the integrated drive and the user. LEDs will provide a visual indication to the user. The LEDs should be interfaced to the embedded devices via suitable buffers.

3.3.8 JTAG interface

The DSP and the FPGA each require a dedicated IEEE 1149.1 JTAG interface for device programming and debugging purposes. In addition the FPGA requires a configuration device that also has an IEEE 1149.1 JTAG port. The FPGA and the configuration device are connected in a JTAG scan chain where both devices share the test clock (TCK) and test mode select (TMS) inputs. The devices may be connected in either order in the scan chain with the test data output (TDO) of the first device feeding the test data input (TDI) of the second device in the scan chain. The TDO of the second device drives the JTAG connector [52]. The DSP JTAG interface is simpler to implement since the DSP is the only device in the scan chain. The DSP JTAG interface uses an additional signal, the test reset (TRST) signal. A diagram showing the JTAG interfaces for both embedded devices and the configuration device is shown in Figure 3-18.

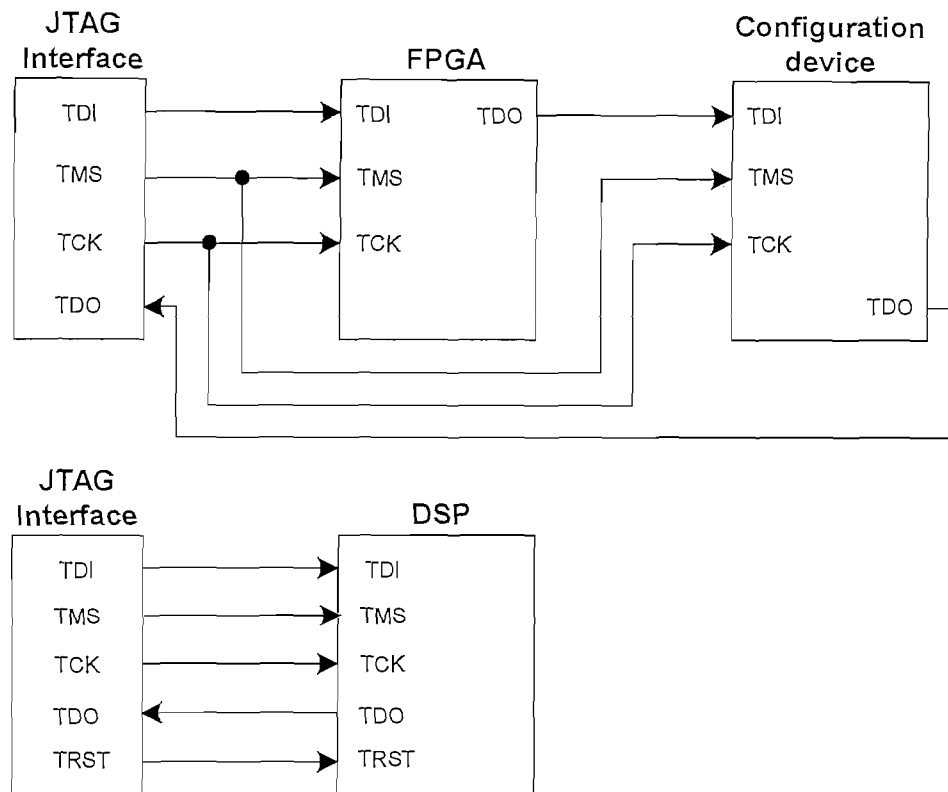


Figure 3-28 Embedded devices JTAG interface

3.4 Electronic supply

The electronic supply must generate the regulated voltages necessary for the integrated drive electronics i.e. the digital controller circuitry, the analog circuitry and the power amplifier small signal electronics. The electronic supply must derive and isolate these voltages from the system input supply which can be 50 V to 150 V DC. The following voltages are required:

- Power amplifier small signal electronics:
 - +12 V, +5 V
- Analog circuitry:
 - ± 12 V
- Digital controller:
 - +12 V, +5 V, +3.3 V, +2.5 V, +1.8 V, +1.2 V

The +12 V and +5 V used by the power amplifier small signal electronics may not be referenced to the same ground as the +12 V and +5 V used by the digital controller, thus the electronic supply has to generate multiple output voltages. A functional block diagram of the electronic supply is shown in Figure 3-19.

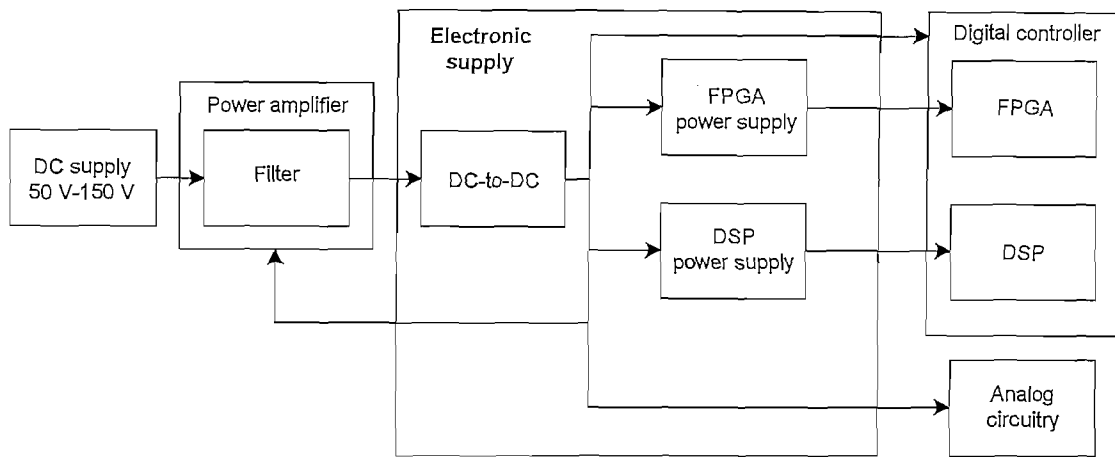


Figure 3-29 Electronic supply block diagram

The electronic supply will consist of the following functional units:

- DC-to-DC converter
- FPGA power supply
- DSP power supply

In the following sections a conceptual design will be proposed for each of the electronic supply functional units. This information will assist in developing the integrated drive specification and subsequently performing the detail design.

3.4.1 DC-to-DC converter

There are three fundamental fixed frequency PWM switching power supply topologies namely the buck, boost or buck-boost topology. The buck topology is used to generate an output voltage that is lower than the input voltage, the boost topology is used to generate an output voltage that is higher than the input voltage and the buck-boost topology can generate an output that is either lower or higher than the input voltage [36]. Since they are capable of stepping the input voltage down, the buck or buck-boost topology are most suitable for implementing the DC-to-DC converter.

The transformer coupled versions of the buck or buck-boost converter will provide the necessary isolation between the input and output while permitting turns ratio adjustment to optimize the duty cycle and minimize the primary peak current. Multiple outputs at different voltages can be generated by multiple secondary windings on the transformer. The transformer coupled version of the buck-boost converter is called a flyback converter. The flyback topology is particularly well suited to multiple secondary output windings because it doesn't have a filter inductor in series with the output to degrade the dynamic cross regulation between the multiple windings [53]. The dynamic performance is also improved when the flyback converter is

operated in the discontinuous current mode since the small signal closed loop characteristic only contains a capacitor with the associated 90 degree phase lag. This single pole characteristic is inherently stable which simplifies the design of the closed loop compensator. There are three fixed frequency PWM control methods namely direct duty cycle control, voltage feed forward control and current mode control that can be used to control the discontinuous mode flyback converter. Current mode PWM control is recommended since it adds an inner control loop that improves the converter line regulation [53]. The basic multiple output transformer coupled flyback converter is shown in Figure 3-20.

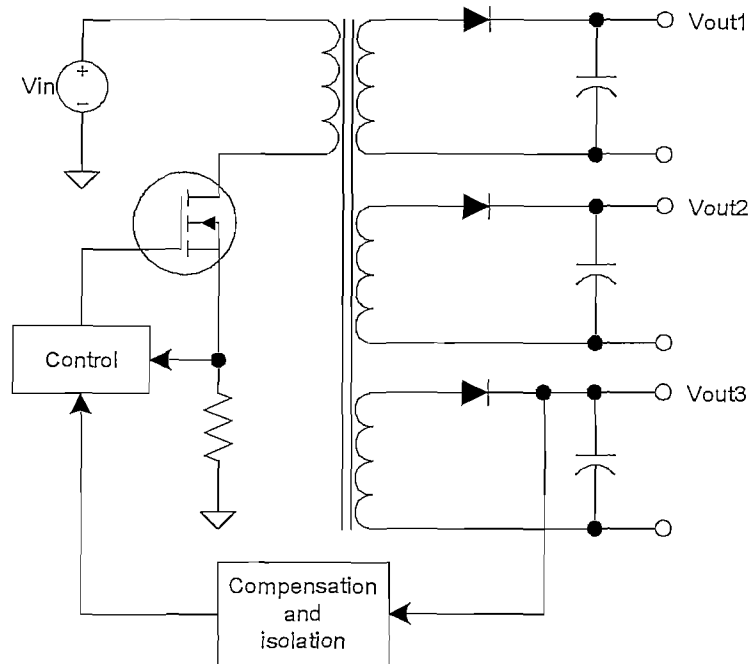


Figure 3-30 Multiple output flyback converter

The transformer coupled discontinuous mode flyback topology is recommended for applications at low power levels, under 200 W, that require isolation and multiple outputs [53]. Due to its simplicity, especially when operated in the discontinuous current mode with current mode PWM control, the flyback topology is considered the most appropriate for the DC-to-DC converter.

3.4.2 FPGA power supply

The XC3S500E FPGA requires multiple supply voltages. The internal core supply voltage V_{CCINT} is 1.2 V and supplies all the internal logic functions such as CLBs, block RAM and the multipliers. The auxiliary supply voltage V_{CCAUX} is 2.5 V and supplies the DCMs, differential drivers, certain dedicated configuration pins and the JTAG interface. Each of the four I/O banks has its own V_{CCO} supply that is selectable between 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V and 3.3 V depending on the application requirements however all V_{CCO} pins in a specific I/O bank must be connected to the same supply voltage. The current consumption for each supply voltage

depends on the application thus for design flexibility provision must be made for maximum device current.

At power-up a built-in power on reset (POR) circuit monitors the V_{CCINT} , V_{CCAUX} and the V_{CC0} bank 2 supply voltages. The POR circuit holds the FPGA in reset until these voltages reach the respective thresholds required for successful FPGA configuration. Once these voltages reach the correct levels the POR circuit releases the FPGA from reset and configuration proceeds. Since the POR circuit monitors all the supply voltages there is no specific voltage sequencing requirement, however applying the V_{CCAUX} supply before the V_{CCINT} supply will minimize the current required by the FPGA at power-up [52].

Various component manufacturers offer custom power solutions for FPGAs. These custom ICs operate from a single input supply voltage such as +5 V and include all the functions required to power the FPGA according to the manufacturer specifications. The TPS75003 power management IC from Texas Instruments meets all the requirements for powering the XC3S500E FPGA including features such as soft start, adjustable output voltage and independent enables allowing flexible voltage sequencing to minimize start-up current.

The TPS75003 power management IC will ensure reliable power supply with minimum complexity and is thus recommended for powering the FPGA.

3.4.3 DSP power supply

The TMS320F2812 DSP core supply voltage V_{DD} is 1.8 V. The V_{DDIO} I/O supply, the V_{DDA} analog supply, and the V_{DD3VFL} flash programming supply voltages are all 3.3 V. The power-up sequence requires that all the 3.3 V supplies be enabled prior to ramping up the 1.8 V core supply. During power down the device reset should be asserted low before the V_{DD} supply goes below 1.5 V in order to keep the on-chip flash logic in reset. Texas Instruments recommends that a custom low dropout regulator be used to power the DSP in order to meet these POR requirements. The TPS767D301 low dropout regulator complies with all the requirements for powering the TMS320F2812 DSP and will thus be used for this purpose.

3.5 PCB layout

The power amplifier, digital controller and analog circuitry will be partitioned in an attempt to minimize the interference between these circuits [44]. Separate PCBs and insulated metal substrate will be used to accommodate the partitioning of these subsystems by stacking them on top of each other using appropriate headers and sockets. Brass pillars of appropriate length will be used to provide the necessary mechanical rigidity between the various PCB assemblies.

The proposed PCB stacking arrangement is shown in Figure 3-21. A grounding philosophy based on a dedicated layer of solid ground plane will be implemented for the digital controller PCB and analog PCB design since it offers the following benefits:

- Minimized crosstalk.
- Maximize the capacitive decoupling between the power plane and the solid ground plane, thus providing an effective high frequency decoupling mechanism.
- Maximize the flexibility in terms of where components may be placed.

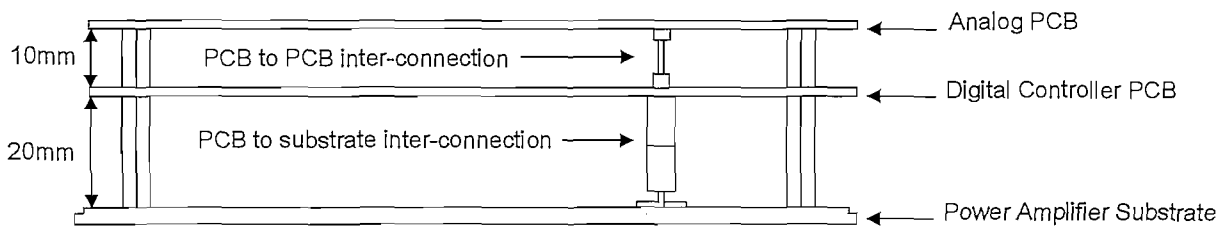


Figure 3-31 PCB stacking

A solid ground plane will be implemented on the analog interface PCB and on the digital controller PCB. The most critical connection between these PCBs is the ± 12 V analog supply return. A common ± 12 V analog supply return will be established between the two PCB ground plains by means of a single inter PCB connection, thus minimizing the possibility of creating unwanted ground loops. The inter PCB connection will be placed as close as possible to the ADC converter on the digital controller PCB.

The size of the BGA package will play a major role in determining the number of layers required to route the PCB effectively [47]. The FPGA is a XC3S500E device in a 256-ball fine pitch ball grid array package. Applying the BGA design rule shown in Figure 2-15 to the 256-ball fine pitch ball grid array package, a minimum of four PCB layers are required to route the FPGA. Since additional layers are required for routing the solid ground plane, power supply and power amplifier signals, the initial target for the digital PCB layout will be eight PCB layers. Layers may be added as the PCB design progresses since the design should not be forced into the fewest number of layers possible at the expense of design integrity or reliability.

3.6 Mechanical layout

As stated in section 3.5, separate PCBs and insulated metal substrate will be used to accommodate the partitioning of these subsystems by stacking them on top of each other using appropriate headers and sockets. The size of the PCBs and insulated metal substrate is specified as 159 mm x 235 mm for mounting in a standard 6U subrack. A front view of the proposed mechanical layout of the integrated drive is shown in Figure 3-22.

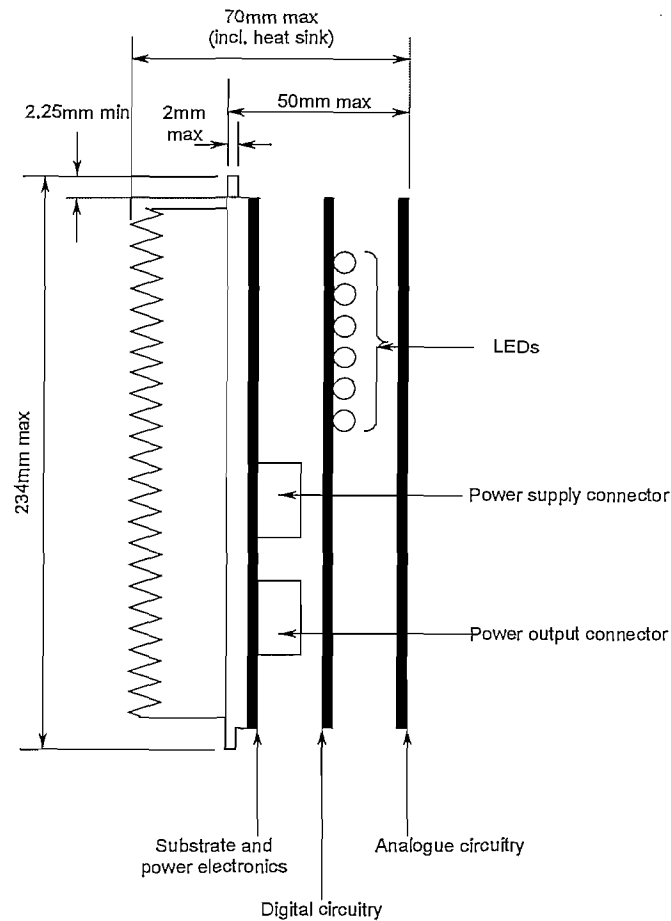


Figure 3-32 Integrated drive mechanical layout

The subrack is 425 mm wide and will thus be able to house six of the integrated drive assemblies, including a 20 mm heat sink for each assembly as shown in Figure 3-22. The total height of each integrated drive electronic assembly, excluding the 20 mm heat sink, will thus be limited to 50 mm.

3.7 Conclusion

In Chapter 3 a conceptual design was proposed for the power amplifier, digital controller and electronic supply. The mechanical layout of the integrated drive was also addressed. The results of the conceptual design can now be used to perform a detail design of the integrated co-processor based power electronic drive. The results of the conceptual design will also assist the McTronX Research Group to compile a subsystem development specification for the integrated drive. Chapter 4 covers the detail design of the integrated co-processor based power electronic drive.

Chapter 4

Detail design

Chapter 4 covers the detail design of the integrated co-processor based power electronic drive. The detail implementation issues such as component selection, power supply requirements, thermal design and interfacing of the various circuit elements will be addressed.

4.1 Digital controller

The digital controller consists of the following functional units:

- Embedded devices
- External memory
- Manual user interface
- Communication interface
- PWM generation
- I/O expansion
- Visual user interface
- JTAG

In the following sections the detail design of the digital controller functional units will be done. The detail design will be grouped into three sections namely DSP, FPGA and communication.

4.1.1 DSP

The TMS320F2812 DSP in a 176 pin low profile quad flat pack package has been identified as the embedded device for the DSP function in the co-processor architecture.

Power supply

The TMS320F2812 DSP core supply voltage V_{DD} is 1.8 V. The V_{DDIO} I/O supply, the V_{DDA} analog supply, and the V_{DD3VFL} flash programming supply voltages are all 3.3 V. The TPS767D301 low dropout voltage regulator will be used to regulate the 1.8 V and the 3.3 V required by the DSP and generate the active-low external reset signal for the DSP. Ceramic SMD capacitors in X7R dielectric with a 0805 footprint are used for power supply decoupling of each DSP power pin. The decoupling capacitors are placed as close as possible to the appropriate DSP pins. The DSP on-chip ADC reference pins, ADCREFM and ADCREFP are also decoupled strictly in accordance with the manufacturer's guidelines. These pins are each decoupled with five parallel 2.2 μ F ceramic SMD capacitors in X7R dielectric. The typical current consumption versus frequency for the DSP with all the peripheral clocks enabled is shown in Figure 4-1. From Figure 4-1 it can be seen that the DSP will require approximately 280 mA of current when operating at 150 MIPS.

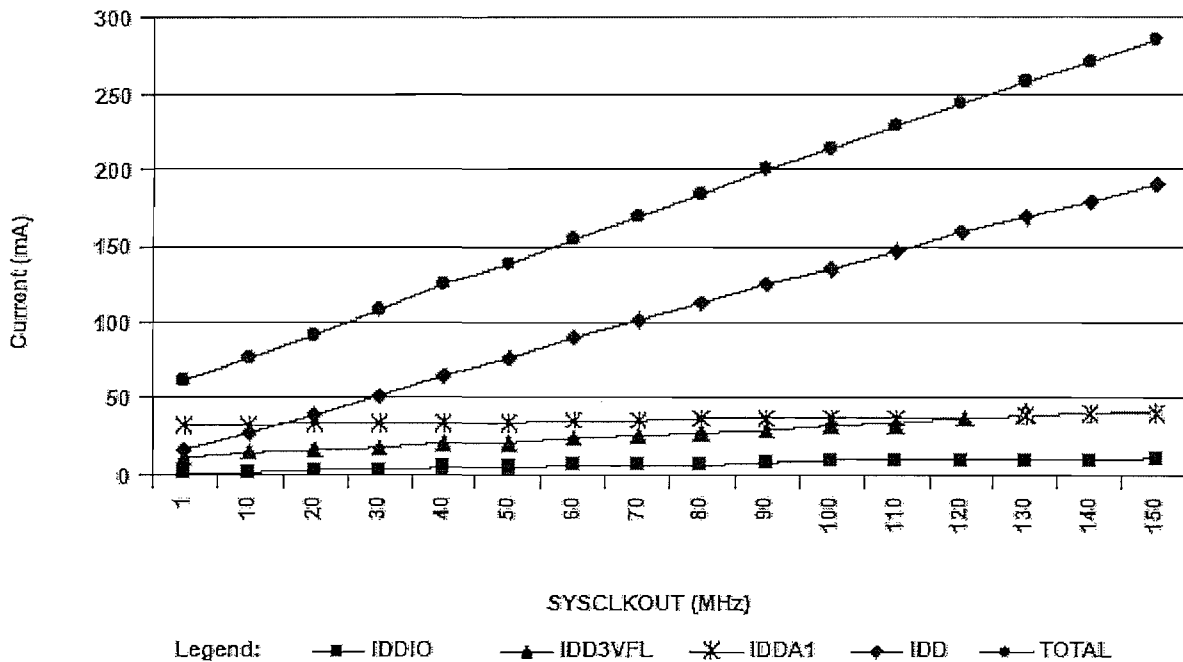


Figure 4-1 DSP current versus frequency [50]

Thermal considerations

The DSP total current consumption can be reduced from 280 mA to 255 mA since the multi-channel buffered serial port and the controller area network peripherals are not used. These peripherals use 13 mA and 12 mA of I_{DD} current respectively. The total power dissipation for the DSP can now be calculated

$$\begin{aligned}
 P_{D(tot)} &= (V_{DDIO} \cdot I_{DDIO}) + (V_{DD3VFL} \cdot I_{DD3VFL}) + (V_{DDA1} \cdot I_{DDA1}) + (V_{DD} \cdot I_{DD}) \\
 &= (3.3 \cdot 0.01) + (3.3 \cdot 0.04) + (3.3 \cdot 0.04) + (1.8 \cdot 0.165) \text{ W} \\
 &= 0.594 \text{ W}
 \end{aligned} \tag{4-1}$$

Provided that the ambient temperature remains at 25 °C, the junction temperature of the DSP will rise to

$$\begin{aligned} T_J &= T_A + P_{D(tot)} \cdot R_{\Theta JA} \\ &= 25 + (0.594 \cdot 41.88) \text{ } ^\circ\text{C} \\ &= 49.88 \text{ } ^\circ\text{C} \end{aligned} \quad (4-2)$$

The case temperature of the DSP will rise to

$$\begin{aligned} T_C &= T_J - P_{D(tot)} \cdot R_{\Theta JC} \\ &= 49.88 - (0.594 \cdot 9.73) \text{ } ^\circ\text{C} \\ &= 44.1 \text{ } ^\circ\text{C} \end{aligned} \quad (4-3)$$

Although the calculated junction temperature rise is well within the maximum value specified for the DSP, actual temperature rise will have to be measured since these calculations are based on manufacturer's typical data for the DSP.

Clock oscillator

A 30 MHz external clock oscillator will be used as a clock source for the DSP. The clock oscillator output is 3.3 V and thus requires level shifting to 1.8 V since the XCLKIN input of the DSP is referenced to the 1.8 V core supply voltage V_{DD} . The voltage level shift is accomplished by using the SN74LVC1G14 single Schmitt-trigger inverter in a 5-pin SOT-23 package. This low voltage CMOS part is capable of operating with a supply voltage as low as 1.65 V and can thus be powered from 1.8 V while accepting input voltages as high as 5.5 V. For signal integrity purposes the external clock oscillator and Schmitt-trigger inverter should be placed as close as possible to the XCLKIN input of the DSP.

User interface

The DSP is interfaced to the visual user interface and the manual user interface by means of SN74LVC14A hex Schmitt-trigger inverters. The low voltage CMOS inverters are supplied with 3.3 V and are capable of delivering ± 24 mA of current while their inputs are 5 V tolerant. The V_{DDIO} I/O supply on the DSP is 3.3 V and thus directly compatible with the low voltage CMOS inverters.

External memory

The IS61LV6416-10T is a 3.3 V CMOS static RAM with 10 ns access time and three state outputs that can be directly interfaced to the DSP as an external memory device. The RAM is

packaged in a 44-pin TSOP package. The memory is organized as 65536 x 16-bit words. The FPGA co-processor is used to do the address decoding for the external RAM and generates the active-low chip-enable input for the RAM. The active-low write-enable input of the RAM is connected directly to the active-low external-write-enable output of the DSP. The active-low output-enable input of the RAM is connected directly to the active-low external-read-enable output of the DSP. The active-low upper-byte and lower-byte inputs of the RAM are tied directly to digital ground since individual access to upper and lower bytes of the 16-bit words is not necessary. The data and address bus of the RAM is connected directly to the appropriate pins on the data and address bus of the DSP. The RAM is supplied with 3.3 V and decoupled by a 100 nF ceramic SMD capacitor in X7R dielectric with a 0805 footprint. The RAM requires 190 mA of dynamic operating current and 10 mA of standby current.

JTAG

The DSP JTAG interface is made available via a 14-pin double row 2.54 mm pitch header. The pin numbering and signal allocation of the JTAG header matches the manufacture's emulator header pin numbering.

PWM

The DSP on-chip PWM peripheral is used to generate the PWM signals for the dual three-phase bridges. As shown in Figure 3-4, an opto-coupler is required to provide an isolation boundary between the DSP and the power amplifier gate drive circuitry. The DSP is not capable of driving the opto-coupler directly thus a SN74LVC14A hex Schmitt-trigger inverter is used as a buffer between the DSP on-chip PWM peripheral and the opto-coupler. The HCPL-0631 from Agilent Technologies is a dual high speed opto-coupler capable of signal transmission at 10 Mbps. Using the recommended operating conditions for the opto-coupler, the current limiting resistor for the light emitting diode can be calculated as follows:

$$\begin{aligned}
 R &= \frac{V_s - V_f}{I_f} \\
 &= \frac{5 - 1.5}{0.0075} \Omega \\
 &= 466.67 \Omega
 \end{aligned}
 \tag{4-4}$$

The closest standard value resistor is 470 Ω . The power dissipated in the resistor is

$$\begin{aligned}
 P_D &= I^2 \cdot R \\
 &= \left(\frac{5-1.5}{470} \right)^2 \cdot 470 \text{ W} \\
 &= 26.06 \text{ mW}
 \end{aligned}
 \tag{4-5}$$

A 470 Ω 1% 0805 resistor capable of dissipating 0.125 W is selected. The software enable signal from the DSP to the power amplifier gate drive circuitry is also interfaced through a SN74LVC14A hex Schmitt-trigger inverter and isolated via a HCPL-0631 opto-coupler.

Floating supply drive

The DSP T4PWM output is used to generate a 50% duty cycle drive signal at 100 KHz for the floating supply of the power amplifier gate drive circuitry. A SN74LVC14A hex Schmitt-trigger inverter is used as a buffer between the T4PWM output and the floating supply circuitry.

ADC

The DSP has sixteen on-chip ADC channels. Eight of the ADC channels are routed to the analog circuitry PCB via a inter PCB connection. The remaining eight ADC channels and the ADC reference pins, ADCREFM and ADCREFP are routed to a 20-pin double row 2 mm pitch header for external interfacing. Ten general purpose I/O pins from the DSP are also routed to a 20-pin double row 2 mm pitch header for external interfacing.

DSP to FPGA interface

The DSP address bus, data bus and control bus are routed directly to the FPGA for memory interface and decoding purposes. The FPGA I/Os are configured for 3.3 V low voltage CMOS and thus are directly compatible with the DSP I/Os. The additional signals that are routed directly between the DSP and FPGA are listed in Table 4-1.

Table 4-1 Additional FPGA and DSP signals

DSP		FPGA	Function
Pin Name	Pin No.	Pin No.	
XCLKOUT	119	P9	DSP clock to FPGA
TDIRA	116	N16	DSP timer A external direction control signal from FPGA
TCLKINA	117	P8	DSP timer A external clock input from FPGA
TDIRB	71	M16	DSP timer B external direction control signal from FPGA
TCLKINB	72	T9	DSP timer B external clock input from FPGA
XINT1	149	B14	DSP external interrupt from FPGA

XNMI	150	A14	DSP non-masked external interrupt from FPGA
SPISIMO	40	L15	DSP SPI peripheral slave in master out to FPGA
SPISOMI	41	L14	DSP SPI peripheral slave out master in from FPGA
SPICLK	34	K16	DSP SPI peripheral clock output to FPGA
SPISTE	35	K15	DSP SPI peripheral slave transmit enable output to FPGA

4.1.2 FPGA

The XC3S500E FPGA in a 256-ball BGA package has been identified as the embedded device for the FPGA function in the co-processor architecture.

Power supply

The TPS75003 power management IC from Texas Instruments supplies the FPGA 1.2 V core supply voltage V_{CCINT} , the 2.5 V auxiliary supply voltage V_{CCAUX} and the V_{CC0} supply voltage. To simplify the interfacing between the FPGA and the DSP, all four FPGA I/O banks are supplied with the same V_{CC0} supply voltage of 3.3 V. Since the FPGA has a built-in power on reset (POR) circuit there is no specific voltage sequencing requirement, however applying the V_{CCAUX} supply before the V_{CCINT} supply will minimize the current required by the FPGA at power-up.

Decoupling considerations

The FPGA requires decoupling capacitors to supply local energy storage during switching transients across a wide frequency range. Each power pin on the FPGA must be decoupled with a mid frequency decoupling capacitor and a high frequency decoupling capacitor. A low frequency decoupling capacitor is required for each power rail. Figure 4-2 shows how the impedance of these decoupling capacitors changes with frequency.

The low frequency decoupling capacitor is a 10 μ F solid chip tantalum capacitor from the T491 series by KEMET in a SMD B case size. From Figure 4-2 it can be seen that this capacitor provides decoupling in the frequency range below 500 KHz. The mid frequency decoupling capacitor provides decoupling in the frequency range from 500 KHz up to 100 MHz. The mid frequency decoupling capacitor is a 0805 size SMD 100 nF multilayer ceramic chip capacitor in X7R dielectric. The high frequency decoupling capacitor is a 0805 size SMD 1 nF multilayer ceramic chip capacitor in X7R dielectric. The high frequency decoupling capacitor provides decoupling in the frequency range upward of 100 MHz.

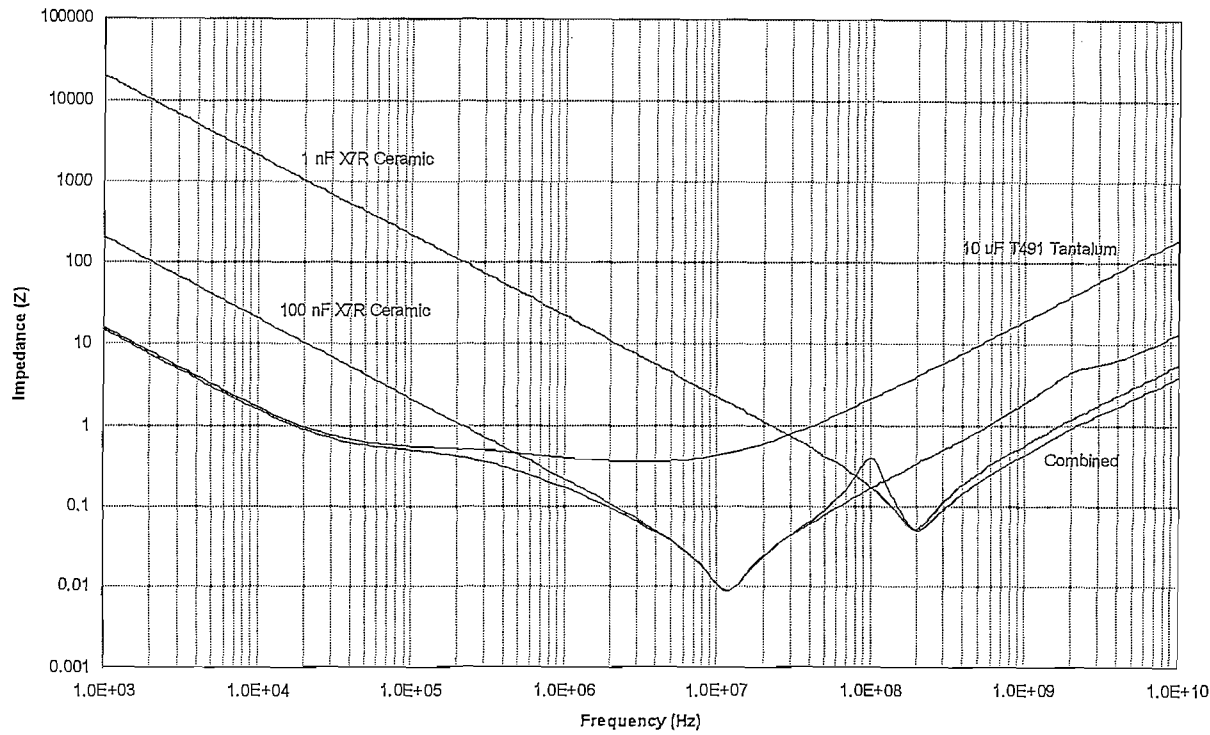


Figure 4-2 Decoupling capacitor impedance versus frequency

It is evident from the plot of the combined capacitor impedance in Figure 4-2 that the capacitors compliment each other thus providing the necessary decoupling across the frequency spectrum.

Thermal considerations

The current consumption, power dissipation and temperature rise of the FPGA is estimated using the XPower Estimator (XPE) tool from Xilinx. A map report file, generated from a hardware description language design similar to the self-sensing algorithm implementation, is loaded into XPE version 9.1.03 for the Spartan-3E series of FPGA. The XPE tool generates the results shown in Table 4-2 for the 256-ball BGA package with a 30 MHz clock operating at an ambient temperature of 25 °C without forced air cooling.

Table 4-2 FPGA power estimation

Parameter	Result
Power dissipation for V_{CCINT}	$1.2V \times 0.123A = 0.148\text{ W}$
Power dissipation for V_{CCAUX}	$2.5V \times 0.034A = 0.085\text{ W}$
Power dissipation for V_{CCO}	$3.3V \times 0.019A = 0.063\text{ W}$
Total device dissipation	0.295 W
Junction to Ambient thermal resistance	31.1 °C/W
Maximum allowable ambient temperature	75.8 °C

Using the data in Table 4-2, if the ambient temperature remains at 25 °C, the junction temperature of the FPGA will rise to

$$\begin{aligned} T_J &= T_A + P_D \cdot R_{\Theta JA} \\ &= 25 + (0.295 \cdot 31.1) \text{ } ^\circ\text{C} \\ &= 34.18 \text{ } ^\circ\text{C} \end{aligned} \quad (4-6)$$

The case temperature of the FPGA will rise to

$$\begin{aligned} T_C &= T_J - P_D \cdot R_{\Theta JC} \\ &= 34.18 - (0.295 \cdot 9.7) \text{ } ^\circ\text{C} \\ &= 31.32 \text{ } ^\circ\text{C} \end{aligned} \quad (4-7)$$

Although the calculated junction temperature rise is well within the maximum value specified for the FPGA, actual temperature rise will have to be measured since these calculations are not based on the actual self-sensing algorithm implementation.

Configuration

The FPGA static CMOS configuration latches have to be programmed every time power is applied to the FPGA. Several options are available to store the configuration data and accomplish the programming process. In master serial mode configuration, the FPGA configures itself from an external platform flash memory that stores the configuration data. Figure 4-2 shows a schematic representation of the master serial configuration mode using a Xilinx platform flash. The XCF04S is a 4 Mbit platform flash, the smallest device capable of storing the configuration data for the XC3S500E FPGA.

The FPGA supplies the configuration clock (CCLK) from its internal oscillator to the platform flash memory. The maximum CCLK speed is 25 MHz for a V_{CCO} supply of 3.3 V. For master serial mode configuration, the FPGA mode pins M0, M1 and M2 have to be connected to ground. The HSWAP pin is pulled high which places all user I/O pins in a high impedance state for the duration of the configuration process. The FPGA JTAG port is available to reprogram the FPGA at any time while the system is powered, regardless of the mode select pin settings. The JTAG interface is made available via a 14-pin double row 2 mm pitch header.

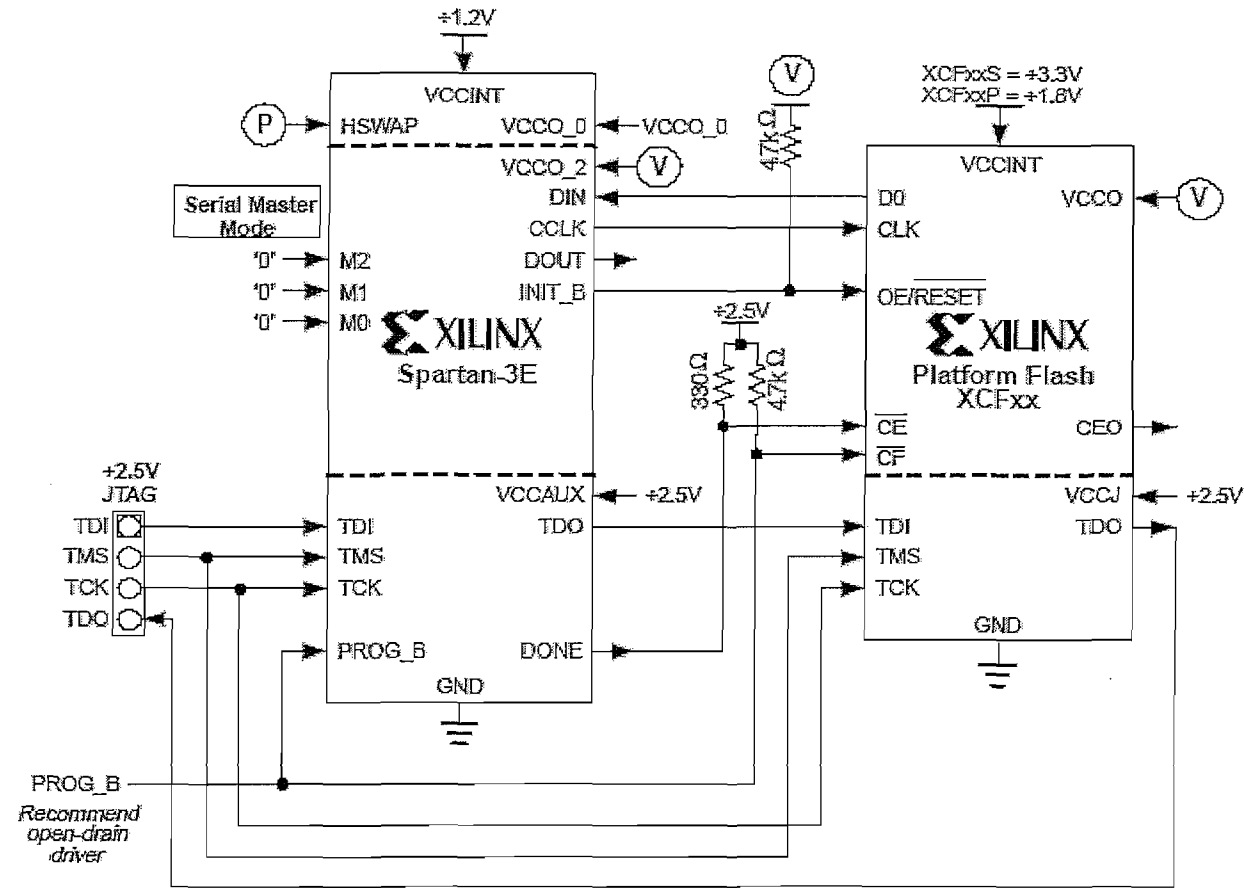


Figure 4-3 FPGA master serial configuration mode [52]

The pin numbering and signal allocation of the JTAG header matches the manufacture’s emulator header pin numbering.

4.1.3 Communication

A master slave type data link protocol will be implemented for high speed serial communication between the main controller and the integrated drives via a TIA/EIA-485 network. A TIA/EIA-232 asynchronous serial interface will be used for low speed single ended point-to-point communication between each integrated drive and a personal computer.

TIA/EIA-232 communication

Both DSP on-chip UART peripherals are interfaced via a MAX232A dual TIA/EIA-232 compatible transceiver. The MAX232A supports data rates up to 200 Kilo bits per second (Kbps). The MAX232A operating from a single +5 V supply, uses an on-chip charge pump and four external 100 nF capacitors to generate the ± 10 V levels required by the TIA/EIA-232 standard. The maximum current consumption for the MAX232A with both transceivers active is 15 mA.

The MAX232A transmitter inputs are TTL compatible. The TTL V_{IL} and V_{IH} levels are specified as 0.8 V and 2.4 V respectively while the DSP output buffer can swing between 0.4 V and 2.8 V, allowing a direct connection between the DSP output and the MAX232A transmitter inputs.

The MAX232A receiver outputs can't be connected directly to the DSP inputs. Interfacing a 5 V TTL output to the 3.3 V CMOS input requires a 10 K Ω current limiting resistor between the 5 V TTL output to the 3.3 V CMOS input. The current limiting resistor will form a LPF with the 2 pF input capacitance of the DSP input resulting in a 20 ns delay of the signal. This delay is acceptable since this interface will be used for low speed single ended point-to-point communication between the integrated drive and a personal computer at a maximum bit rate of 115.2 Kbps.

Two MMBZ5V6A transient voltage suppressors are mounted back-to-back to provide transient voltage protection for each of the MAX232A transmitter outputs and receiver inputs.

TIA/EIA-485 communication

To satisfy the bit rate requirement of 20 Mbps, a propriety data link protocol for the integrated drive control network is instantiated as a firmware component in the FPGA co-processor. The SN65HVD3088E is a TIA/EIA-485 transceiver capable of data transmission up to 20 Mbps and will be used for the balanced differential data transmission in the half-duplex multi point network. The multi point network will consist of six nodes, one for the main controller and one for each of the five integrated drives.

The TIA/EIA-485 network must make provision for appropriate bus termination. A 20 m length of CAT5e network cable will be used as a transmission line for the bus. The characteristic impedance Z_0 of this transmission line is specified as 100 Ω at 110 MHz. A parallel termination resistor of 100 Ω will be placed at the two extreme ends of the bus.

Fail safe biasing of the differential bus will be implemented since it provides a known state for all the transceivers when the bus is inactive. The fail safe biasing configuration is shown in Figure 4-4.

The requirement for fail safe biasing is that V_{FSB} be at least 200 mV, the receiver input threshold voltage and that the biasing network should not load the active driver. The pull-up resistor R_{PU} and the pull-down resistor R_{PD} should be the same value for symmetrical loading of the driver. The equivalent resistance of R_{PU} , R_{PD} and R_{O1} should also match the characteristic impedance of the transmission line. Given these requirements the resistor values for the TIA/EIA-485 network can be calculated.

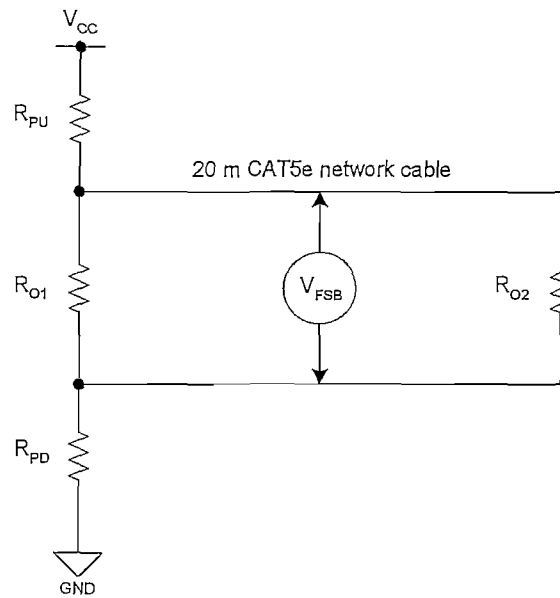


Figure 4-4 TIA/EIA-485 network fail safe biasing

The parallel bus termination resistors must match the characteristic impedance of the transmission line, Z_o . This gives

$$R_{O1} = R_{O2} = Z_o = 100 \, \Omega \quad (4-8)$$

The equivalent resistance of the parallel bus termination resistors is

$$\begin{aligned} R_{EQ} &= \frac{1}{\frac{1}{R_{O1}} + \frac{1}{R_{O2}}} \\ &= \frac{1}{\frac{1}{100} + \frac{1}{100}} \, \Omega \\ &= 50 \, \Omega \end{aligned} \quad (4-9)$$

With a supply voltage V_{CC} the fail safe voltage V_{FSB} is

$$V_{FSB} = V_{CC} \cdot \left(\frac{R_{EQ}}{R_{PU} + R_{PD} + R_{EQ}} \right) \quad (4-10)$$

Rearranging (4-10) the bias resistors R_{PU} , and R_{PD} can be calculated for a V_{CC} supply voltage of +5 V

$$\begin{aligned}
 (R_{PU} + R_{PD}) &= \left(\frac{V_{CC}}{V_{FSB}} \cdot R_{EQ} \right) - R_{EQ} \\
 &= \left(\frac{5}{0.2} \cdot 50 \right) - 50 \, \Omega \\
 &= 1200 \, \Omega
 \end{aligned} \tag{4-11}$$

However the requirement that the pull-up resistor R_{PU} and the pull-down resistor R_{PD} should be equal gives

$$R_{PU} = R_{PD} = 600 \, \Omega \tag{4-12}$$

The equivalent resistance R'_{O1} formed by R_{PU} , R_{PD} and R_{O1} must match the characteristic impedance of the transmission line

$$\begin{aligned}
 R'_{O1} &= \frac{1}{\frac{1}{R_{O1}} + \frac{1}{(R_{PU} + R_{PD})}} \\
 &= \frac{1}{\frac{1}{100} + \frac{1}{(600 + 600)}} \, \Omega \\
 &= 92.3 \, \Omega
 \end{aligned} \tag{4-13}$$

The equivalent resistance R'_{O1} can be more accurately matched to the characteristic impedance of the transmission line by recalculating R_{O1}

$$\begin{aligned}
 R_{O1} &= \frac{1}{\frac{1}{Z_O} - \frac{1}{(R_{PD} + R_{PU})}} \\
 &= \frac{1}{\frac{1}{100} - \frac{1}{(600 + 600)}} \, \Omega \\
 &= 109.09 \, \Omega
 \end{aligned} \tag{4-14}$$

The following standard resistance values are selected for the calculated values, $R_{PU} = R_{PD} = 619 \, \Omega$, with $R_{O1} = 110 \, \Omega$ and $R_{O2} = 100 \, \Omega$.

The selected standard resistance values are checked according to the requirement for fail safe biasing and characteristic impedance matching of the transmission line. Using (4-9) $R_{EQ} = 52.38 \, \Omega$, using (4-10) $V_{FSB} = 0.202 \, V$ and using (4-13) $Z_O = 101.02 \, \Omega$.

The SN65HVD3088E supply current is a function of the network data rate and the number of receiving nodes the active driver sees, in this case five. The fail safe biasing and impedance matching resistors also contribute to the supply current requirement. The supply current required by the SN65HVD3088E for this operating condition is approximately 50 mA.

A MMBZ5V6A transient voltage suppressor provides transient voltage protection for the SN65HVD3088E transmitter input and receiver output.

4.2 Power amplifier

The power amplifier consists of the following functional units:

- Filter
- Isolation circuitry
- Gate drive floating supply
- Gate drive circuitry
- Protection circuitry
- Power circuit
- Sense circuitry

In the following sections the detail design of the power amplifier functional units will be done. The detail design will be grouped into two sections namely gate drive circuitry and power circuit.

4.2.1 Gate drive

The gate drive circuitry for the power amplifier consists of isolation circuitry, the gate driver IC, a floating supply and the protection circuitry.

Isolation circuitry

Isolation circuitry is required to establish an isolation boundary between the digital controller circuitry and the power amplifier gate drive circuitry with minimum signal propagation delay. The HCPL-0631 from Agilent Technologies is a dual high speed opto-coupler capable of signal transmission at 10 Mbps. The implementation of the optical isolation function is shown in Figure 3-4. A SN74LVC14A hex Schmitt-trigger inverter is used as a buffer between the DSP on-chip PWM peripheral and the opto-coupler. The current limiting resistor for the opto-coupler light emitting diode is calculated according to (4-4). The opto-coupler output is an open collector

transistor that is pulled up to the +5 V supply rail via a 390 Ω resistor. This method of biasing allows the output of the opto-coupler to be connected directly to the input of the gate drive IC.

Gate drive IC

The IR2113 integrated gate drive IC complies with all the requirements for gate drive circuitry as listed in section 3.2.2. A block diagram depicting the internal functions of the IR2113 is shown in Figure 3-5. The device requires a V_{DD} supply of +5 V, a V_{CC} supply of +12 V and a floating supply for the driver circuitry of the upper IGBT in a bridge configuration. Local power supply decoupling of these supplies is essential. A 100 nF 0805 size SMD multilayer ceramic chip capacitor in X7R dielectric is used to decouple the V_{DD} supply while the V_{CC} supply is decoupled with a 1 μ F 1210 size SMD multilayer ceramic chip capacitor in X7R dielectric. The floating supply is also decoupled with a 1 μ F 1210 size SMD multilayer ceramic chip capacitor in X7R dielectric, since the current pulse required to turn on the upper IGBT will be supplied from this capacitor. The floating supply provides the average current to replenish the charge in the decoupling capacitor.

The floating supply requirements are determined by the quiescent current and leakage current for the high side driver circuitry as well as the current necessary to satisfy the total gate charge for the upper IGBT at the selected switching frequency. The quiescent current and leakage current for the high side driver circuitry is 230 μ A and 50 μ A respectively. The total gate charge for a 600 V IGBT capable of switching 15 A at 20 kHz is approximately 150 nC (IRG4BC40W). The minimum current necessary from the floating supply can be determined as follows

$$\begin{aligned} I_{float} &= Q_g \cdot f_{sw} + I_{quiescent} + I_{leak} \\ &= (150 \times 10^{-9}) \cdot (20 \times 10^3) + 230 \times 10^{-6} + 50 \times 10^{-6} \text{ A} \\ &= 3.28 \text{ mA} \end{aligned} \tag{4-15}$$

Since this is the minimum current required from the floating supply it can be multiplied with a safety factor.

The gate drive IC input pins, HIN and LIN are TTL compatible and can thus be connected directly to the open collector outputs of the isolation circuitry opto-coupler. The shutdown function of the gate drive IC has a maximum propagation delay time of 140 ns and is thus fast enough to implement an edge triggered pulse-for-pulse over current protection mechanism.

The gate drive IC output pins, LO and HO are capable of delivering a peak output current of 2 A. To limit the current within this range, a gate resistor is placed between the IC output pins and

the IGBT gates. The impedance of the gate circuit affects the turn-on time and the switching loss of the IGBT. To switch the IRG4BC40W on in 100 ns will require a gate current of

$$\begin{aligned} I_g &= \frac{Q_g}{t_{on}} \\ &= \frac{150 \times 10^{-9}}{100 \times 10^{-9}} \text{ A} \\ &= 1.5 \text{ A} \end{aligned} \quad (4-16)$$

The required gate current is within the 2 A limit of the IR2113 gate drive IC. The gate current is used to calculate the gate resistor as follows

$$\begin{aligned} R_g &= \frac{V}{I_g} \\ &= \frac{15}{1.5} \Omega \\ &= 10 \Omega \end{aligned} \quad (4-17)$$

A 10 Ω , 1206 SMD resistor is selected for R_g . In order to turn off the IGBT as fast as possible an anti-parallel Schottky diode, a PRL5819 is placed across the gate resistor. This improves the initial turn-off time of the current waveform but does not significantly influence the current “tail” section of the turn-off current. The reason for this is the charge stored in the base of the PNP structure of the IGBT is responsible for the current “tail”. Since this base is not accessible external drive circuitry cannot be used to improve this section of the switching time.

Floating supply

The floating supply generates a gate drive voltage higher than the bridge supply voltage for each high side power transistor in the three-phase bridge. A schematic representation of the transformer isolated floating supply is shown in Figure 4-5. One such supply, with three isolated outputs, will be used for each three-phase bridge.

The 100 KHz clock shown in Figure 4-5 is generated by the DSP and buffered by a SN74LVC14A hex Schmitt-trigger inverter. The buffered clock is fed into a TC4428 differential driver IC that switches the primary winding of the transformer. The transformer generates three isolated secondary voltages V_1 , V_2 and V_3 via the secondary windings N_{S1} , N_{S2} and N_{S3} . The diode and capacitor in each output form a peak rectifier stage with the resistor in each output providing a pre-load for the peak rectifier. The three secondary outputs are identical, each generating +15 V. The diodes $D1$, $D2$ and $D3$ are PRL5819 devices and the capacitors $C1$, $C2$

and $C3$ are $1\ \mu\text{F}$ 1210 size SMD multilayer ceramic chip capacitor in X7R dielectric. The resistors $R1$, $R2$ and $R3$ are $10\ \text{K}\Omega$ thus providing a $1.5\ \text{mA}$ pre-load for each output.

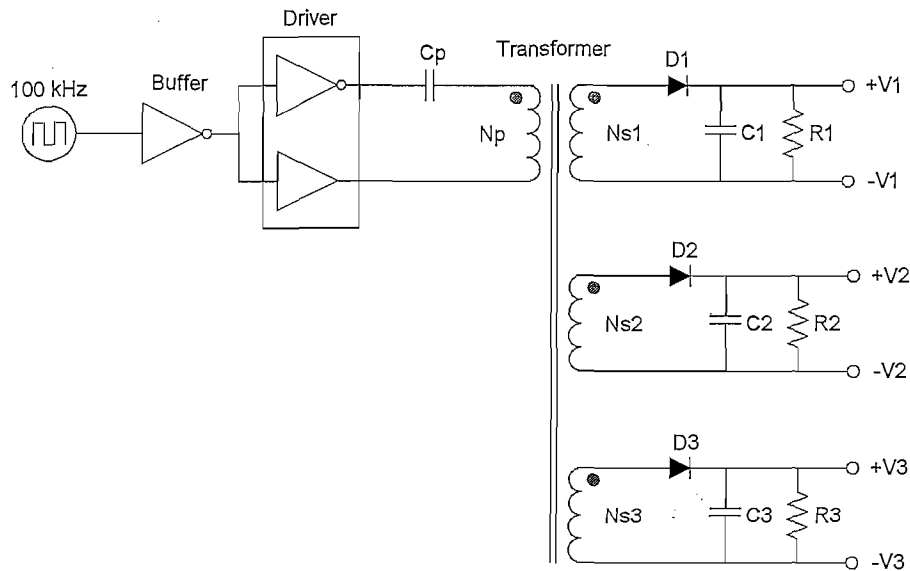


Figure 4-5 Floating supply

The transformer design is an iterative process governed by the size of the device instead of power loss since the power throughput is so small. Multiplying the current requirement obtained from (4-15) with a safety factor of three and adding the pre-load of $1.5\ \text{mA}$, the current required per output is approximately $12\ \text{mA}$. The power throughput of the transformer is determined by multiplying the $+15\ \text{V}$ output voltage with the output current of $12\ \text{mA}$ for each output, resulting in a total output power of $0.54\ \text{W}$.

The efficiency of the transformer will be poor because the output power is similar to the total power loss of the transformer. The total power loss of the transformer consists of core loss and copper loss. In this design the core loss will be dominant due to the small winding currents. The efficiency is estimated as 50% yielding a total power requirement of approximately $1\ \text{W}$.

As a departure point an EFD 12 core in 3F3 ferrite material will be selected for the transformer design. The EFD 12 core is capable of a power throughput well in excess of $1\ \text{W}$ at a switching frequency of $100\ \text{KHz}$ in the push-pull configuration used here, however as mentioned previously the design is governed by size.

The first step in the transformer design is to determine the number of primary turns for a particular flux density. The flux density is inversely proportional to the number of turns and directly proportional to the core power loss, thus requiring a tradeoff of turns versus core power loss. Using data, for 3F3 core material, of power loss as a function of flux density with frequency

as a parameter, a flux density of 260 mT is selected. The primary turns are now obtained from (4-18)

$$\begin{aligned}
 N_p &= \frac{V_p}{B \cdot A_e \cdot f_{sw}} \\
 &= \frac{12}{260 \times 10^{-3} \cdot 11.4 \times 10^{-6} \cdot 100 \times 10^3} \text{ Turns} \\
 &= 40 \text{ Turns}
 \end{aligned} \tag{4-18}$$

where:

- N_p = Number of primary turns
- V_p = Primary voltage
- B = Flux density in Tesla
- A_e = Effective core area for the EFD 12 core m^2
- f_{sw} = Transformer switching frequency in Hz.

The number of secondary turns can now be calculated using (4-19)

$$\begin{aligned}
 N_s &= \frac{(V_o + V_f) \cdot N_p}{V_p} \\
 &= \frac{(15 + 0.4) \cdot 40}{12} \text{ Turns} \\
 &= 51 \text{ Turns}
 \end{aligned} \tag{4-19}$$

where:

- N_s = Number of secondary turns
- V_f = Diode forward voltage drop
- V_o = Output voltage.

The total number of turns required to fit onto the EFD 12 coil former is 193. The minimum winding area for the coil former is 6.5 mm^2 . This equates to a cross sectional area of 0.0337 mm^2 per conductor, excluding inter layer and final layer isolation. To avoid several iterations of the winding design it is necessary to multiply the available area per conductor with a stacking factor. A conservative stacking factor of 0.5 gives a cross sectional area of 0.0169 mm^2 per conductor. From this the final conductor diameter is calculated as 0.14 mm.

The EFD 12 core satisfies the requirements since the 193 turns of 0.14 mm wire fill the available coil former winding area resulting in an optimal transformer design. The temperature

rise of the floating supply transformer will be measured in the final design. A temperature rise of 20 °C to 30 °C above ambient will be considered acceptable.

Protection circuitry

A temperature sensor IC will provide the most versatile solution for the over temperature protection function of the power amplifier. The Dallas Semiconductor DS18S20 digital thermometer provides 9-bit centigrade temperature measurements over the operating temperature range of –55 °C to +125 °C. The device is accurate to ± 0.5 °C over the temperature range of –10 °C to +85 °C. The DS18S20 communicates with a master controller by means of the 1-Wire® protocol. The 1-Wire® bus only requires three connections, ground, +3.3 V supply and a single data line. The device also contains nonvolatile over and under temperature alarm triggers that are user programmable. The DS18S20 take approximately 750 ms to convert a temperature measurement. A 1-Wire® bus master will be instantiated on the FPGA coprocessor to interface the DS18S20 to the integrated controller. The DS18S20 is packaged in a TO-92 package that can be attached to the power amplifier substrate with thermal epoxy. Figure 4-6 shows the 1-Wire® interface between the 18S20 and the FPGA.

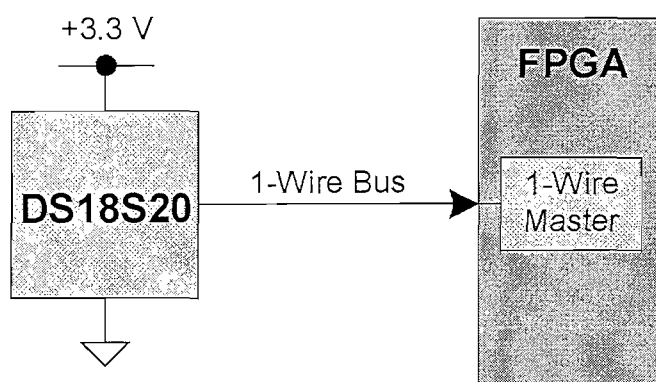


Figure 4-6 1-Wire® interface

Continuous over current protection will be derived from the AMB coil current measurement performed by the integrated current transducer. The AMB coil current measurement will be used in the high sample rate control algorithms and thus be available for continuous current limit implementation.

The pulse-for-pulse current limit occurs at the rate of the PWM switching frequency and will be implemented via the IR2113 integrated gate drive IC shutdown pin with a maximum propagation delay of 140 ns. A 2 W non-inductive power metal film resistor senses the IGBT current. The sensed voltage is filtered and compared to a reference by an ultra-fast TTL comparator, the MAX 913. The output of the comparator drives the shutdown pin of the IR2113 integrated gate

drive IC. A schematic representation of the pulse-for-pulse current limit circuit is shown in Figure 4-7.

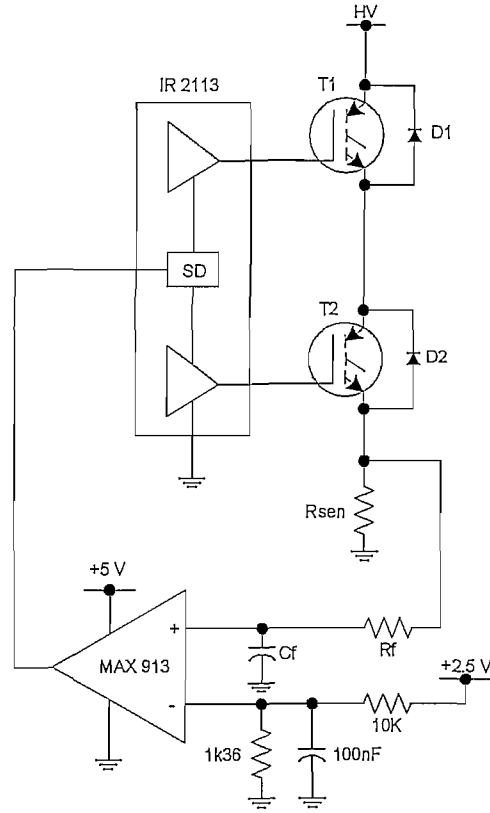


Figure 4-7 Pulse-for-pulse current limit

The power amplifier peak current is specified as 15 A while the RMS current is specified as 7.5 A. A 2 W non-inductive power metal film resistor will be able to dissipate 1 W continuously at an ambient temperature of 70 °C without any de-rating. Therefore the required resistance of the sense resistor is

$$\begin{aligned}
 R_{sen} &= \frac{P}{I_{rms}^2} \\
 &= \frac{1}{(7.5)^2} \Omega \\
 &= 0.018 \Omega
 \end{aligned}
 \tag{4-20}$$

A 2 W, 0.02 Ω Dale power metal film resistor is used. The voltage developed across the sense resistor for a peak current of 15 A is

$$\begin{aligned}
 V_{sen} &= I_{pk} \times R_{sen} \\
 &= 15 \times 0.02 \text{ V} \\
 &= 0.3 \text{ V}
 \end{aligned}
 \tag{4-21}$$

The sensed voltage is filtered before being applied to the input of the MAX 913 comparator to avoid false triggering of the pulse-for-pulse current limit. The filter is a single order low pass resistor-capacitor filter with a cut-off frequency approximately equal to five times the amplifier switching frequency. This gives a cut-off frequency of 250 kHz. The filter resistor is selected as 1 K Ω that gives a filter capacitor value of

$$\begin{aligned} C_f &= \frac{1}{2 \cdot \pi \cdot f_c \cdot R_f} \\ &= \frac{1}{2 \cdot \pi \cdot 250 \times 10^3 \cdot 1 \times 10^3} \text{ F} \\ &= 636.6 \text{ pF} \end{aligned} \quad (4-22)$$

A 560 pF ceramic chip capacitor is selected giving a cut-off frequency of 284 kHz.

The comparator requires a 0.3 V reference that is generated with a 2.5 V precision voltage reference and a resistor divider network. The resistor divider network allows the peak current limit level for the power amplifier to be adjusted. If one resistor in the divider network is chosen as 10 K Ω the other resistor is calculated as 1.36 K Ω . The divider network is decoupled with a 100 nF multilayer ceramic chip capacitor in X7R dielectric.

The MAX 913 is an ultra-fast TTL comparator with a propagation delay of approximately 10 ns. The comparator operates from a single 5 V supply with 6 mA of supply current. The TTL output of the comparator is connected directly to the shutdown pin of the IR2113 integrated gate drive IC.

4.2.2 Power circuit

The power circuitry includes the dual three-phase bridge, the filter and the sense circuitry.

Sense circuitry

The AMB coil voltage and current will be used in self-sensing algorithms to extract rotor position information.

An integrated current transducer will be used to measure the AMB coil current. The LAH 25-NP device from LEM allows for extremely accurate measurement of DC, AC and pulsed currents with galvanic isolation between the load and the subsequent signal conditioning circuitry. The LAH 25-NP is an active device that makes use of the Hall effect to measure current and thus requires a DC power supply to operate. The key features of this device are listed in Table 4-3.

Table 4-3 Current transducer specifications

Parameter	Value
Primary nominal current	25 A
Primary current measurement range	0-55 A
Conversion ratio	1:1000, 2:1000, 3:1000
Accuracy	$\pm 0.3\%$
Bandwidth	200 kHz
di/dt limit	200 A/ μ s
Supply voltage	± 12 Vdc
Current consumption	10 mA
Rated operating voltage	600 V
Rated isolation voltage	5000 V
Ambient operating temperature range	-25 °C to +85 °C

The power amplifier peak current is specified as 15 A while the RMS current is specified as 7.5 A. The ripple current component of the coil current that is used in the self-sensing algorithm is a triangle waveform with a peak-to-peak amplitude of approximately 350 mA at a supply voltage of 50 V. The period of the ripple current is 50 μ s, the PWM switching period. The bandwidth of the LAH 25-NP current transducer is 200 kHz which is ten times higher than the PWM switching frequency. Given these requirements, it is evident from the transducer specifications listed in Table 4-3 that the LAH 25-NP is ideally suited to measure the AMB coil current. The circuitry required to interface the LAH 25-NP output to the FPGA co-processor forms part of the analog interface circuitry as shown in Figure 4-8.

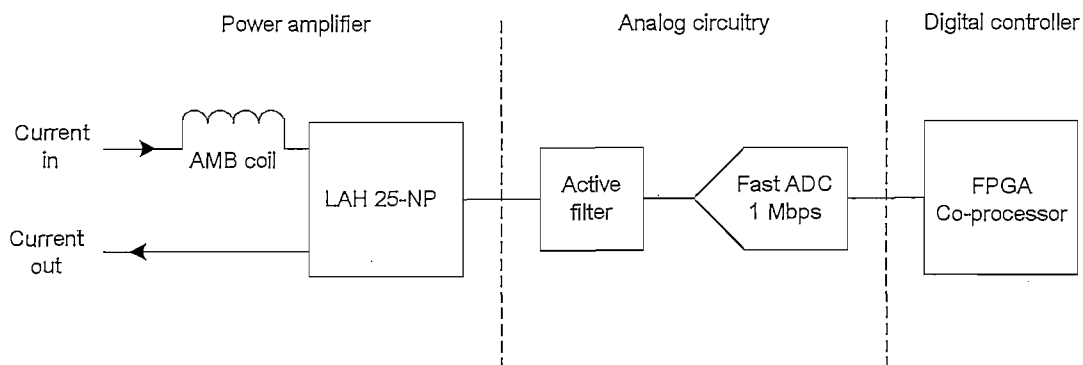


Figure 4-8 LAH 25-NP interface

A voltage divider, configured from discrete resistors, will be used to attenuate the AMB coil voltage to an acceptable level before being measured differentially by a conventional instrumentation amplifier. The voltage divider requires a sensitivity of 0.0267 V/V. The power

dissipation in the resistors is limited to 0.25 W that allows the use of 1206 package SMD resistors. The voltage divider configuration is shown in Figure 4-9.

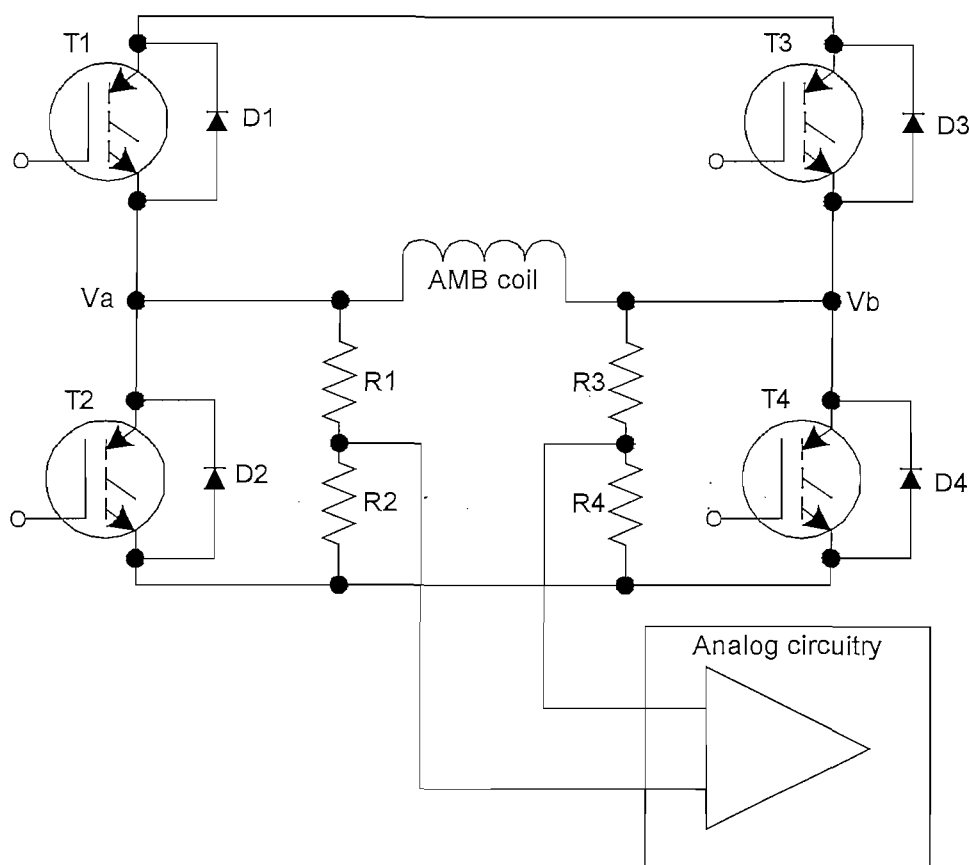


Figure 4-9 Voltage divider circuit

Referring to Figure 4-9, with V_a at 150 V and V_b at 0 V, the voltage across resistor R_1 is 146 V and the voltage across resistor R_2 is 4 V. The value of R_1 is given by (4-23)

$$\begin{aligned} R_1 &= \frac{V^2}{P} \\ &= \frac{(146)^2}{0.25} \Omega \\ &= 85.26 \text{ k}\Omega \end{aligned} \quad (4-23)$$

Selecting R_1 as 100 k Ω allows power de-rating for the 0.25 W resistor according to (4-24)

$$\begin{aligned} P &= \frac{V^2}{R_1} \\ &= \frac{(146)^2}{100 \times 10^3} \text{ W} \\ &= 0.21 \text{ W} \end{aligned} \quad (4-24)$$

The value of R_2 can now be determined

$$\begin{aligned} R_2 &= R_1 \times V/V \\ &= 100 \times 10^3 \times 0.0267 \, \Omega \\ &= 2.67 \, \text{k}\Omega \end{aligned} \quad (4-25)$$

The power dissipation in R_2 is negligible. Resistor R_3 is equal to R_1 and resistor R_4 is equal to R_2 . In order to preserve accuracy and common mode rejection the resistors must be very accurate, 0.1% to 0.01%, and be placed very close together for thermal equilibrium.

Filter

A high quality decoupling capacitor must be placed directly across each half bridge leg of the three-phase bridge to attenuate high frequency noise that exists as a result of stray inductance in the high current path of the power amplifier. In order to be effective the decoupling capacitor must be placed as close as possible to the IGBTs on the power amplifier substrate.

The CS6 range of MLP capacitors manufactured by ITW Paktron are ultra-low ESR devices in SMD packaging. The 1 μF CS6 capacitor has an ESR of 0.05 Ω at a frequency of 20 KHz. Since two half bridge legs are combined to form an H-bridge or modified H-bridge, the total decoupling capacitance is doubled and the ESR is effectively halved. The power dissipation in each decoupling capacitor for an RMS current 7.5 A is given by (4-26).

$$\begin{aligned} P &= I_{rms}^2 \cdot ESR \\ &= (7.5)^2 \cdot \frac{0.05}{2} \, \text{W} \\ &= 1.4 \, \text{W} \end{aligned} \quad (4-26)$$

The manufacturer doesn't provide a coefficient to translate the power dissipation in the decoupling capacitor into a temperature rise.

Dual three-phase bridge

The design of the dual three-phase bridge will be done according to the functional specifications listed in Table 4-5. Since the dual bridges are identical the design will only consider one three-phase bridge. The first step in the design is to identify suitable switching components for the bridge. In section 2.4.2 the IGBT was identified as the preferred power switch and will thus be used for this design.

Table 4-4 Power amplifier specifications

Parameter	Specification
Supply voltage	50 V to 150 V DC
Nominal load current	7.5 A RMS
Peak load current	15 A
Pulse-for-pulse current limit level	15 A
Switching frequency	20 kHz to 50kHz
Small signal bandwidth	2500 Hz

The IGBT doesn't contain an integral reverse diode like the MOSFET. The absence of the internal diode allows the designer the flexibility of choosing an external diode or using a co-pak IGBT. A co-pak is a specially manufactured IGBT that contains a reverse diode on the same die. This simplifies the PCB layout and minimizes the lead inductance of the device. However the two component implementation offers a better thermal solution since the current density in the die is effectively halved by using individual components for the IGBT and the diode. Individual IGBTs and diodes are preferred for the three-phase bridge since they offer increased flexibility and superior thermal performance in comparison to the co-pak solution.

IGBT

IGBTs are available in various switching speed grades with the slower devices optimized for reduced conduction loss whereas the faster devices are optimized for reduced switching loss. International Rectifier provides a graph of operating current versus frequency for IGBTs in a half-bridge switching topology operated with a clamped inductive load. Such a graph is shown in Figure 4-10 for the IRG4BC40WS warp-speed IGBT.

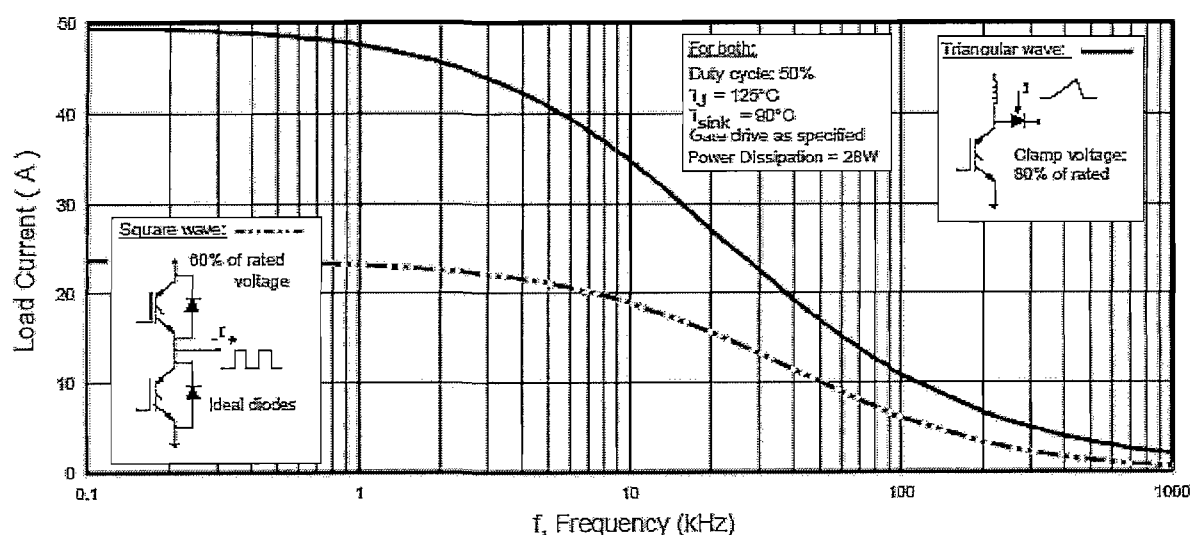


Figure 4-10 Operating current versus frequency for the IRG4BC40WS [54]

Figure 4-10 provides a convenient method for selecting the optimum device based on operating current and frequency since it takes thermal constraints, conduction loss and switching loss into consideration. From Figure 4-10 it can be seen that the IRG4BC40WS is capable of switching 16 A_{rms} at a switching frequency of 20 kHz. The IRG4BC40WS is available in SMD packaging and thus suitable for mounting on the power amplifier substrate.

The IGBT power losses consist of switching loss and conduction loss. The switching loss is determined using manufacturer data for total switching energy versus junction temperature. This data is related to specific test parameters that are directly proportional to the switching energy, thus the data has to be scaled before being used here. The switching energy data scale factors are given in Table 4-5.

Table 4-5 IGBT switching energy scale factors

Parameter	Test data value	Three-phase bridge value	Scale factor
Collector-emitter voltage	480 V	150 V	0.3125
Gate-source voltage	15 V	15 V	1
Gate resistor	10 Ω	10 Ω	1
Load current	10 A	7.5 A	0.75
Junction temperature	150 °C	150 °C	1

Using the scaled values from Table 4-5, the total switching energy is calculated as

$$\begin{aligned}
 E_{ts} &= 0.3125 \times 0.75 \times E_{ts(data)} \\
 &= 0.3125 \times 0.75 \times 400 \times 10^{-6} \text{ J} \\
 &= 93.75 \times 10^{-6} \text{ J}
 \end{aligned} \tag{4-27}$$

The switching power loss is determined by multiplying the total switching energy by the switching frequency

$$\begin{aligned}
 P_{sw(IGBT)} &= E_{ts} \cdot f_{sw} \\
 &= 93.75 \times 10^{-6} \times 20 \times 10^3 \text{ W} \\
 &= 1.88 \text{ W}
 \end{aligned} \tag{4-28}$$

In reality the switching loss will be higher than the calculated value because the calculated value represents the switching power loss with an ideal freewheel diode. The reverse recovery characteristic of a practical freewheel diode will increase the turn-on switching loss of the IGBT.

The conduction power loss of the IGBT is determined using the manufacturer data for on-state voltage drop across the collector-emitter junction versus temperature. The conduction power loss is the product of the voltage drop across the collector-emitter junction and the load current. The conduction power loss at a junction temperature of 150 °C is

$$\begin{aligned} P_{on(IGBT)} &= V_{ce(on)} \cdot I_L \\ &= 1.55 \times 7.5 \text{ W} \\ &= 11.63 \text{ W} \end{aligned} \quad (4-29)$$

The total power loss per IGBT is given by (4-28) and (4-29)

$$\begin{aligned} P_{total(IGBT)} &= P_{on(IGBT)} + P_{switch(IGBT)} \\ &= 11.63 + 1.88 \text{ W} \\ &= 13.51 \text{ W} \end{aligned} \quad (4-30)$$

Freewheel diode

The HFA25TB60S is an ultra-fast, soft recovery diode that is particularly well suited for use as a freewheel diode for IGBTs. The HFA25TB60S is a 600 V diode capable of an average forward current of 25 A with a reverse recovery time of 70 ns. The HFA25TB60S is available in SMD packaging and thus suitable for mounting on the power amplifier substrate.

The diode power losses also consist of switching loss and conduction loss. The switching loss in the diode occurs at turn-off when the diode current reverses for the reverse recovery time t_{rr} . The reverse recovery current waveform is a triangle shape with the area of the waveform representing the reverse recovery charge Q_{rr} . The base of the triangle waveform is equal to the reverse recovery time t_{rr} while the height is equal to the reverse recover current I_{rr} . Using the manufacturer data, the switching loss for the HFA25TB60S is calculated as

$$\begin{aligned} P_{sw(diode)} &= V_R \cdot Q_{rr} \cdot f_{sw} \\ &= \frac{1}{2} \cdot V_R \cdot I_{rr} \cdot t_{rr} \cdot f_{sw} \\ &= 0.5 \cdot 150 \cdot 7.5 \cdot 70 \times 10^{-9} \cdot 20 \times 10^3 \text{ W} \\ &= 0.79 \text{ W} \end{aligned} \quad (4-31)$$

The conduction loss for the HFA25TB60S is calculated using the forward current and data for the forward voltage drop V_F as follows

$$\begin{aligned}
 P_{on(diode)} &= V_F \cdot I_F \\
 &= 1.1 \cdot 7.5 \text{ W} \\
 &= 8.25 \text{ W}
 \end{aligned} \tag{4-32}$$

The total power loss per freewheel diode is given by (4-31) and (4-32)

$$\begin{aligned}
 P_{total(diode)} &= P_{sw(diode)} + P_{on(diode)} \\
 &= 0.79 + 8.25 \text{ W} \\
 &= 9.04 \text{ W}
 \end{aligned} \tag{4-33}$$

Sense resistor power loss

The 0.02 Ω current sense resistor also contributes towards the total power loss of the three-phase bridge:

$$\begin{aligned}
 P_{Rsen} &= I_{rms}^2 \cdot R_{sen} \\
 &= (7.5)^2 \cdot 0.02 \text{ W} \\
 &= 1.13 \text{ W}
 \end{aligned} \tag{4-34}$$

Total power dissipation

Since the dual three-phase bridges can be configured for various switching topologies, the total power dissipation will depend on the specific topology used. Two modified H-bridge amplifiers is the most economic topology to suspend a 1 DOF AMB, the total power dissipation for this configuration is given by (4-35).

$$\begin{aligned}
 P_{total} &= 4 \cdot (P_{total(IGBT)} + P_{total(diode)} + P_{Rsen}) \\
 &= 4 \cdot (13.51 + 9.04 + 1.13) \text{ W} \\
 &= 94.72 \text{ W}
 \end{aligned} \tag{4-35}$$

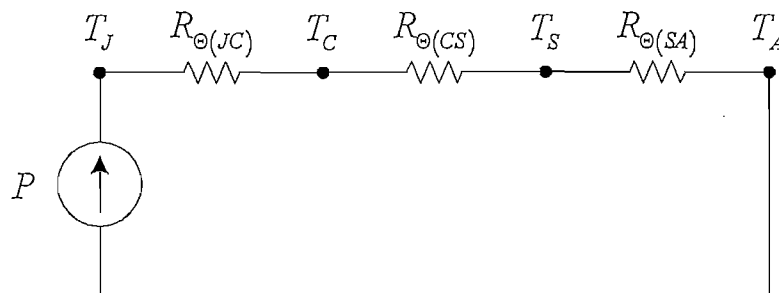
Thermal design

The case temperature of the sense resistor and the junction temperature of the IGBTs and diodes will rise as a result of power dissipation. The temperature rise must be controlled so that the specified maximum junction temperature for these components is not exceeded. A heat sink, in conjunction with the power amplifier insulated metal substrate will conduct the heat away from the components to the ambient and thus maintain the junction temperature within safe limits. The substrate will be clamped to a heat sink as indicated in section 3.6, however this section of the design will concentrate on the thermal interface between the substrate and the

power components. Members of the McTronX research group will be responsible for the heat sink selection as indicated in section 3.5. There will be no forced air cooling available thus the power amplifier will rely on heat transfer by means of conduction, radiation and natural convection.

The IGBTs, diodes and the sense resistors are SMD packages and thus soldered directly on to the power amplifier insulated metal substrate and thus don't require electrically isolating thermal pads. This drastically reduces the thermal resistance between the component and the substrate. The aim of the thermal design is to determine the maximum allowable substrate temperature for the sense resistor, the diode and the IGBT at the nominal power dissipation level calculated previously. The component that requires the lowest substrate temperature will determine the size of the heat sink.

The simple thermal model shown in Figure 4-11 is used to determine the maximum allowable substrate temperature for the devices.



Where:

P	Power dissipation
T_J	Junction temperature
T_C	Case temperature
T_S	Substrate temperature
T_A	Ambient temperature
$R_{\Theta(JC)}$	Thermal resistance, junction to case
$R_{\Theta(CS)}$	Thermal resistance, case to substrate
$R_{\Theta(SA)}$	Thermal resistance, substrate to ambient

Figure 4-11 Power amplifier thermal model

Although the components are soldered directly to the substrate and don't require electrically isolating thermal pads, there is still a finite case-to-sink thermal resistance due to the solder joint that has to be considered in the thermal design. The diode and the IGBT are packaged in a D²Pak SMD package with a solder pad area of 101.6 mm². The solder used to solder the

components to the substrate is a 63 Sn / 37 Pb alloy with a thermal conductivity of 50 W/m °C. The height of the solder joint is approximately 80 µm and represents the length of the thermal path. With this information the case-to-sink thermal resistance of the diode and IGBT can be calculated using (4-36)

$$\begin{aligned} R_{\Theta(\infty)} &= \frac{l}{A \cdot k} \\ &= \frac{80 \times 10^{-6}}{101.6 \times 10^{-6} \cdot 50} \text{ °C/W} \\ &= 0.016 \text{ °C/W} \end{aligned} \quad (4-36)$$

where:

- A = Area of the solder pad in m²
 k = Thermal conductivity in W/m °C
 l = The length of the thermal path in m.

The maximum allowable substrate temperature that the diode can tolerate is calculated using manufacturers data for maximum junction temperature, junction-to-case thermal resistance and the previously calculated power loss for the diode

$$\begin{aligned} T_s &= T_J - P_{total(diode)} \cdot (R_{\Theta(JC)} + R_{\Theta(CS)}) \\ &= 150 - 9.04 \cdot (1.0 + 0.016) \text{ °C} \\ &= 140.8 \text{ °C} \end{aligned} \quad (4-37)$$

The maximum allowable substrate temperature that the IGBT can tolerate is calculated using manufacturers data for maximum junction temperature, junction-to-case thermal resistance and the previously calculated power loss for the IGBT

$$\begin{aligned} T_s &= T_J - P_{total(IGBT)} \cdot (R_{\Theta(JC)} + R_{\Theta(CS)}) \\ &= 150 - 13.51 \cdot (0.77 + 0.016) \text{ °C} \\ &= 139.4 \text{ °C} \end{aligned} \quad (4-38)$$

The sense resistor is rated at 2 W up to 70 °C without any thermal de-rating. From 70 °C the 2 W is de-rated down to 0 W at 275 °C resulting in a de-rating factor of 102.5 °C/W. The case temperature of the sense resistor can be calculated for the 1.13 W power dissipation previously calculated

$$\begin{aligned}
 T_C &= 275 - (1.13 \cdot 102.5) \text{ } ^\circ\text{C} \\
 &= 159.7 \text{ } ^\circ\text{C}
 \end{aligned}
 \tag{4-39}$$

The sense resistor SMD package has a solder pad area of 69.67 mm². Using (4-36) this gives a case-to-sink thermal resistance of 0.023 °C/W for the sense resistor. The maximum allowable substrate temperature that the sense resistor can tolerate for the 1.13 W power dissipation is

$$\begin{aligned}
 T_S &= T_C - P_{R_{sen}} \cdot R_{\Theta(cs)} \\
 &= 159.7 - (1.13 \cdot 0.023) \text{ } ^\circ\text{C} \\
 &= 159.67 \text{ } ^\circ\text{C}
 \end{aligned}
 \tag{4-40}$$

The IGBT is the component that represents the thermal limit for the substrate temperature at 139.4 °C. The DS18S20 temperature sensor IC will be attached to the power amplifier substrate with thermal epoxy and thus provide over temperature protection for the power amplifier. The power amplifier can be shut down when the substrate reaches a too high temperature. The shut down temperature is configured in the FPGA firmware and is thus easily adapted for a particular power amplifier configuration and power level.

The power amplifier substrate is 159 mm by 235 mm that gives an area of 0.0374 m². From the manufacturers data, the thermal resistance of the substrate is 0.45 °C/W. The total power dissipation for two modified H-bridge amplifiers considered here is 94.7 W. Thus at an ambient temperature of 25 °C the substrate temperature will rise to

$$\begin{aligned}
 T_S &= R_{\Theta(sA)} \cdot P_{total} + T_A \\
 &= (0.45 \cdot 94.7) + 25 \text{ } ^\circ\text{C} \\
 &= 67.6 \text{ } ^\circ\text{C}
 \end{aligned}
 \tag{4-41}$$

This substrate temperature rise is particularly low. The actual temperature will be measured during operational conditions to verify this result.

Amplifier small signal bandwidth

In order to predict the amplifier small signal bandwidth, a current control loop has to be closed around the amplifier. The current loop is designed by selecting a compensator transfer function that eliminates the pole in the AMB coil transfer function and provides sufficient gain at the desired cross-over frequency to ensure a small signal bandwidth of 2.5 kHz. A single pole-zero compensator with a pole situated at 0 Hz and a zero coincident with the pole in the AMB coil

transfer function will provide the required response. Such a compensator is shown in Figure 4-12.

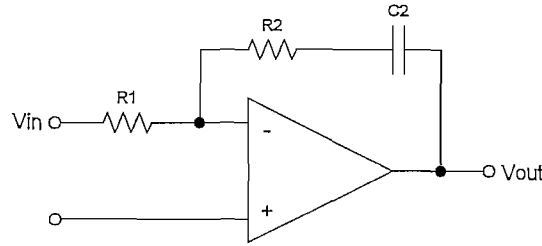


Figure 4-12 Pole-zero compensator

The transfer function for this compensator in the Laplace domain is given by (4-42)

$$\begin{aligned}\frac{V_{out}}{V_{in}}(s) &= \frac{R_2 + \frac{1}{s \cdot C_2}}{R_1} \\ &= \frac{1 + s \cdot R_2 \cdot C_2}{s \cdot R_1 \cdot C_2}\end{aligned}\quad (4-42)$$

The AMB coil resistance is $0.2 \, \Omega$ and the coil inductance is $7.2 \, \text{mH}$. The time constant of the AMB coil is given by (4-43)

$$\begin{aligned}\tau &= \frac{L_{coil}}{R_{coil}} \\ &= \frac{7.2 \times 10^{-3}}{0.2} \, \text{s} \\ &= 0.036 \, \text{s}\end{aligned}\quad (4-43)$$

The Laplace domain transfer function for the AMB is given by (4-44)

$$\begin{aligned}\frac{I(s)}{V(s)} &= \frac{\frac{1}{R_{coil}}}{1 + s \cdot \frac{L_{coil}}{R_{coil}}} \\ &= \frac{1}{1 + s \cdot \tau}\end{aligned}\quad (4-44)$$

A block diagram of the proposed closed loop system is shown in Figure 4-13. The amplifier is represented as a pure gain in the Laplace domain. The amplifier gain factor K_{PWM} is equal to the

amplifier supply voltage divided by the peak value of the triangle used to generate the PWM signal. In this case K_{PWM} is equal to 16.67. A Bode plot of the open loop response of the amplifier and the AMB coil will reveal the gain required at the zero frequency to ensure a small signal bandwidth of 2.5 kHz.

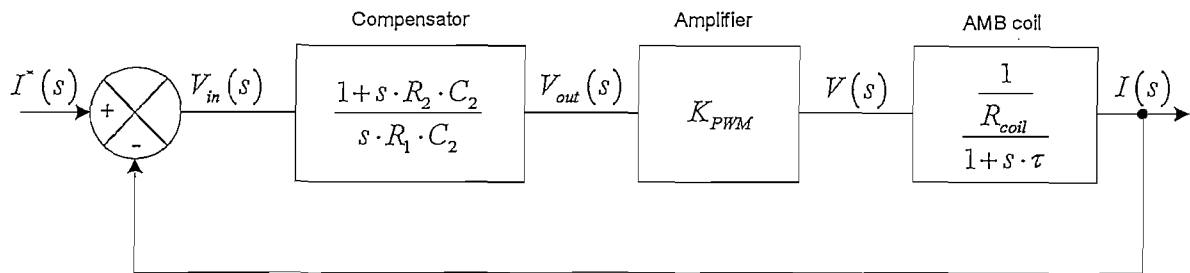


Figure 4-13 Current loop block diagram

The open loop response is plotted from $V_{out}(s)$ to $I(s)$ with the unity feedback path open. A Bode plot of the open loop response is shown in Figure 4-14. The open loop response is typical for a first-order system with a -20 dB per decade slope for the gain and an overall phase shift of -90 degrees.

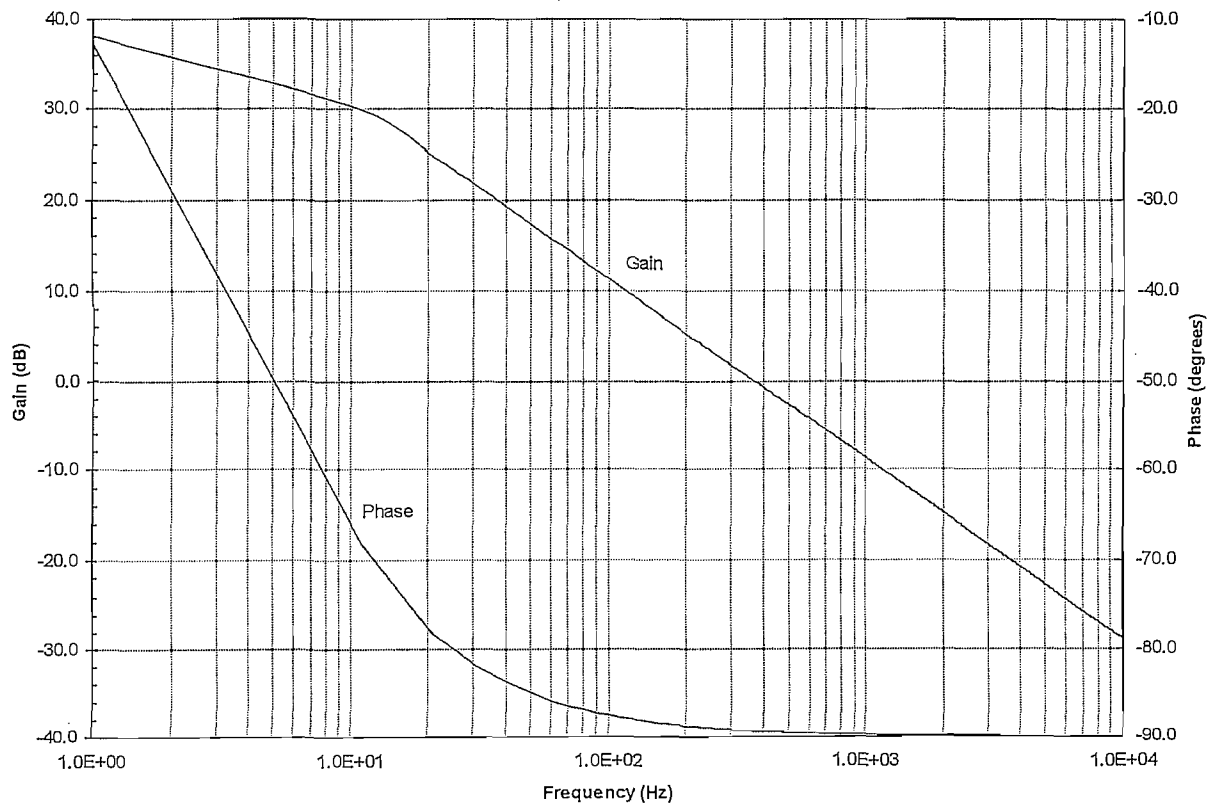


Figure 4-14 Open loop response

Designing the compensator involves calculating suitable values for R_1 , R_2 and C_2 to ensure a closed loop small signal bandwidth of 2.5 kHz. From the open loop Bode plot in Figure 4-14 the

gain at 2.5 kHz is -16.5 dB. The compensator must thus add a gain of +16.5 dB to the closed loop system at the zero frequency. Before the gain can be adjusted, the compensator zero is calculated to coincide with the pole in the AMB coil transfer function as follows

$$\begin{aligned}\tau &= R_2 \cdot C_2 \\ &= 0.036 \text{ s}\end{aligned}\tag{4-45}$$

Choosing the value of R_2 in (4-45) as 10 k Ω , gives a value for C_2 of 3.6 μ F. The compensator gain is given by (4-46)

$$\text{Gain} = 20 \log \left(\frac{R_2}{R_1} \right)\tag{4-46}$$

Using (4-47) the value of R_1 is calculated to add the required gain of +16.5 dB to the closed loop system

$$\begin{aligned}R_1 &= \frac{R_2}{\log^{-1} \left(\frac{16.5}{20} \right)} \\ &= \frac{10 \times 10^3}{6.68} \Omega \\ &= 1.5 \text{ k}\Omega\end{aligned}\tag{4-47}$$

The closed loop response is plotted from $I^*(s)$ to $I(s)$ with the unity feedback path closed. From the Bode plot of the closed loop response shown in Figure 4-15, the amplifier small signal bandwidth is 2.5 kHz.

Although the current loop has been designed in the s-domain, all the control algorithms for the integrated controller will be implemented as sample data controllers in the z-domain. This implies that the compensator transfer function given by (4-42) will have to be transformed into its equivalent digital form by means of the bilinear transformation. This involves implementing the following substitution

$$s = \frac{2}{T} \cdot \frac{z-1}{z+1}\tag{4-48}$$

where T is the sample period of the digital controller. The sampling period will be a fifth of the required system time constant of 400 μ s, thus T is equal to 80 μ s.

Applying the bilinear transformation gives the digital compensator as

$$H(z) = H(s) \bigg|_{s = \frac{T}{1-z^{-1}}} = \frac{6.674 - 6.659 \cdot z^{-1}}{1 - z^{-1}} \quad (4-49)$$

The difference equation form for (4-49) is

$$y(n) = 6.674 \cdot x(n) - 6.659 \cdot x(n-1) + y(n-1) \quad (4-50)$$

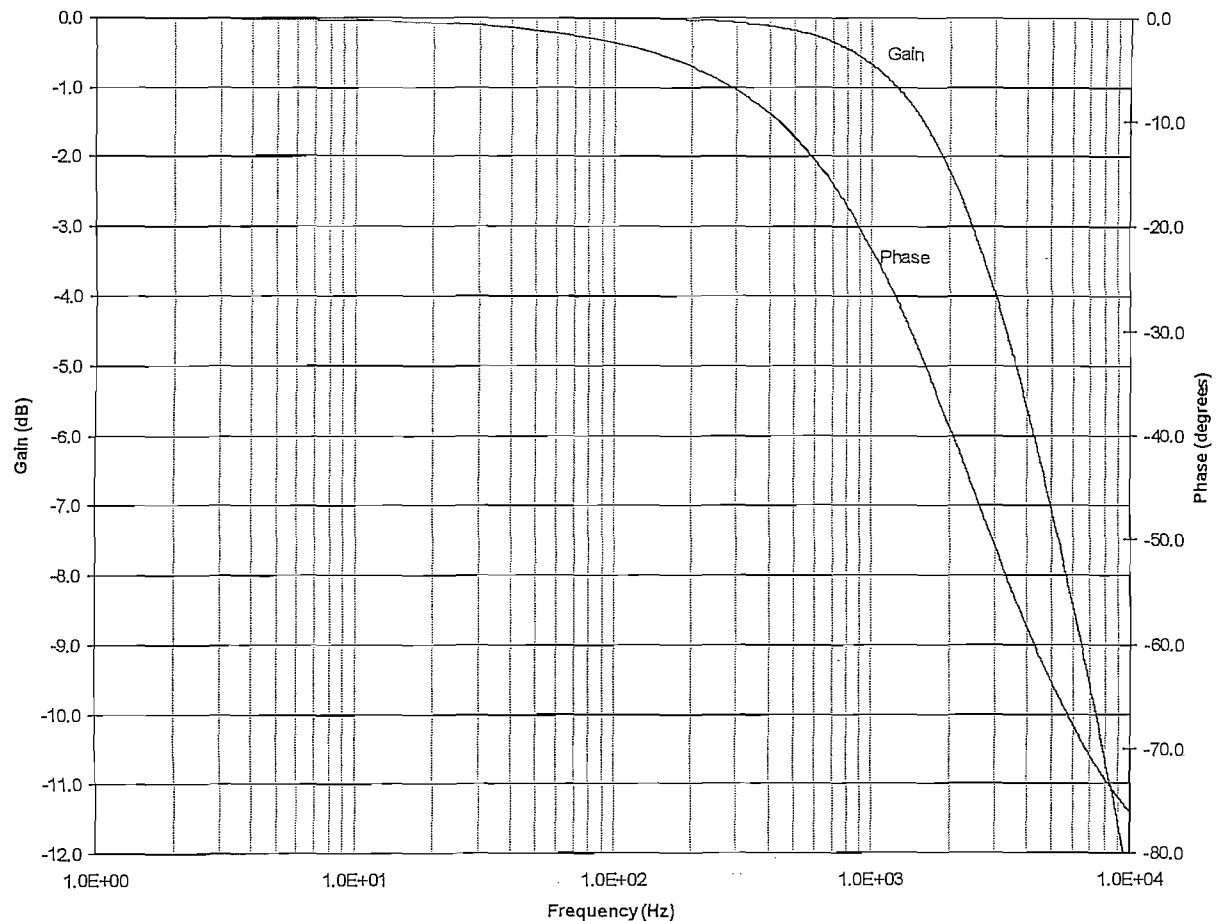


Figure 4-15 Closed loop response

4.3 Electronic supply

The electronic supply consists of the following functional units:

- DC-to-DC converter
- FPGA power supply
- DSP power supply

In the following sections the detail design of the electronic supply functional units will be done. A detail design will be presented for the DC-to-DC converter, the DSP power supply and the FPGA power supply.

4.3.1 DC-to-DC converter

The design of the DC-to-DC converter will be divided in three sections namely the transformer design, component selection and control design. The DC-to-DC converter is a transformer coupled flyback topology operated in discontinuous current mode with current mode PWM control. The relationship between the input voltage and output voltage for this topology is given by (4-51)

$$\frac{V_o}{V_{IN}} = \frac{N_s}{N_p} \cdot \left(\frac{D}{1-D} \right) \quad (4-51)$$

where:

- V_o = Output voltage
- V_{in} = Input voltage
- N_s = Number of transformer secondary turns
- N_p = Number of transformer primary turns
- D = Duty cycle.

Table 4-6 list the various output voltages and currents that the flyback DC-to-DC converter has to generate, including the isolation requirements.

Table 4-6 Flyback power supply requirements

Voltage	Current	Power	Isolation reference	Use
+5 V	5 A	25 W	Digital ground	Digital electronics
+12 V	0.01 A	0.12 W	Digital ground	Digital electronics
+12 V_A	0.2 A	2.4 W	Analog ground	Analog electronics
-12 V_A	0.2 A	2.4 W	Analog ground	Analog electronics
+12 V_P	0.01 A	0.12 W	Power ground	Power electronic control circuitry
+5 V_P	0.02 A	0.1 W	Power ground	Power electronic control circuitry
+12 V_IC	0.01 A	0.12 W	Power ground	Power supply control IC

The DC supply voltage to the integrated controller can be varied between 50 V and 150 V. The flyback power supply must tolerate this variation while regulating the output voltages specified in Table 4-6. The efficiency of the power supply is estimated as 80% and will thus require 37.5 W

of input power to generate the total output power of 30 W. The switching frequency of the flyback power supply is chosen as 50 kHz in order to minimize the frequency dependant losses in the power supply. Since the flyback power supply is operated in discontinuous mode the duty cycle has to be limited to 50% to allow complete demagnetization of the flyback transformer core. The maximum duty cycle is chosen as 0.48 that allows a safety margin to ensure complete demagnetization of the transformer core. The above mentioned operating parameters are summarized in Table 4-7.

Table 4-7 Flyback power supply operating parameters

Parameter	Value
Minimum input voltage, $V_{in(min)}$	50 V
Maximum input voltage, $V_{in(max)}$	150 V
Total output power, P_{out}	30 W
Estimated efficiency, η	0.8
Switching frequency, F_{sw}	50 kHz
Maximum duty cycle, D_{max}	0.48

The requirements and operating parameters specified in Table 4-6 and Table 4-7 are used to do the detail design of the flyback power supply.

Transformer

The duty cycle is the ratio of the on-time versus the total switching period of the converter as given by (4-52)

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T_{sw}} = t_{on} \cdot f_{sw} \quad (4-52)$$

The maximum on-time for the converter can thus be calculated

$$\begin{aligned}
 t_{on(max)} &= \frac{D_{max}}{f_{sw}} \\
 &= \frac{0.48}{50 \times 10^3} \text{ s} \\
 &= 9.6 \text{ } \mu\text{s}
 \end{aligned} \quad (4-53)$$

The flyback power supply transformer is actually an inductor since it stores energy in the primary winding during the converter on-time and transfers the stored energy to the secondary winding during the converter off-time. The transformer turns ratio is used to adjust the

relationship between the input voltage and output voltage. The minimum primary winding inductance required to store the energy during the converter on-time is calculated using (4-54)

$$\begin{aligned}
 L_p &= \frac{(V_{in(min)} \cdot t_{on(max)}) \cdot f_{sw} \cdot \eta}{2 \cdot P_{out}} \\
 &= \frac{(50 \cdot 9.6 \times 10^{-6})^2 \cdot 50 \times 10^3 \cdot 0.8}{2 \cdot 30} \text{ H} \\
 &= 153.6 \text{ } \mu\text{H}
 \end{aligned} \tag{4-54}$$

Since 153.6 μH is the minimum inductance required, the actual inductance is selected as 155 μH . The peak current in the primary winding can now be calculated

$$\begin{aligned}
 \hat{I}_p &= \frac{V_{in(min)} \cdot t_{on(max)}}{L_p} \\
 &= \frac{50 \cdot 9.6 \times 10^{-6}}{155 \times 10^{-6}} \text{ A} \\
 &= 3.1 \text{ A}
 \end{aligned} \tag{4-55}$$

The calculated values for the primary inductance and peak current are verified according to the required primary power

$$\begin{aligned}
 P_{in} &= \frac{1}{2} \cdot L_p \cdot \hat{I}_p^2 \cdot f_{sw} \\
 &= \frac{1}{2} \cdot 155 \times 10^{-6} \cdot (3.1)^2 \cdot 50 \times 10^3 \text{ W} \\
 &= 37.24 \text{ W}
 \end{aligned} \tag{4-56}$$

This correlates well with the estimated input power of 37.5 W. The EFD 25 core in 3F3 ferrite material is capable of the power throughput required with an appropriate air gap in the magnetic path. The manufacturer's data shows the maximum standard gap length for this core is 0.57 mm with an inductance factor, A_L of 160 nH/(Turn)². Using this data the primary turns are calculated as follows

$$\begin{aligned}
 N_p &= \sqrt{\frac{L_p}{A_L}} \\
 &= \sqrt{\frac{155 \times 10^{-6}}{160 \times 10^{-9}}} \text{ Turns} \\
 &= 32 \text{ Turns}
 \end{aligned} \tag{4-57}$$

The introduction of an air gap in the magnetic path of the core increases the magnetic field intensity, H , however the saturation flux density B_{sat} will remain unchanged. Therefore the flux density, B , has to be verified for the calculated primary inductance, primary peak current, cross sectional area of the core and number of primary turns

$$\begin{aligned}
 B &= \frac{L_p \cdot \hat{I}_p}{N_p \cdot A_{core}} \\
 &= \frac{155 \times 10^{-6} \cdot 3.1}{32 \cdot 55 \times 10^{-6}} \text{ T} \\
 &= 0.273 \text{ T}
 \end{aligned} \tag{4-58}$$

The calculated flux density is well below 0.4 T, the saturation flux density for this core material. The number of transformer secondary turns is calculated for the 5 V and 12 V outputs using (4-59)

$$N_s = N_p \cdot \left[\frac{(V_{out} + V_f) \cdot (1 - D_{max})}{V_{in(min)} \cdot D_{max}} \right] \tag{4-59}$$

where V_f is the forward voltage drop of the rectifier in the power supply output. A Schottky rectifier, 12CWQ10FN, with a forward volt drop of 0.65 V is used for the 5 V and 12 V outputs. The number of secondary turns for each 5 V output is

$$\begin{aligned}
 N_{5V} &= 32 \cdot \left[\frac{(5 + 0.65) \cdot (1 - 0.48)}{50 \cdot 0.48} \right] \text{ Turns} \\
 &= 3.92 \text{ Turns}
 \end{aligned} \tag{4-60}$$

Since a fractional number of turns are impractical, the number of secondary turns for each 5 V output is rounded up to 4 turns. The number of secondary turns for each 12 V output is

$$\begin{aligned}
 N_{12V} &= 32 \cdot \left[\frac{(12 + 0.65) \cdot (1 - 0.48)}{50 \cdot 0.48} \right] \text{ Turns} \\
 &= 8.77 \text{ Turns}
 \end{aligned} \tag{4-61}$$

Once again a fractional number of turns are impractical, thus the number of secondary turns for each 12 V output is rounded up to 9 turns. A schematic diagram of the flyback transformer is shown in Figure 4-16.

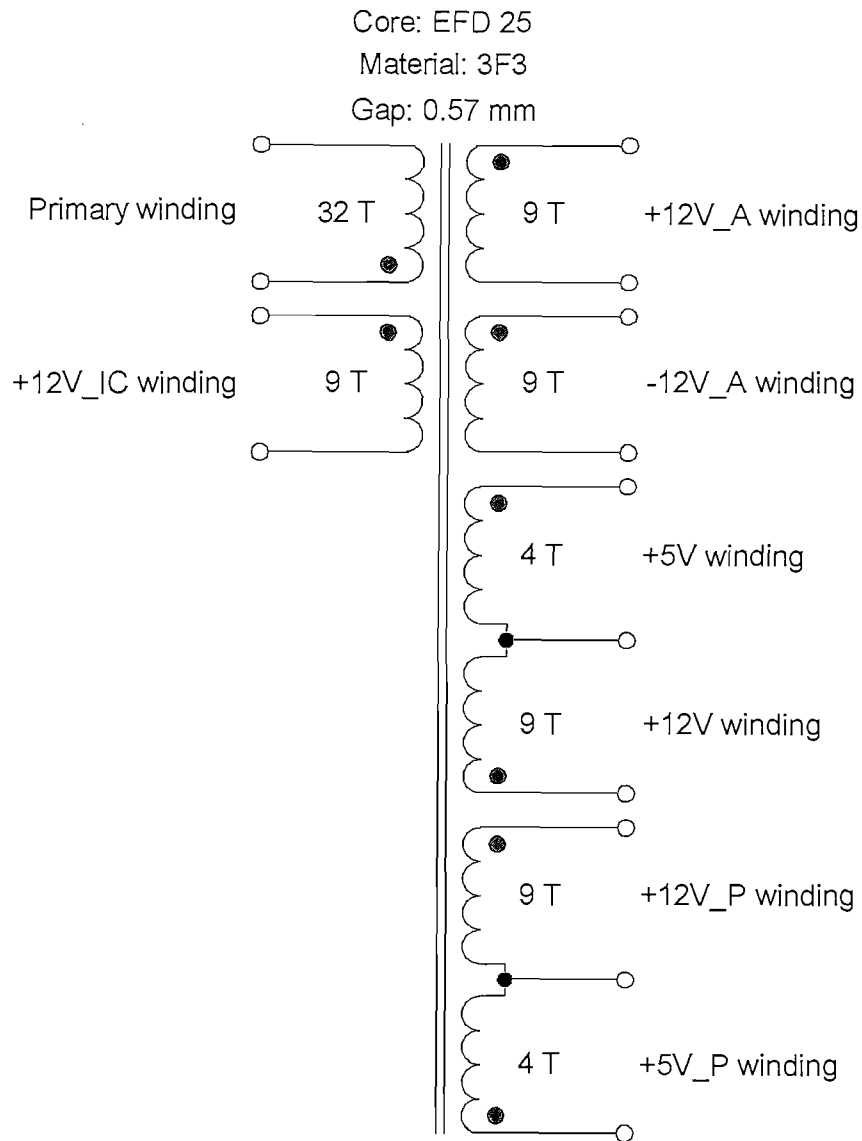


Figure 4-16 Flyback transformer schematic

The transformer winding design is done for a current density, J , of 6 A per mm² that will limit the temperature rise in the transformer to approximately 20 °C above the ambient temperature as result of copper loss. The power loss in the transformer is also a function of core loss and should thus be measured. The results of the winding design are tabulated in Table 4-8.

Table 4-8 Flyback transformer winding design

Winding	Turns	Wire diameter	Number of strands
Primary	32	0.45 mm	1
+12 V_A	9	0.45 mm	1
-12 V_A	9	0.45 mm	1
+5 V	4	0.315 mm	1
+12 V	9	0.315 mm	1
+12 V_P	9	0.315 mm	1

+5 V_P	4	0.45 mm	2
+12 V_IC	9	0.315 mm	1

This concludes the flyback transformer design.

Component selection

The following section of the design will concentrate on component for the flyback power supply. The heart of the power supply is the PWM controller IC. The MIC38HC45BM is a current mode PWM controller in an eight pin SMD package that offers all the necessary features to implement a discontinuous mode flyback controller with current mode PWM control. The device offers features such as under voltage lockout, built-in reference voltage, built-in error amplifier and current sense comparator. The device's output duty cycle is limited at 50%, a key feature for discontinuous mode flyback operation.

The peak current of 3.1 A in the primary winding of the transformer is switched via a power MOSFET. The IRFR430A is a 500 V device that is capable of switching 5 A that makes it ideally suited for this application. The RMS current that heats the MOSFET is given by

$$\begin{aligned}
 I_{rms} &= \hat{I}_p \cdot \sqrt{\frac{D_{max}}{3}} \\
 &= 3.1 \cdot \sqrt{\frac{0.48}{3}} \text{ A} \\
 &= 1.24 \text{ A}
 \end{aligned} \tag{4-62}$$

The IRFR430A has a on-resistance of 1.7 Ω and will thus have to be soldered to a sufficiently large copper pad on the PCB to dissipate the 2.6 W of power loss due to the RMS current heating. The IRFR430A has a total gate charge of 24 nC so it can be driven directly by the 1 A peak output of the MIC38HC45BM current mode PWM controller.

The peak primary current of 3.1 A is converted into a sense voltage by a non-inductive power resistor. The sensed voltage, after being filtered, is used for current mode control feedback in the current mode PWM controller. The sensed current is compared to a 1 V threshold in the MIC38HC45BM. The sense resistor value is calculated by adding a 10% margin to the peak current

$$\begin{aligned}
 R_{sense} &= \frac{V_{sense}}{1.1 \cdot \hat{I}_p} \\
 &= \frac{1}{3.4} \Omega \\
 &= 0.29 \Omega
 \end{aligned}
 \tag{4-63}$$

The closest standard value resistance is 0.27 Ω . The primary RMS current is used to determine the power dissipation in the sense resistor as follows

$$\begin{aligned}
 P_{Rsense} &= I_{rms}^2 \cdot R_{sense} \\
 &= (1.24)^2 \cdot 0.27 \text{ W} \\
 &= 0.42 \text{ W}
 \end{aligned}
 \tag{4-64}$$

A 0.27 Ω non-inductive 1 W power resistor is used to sense the peak primary current.

The primary current is reflected to the secondary by the transformer turns ratio. The output filter capacitors have to accommodate the RMS component of the reflected current in terms of output voltage ripple and self heating. The reflected +5 V RMS current is given by (4-65)

$$\begin{aligned}
 I_{rms(5V)} &= \hat{I}_p \sqrt{\frac{D_{max}}{3}} \cdot \left(\frac{N_p}{N_{5V}} \right) \\
 &= 3.1 \sqrt{\frac{0.48}{3}} \cdot \left(\frac{32}{4} \right) \text{ A} \\
 &= 9.92 \text{ A}
 \end{aligned}
 \tag{4-65}$$

A parallel combination of eight 100 μF low ESR tantalum capacitors is necessary to satisfy this requirement. A plot of RMS ripple current versus frequency for eight parallel 100 μF Kemet T495 tantalum capacitors is shown in Figure 4-17 where the allowable RMS current for this combination of capacitors is just over 10 A at a frequency of 50 kHz.

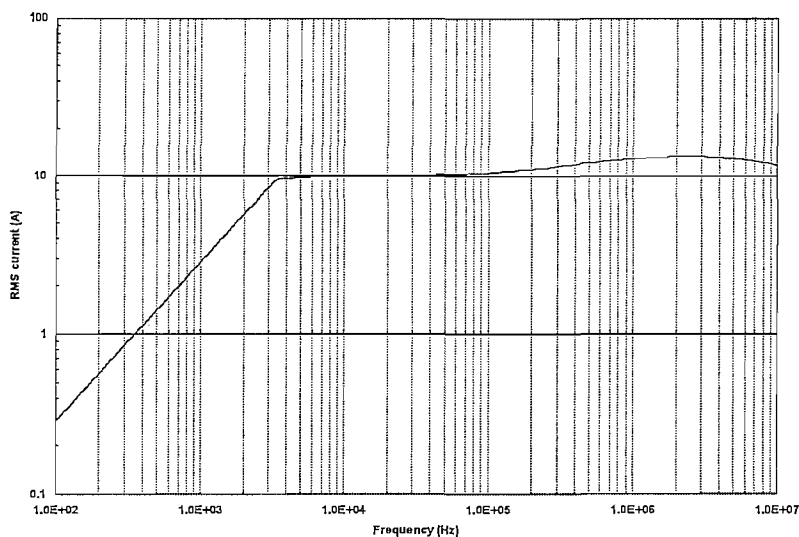


Figure 4-17 RMS current vs frequency for eight parallel 100 uF tantalum capacitors

The reflected +12 V RMS current is given by

$$\begin{aligned}
 I_{rms(12V)} &= \hat{I}_p \cdot \sqrt{\frac{D_{max}}{3}} \cdot \left(\frac{N_p}{N_{12V}} \right) \\
 &= 3.1 \sqrt{\frac{0.48}{3}} \cdot \left(\frac{32}{9} \right) \text{ A} \\
 &= 4.4 \text{ A}
 \end{aligned} \tag{4-66}$$

A parallel combination of six 22 μF low ESR tantalum capacitors easily satisfies this requirement. A plot of RMS ripple current versus frequency for six parallel 22 μF Kemet T495 tantalum capacitors is shown in Figure 4-18.

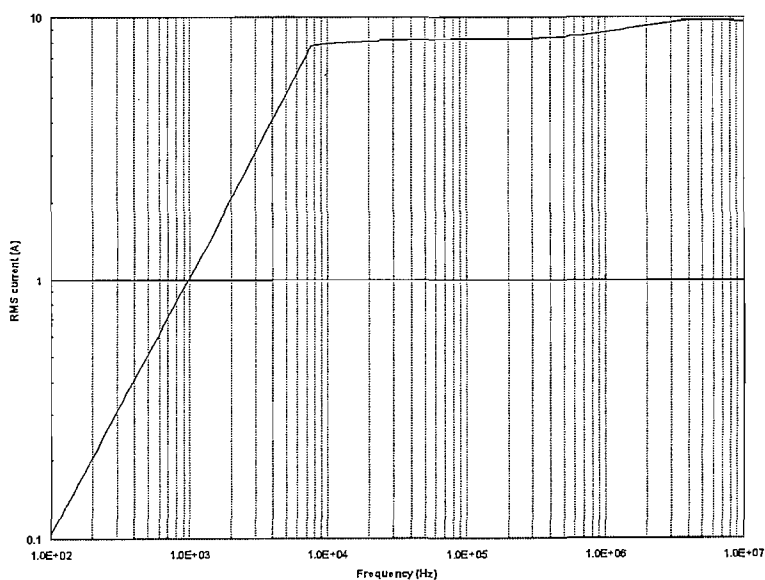


Figure 4-18 RMS current vs frequency for six parallel 22 uF tantalum capacitors

Figure 4-18 shows the allowable RMS current for this combination of capacitors is just under 8 A at a frequency of 50 kHz

Control design

The flyback power supply is implemented with peak current mode PWM control. Current mode control requires two feedback loops, an inner current feedback loop and an outer voltage feedback loop. The current feedback loop is implemented by sensing the peak primary current via a sense resistor. The sensed current, after being filtered, is compared to the voltage feedback loop and together they determine the required pulse width to maintain output voltage regulation.

Table 4-6 shows that the +5 V output is the highest power output and will thus be the directly controlled output with the voltage feedback loop closed around it. All the other outputs rely on the dynamic cross regulation between the transformer windings for output voltage regulation.

In order to simplify the control design, a component level simulation model of the flyback power supply is created using PSpice®. This simulation model considers the +5 V output since this is the controlled output, however the output capacitance, load resistance and ESR of the auxiliary windings are accounted for by reflecting them to the +5 V output. The simulation model contains an equivalent output capacitance C_2 , an equivalent load resistance R_4 and an equivalent ESR R_3 . The equivalent values are reflected to the +5 V output via the square of the transformer turns ratio. A schematic of the simulation model is shown in Figure 4-19.

Referring to Figure 4-19, the block labeled $U1$ is a simulation sub-circuit that represents the discontinuous current mode power stage of the flyback power supply. The block labeled $U2$ is a simulation sub-circuit that represents the peak current mode PWM controller. The operational amplifier $U3$ and its associated components C_3 , C_4 , R_7 and R_8 form the compensation circuit. The simulation sub-circuits are fully described in [56].

The objective of the control design is to determine suitable values for C_3 , C_4 , R_7 and R_8 so that the power supply operates stably for the minimum and maximum variations in output load and input voltage. The stability criteria for the power supply are a phase margin of 45 degrees and a gain margin of 6 dB.

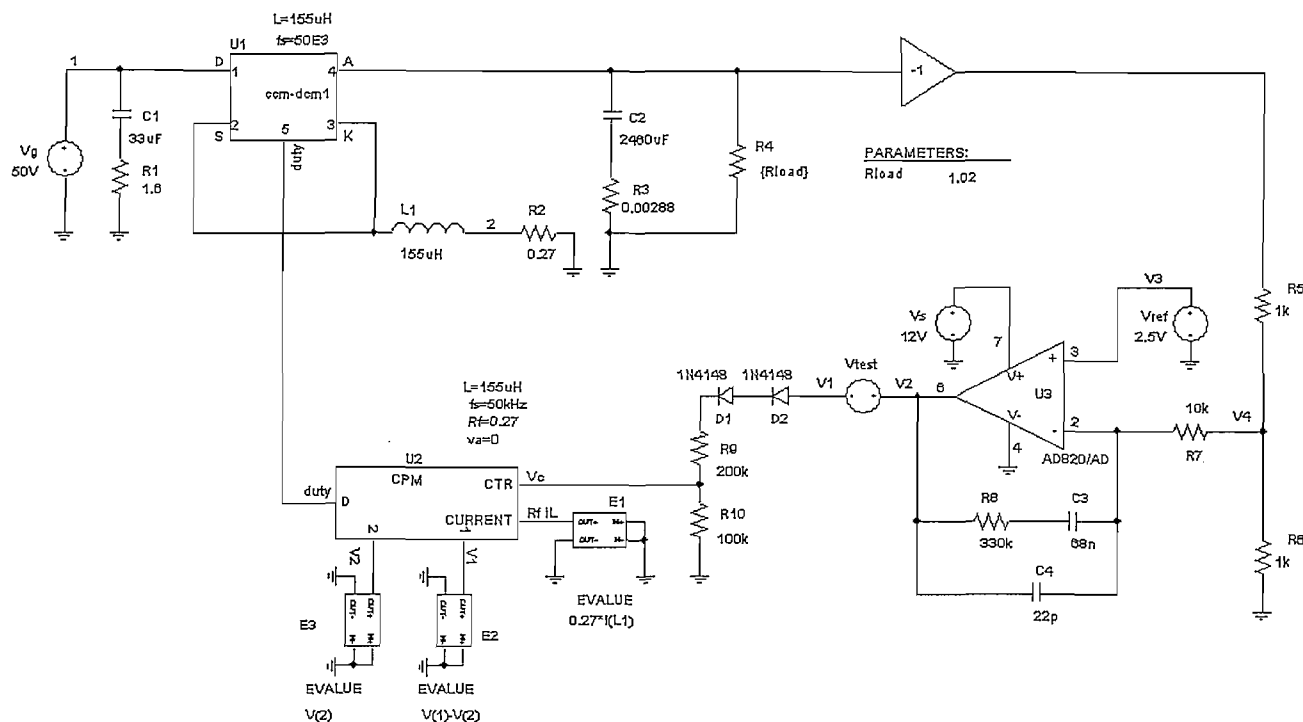


Figure 4-19 Flyback power supply simulation circuit

The simulation circuit in Figure 4-19 is based on the voltage injection approach to measuring loop response as detailed in [56]. The voltage source V_{test} is used to inject AC voltage variations into the system without opening the feedback loop. The advantage of this approach is that the DC bias conditions are established by the actual simulation circuit and thus the loop response measurement is made at the actual circuit operating point. To satisfy the impedance matching requirement of this technique, the injection point is selected between the low impedance output of the compensator and the high impedance PWM simulation sub-circuit input.

A Bode plot of the uncompensated loop transfer of the power supply is used to select an appropriate gain crossover frequency. The loop transfer bode plot is measured at maximum input voltage and minimum load. This represents a worst case condition in terms of maximum gain with minimum damping. The operational amplifier $U3$ is given unity gain by setting R_8 equal to R_7 and removing C_3 , and C_4 . The loop transfer is plotted from the point marked $V1$ to the point marked $V2$ in Figure 4-19. The uncompensated loop transfer Bode plot is shown in Figure 4-20.

As can be seen from Figure 4-20 the loop transfer of the discontinuous flyback converter is characterized by a dominant pole determined by the power stage with a zero at higher frequency due to the output capacitance and ESR.

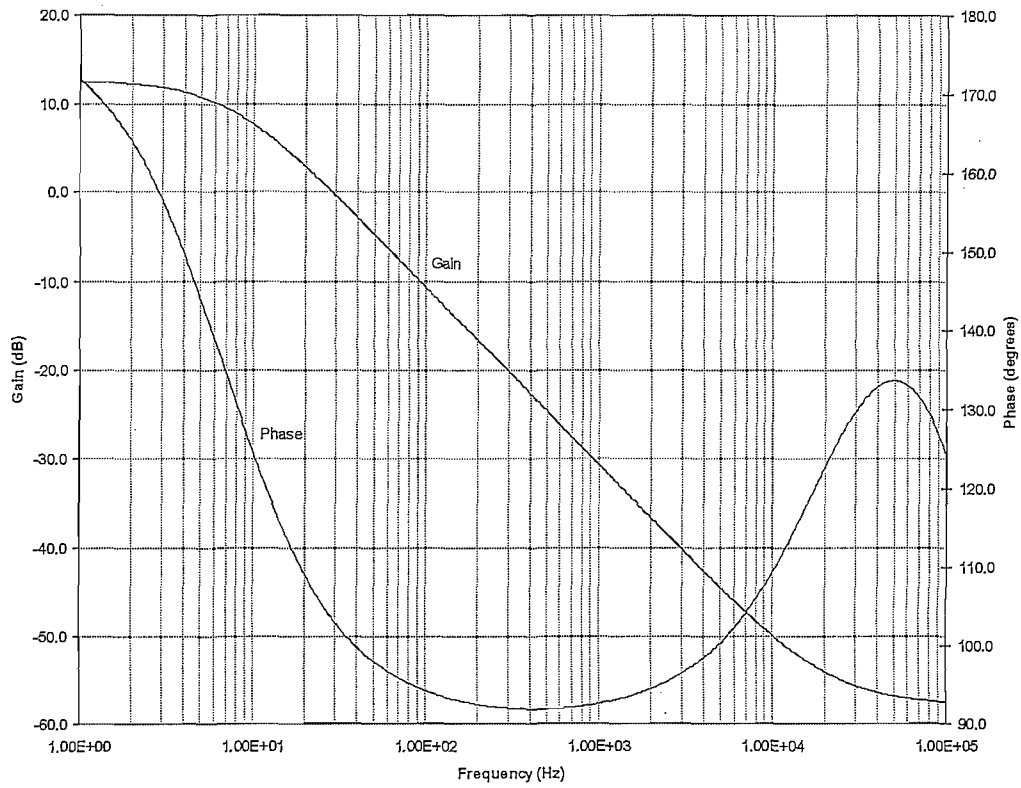


Figure 4-20 Flyback power supply uncompensated loop transfer Bode plot

From Figure 4-20, a compensated gain crossover frequency of 1 kHz appears realistic. Since the load characteristic of the power supply is fairly constant a higher crossover frequency is not considered necessary. The gain at 1 kHz is -30 dB. Thus the compensator has to add +30 dB to the loop gain in order to achieve the selected crossover frequency. The ratio of R_7 and R_8 sets the compensator gain. For R_7 equal to 10 k Ω , R_8 is calculated as follows

$$\begin{aligned}
 R_8 &= \log^{-1} \left(\frac{\text{Gain}}{20} \right) \cdot R_7 \\
 &= \log^{-1} \left(\frac{30}{20} \right) \cdot 10 \times 10^3 \, \Omega \\
 &= 316 \, \text{k}\Omega
 \end{aligned} \tag{4-67}$$

R_8 is chosen as a 330 k Ω standard value resistor. To guarantee sufficient phase at 1 kHz, the phase is boosted at 7 Hz, the frequency of the power stage pole, by means of the zero in the compensator transfer function formed by C_3 and R_8 . The value of C_3 is calculated as follows

$$\begin{aligned}
 C_3 &= \frac{1}{2 \cdot \pi \cdot f_z \cdot R_8} \\
 &= \frac{1}{2 \cdot \pi \cdot 7 \cdot 330 \times 10^3} \, \text{F} \\
 &= 68.9 \, \text{nF}
 \end{aligned} \tag{4-68}$$

C_3 is chosen as a 68 nF standard value capacitor. The high frequency pole in the compensator transfer function, formed by C_4 and R_8 is selected to cancel the zero formed by the output capacitance and it's ESR, effectively resulting in a single pole loop transfer. The value of C_4 is calculated using (4-69)

$$\begin{aligned}
 C_4 &= \frac{1}{2 \cdot \pi \cdot f_p \cdot R_8} \\
 &= \frac{1}{2 \cdot \pi \cdot 22.5 \times 10^3 \times 330 \times 10^3} \text{ F} \\
 &= 21.4 \text{ pF}
 \end{aligned} \tag{4-69}$$

C_4 is chosen as a 22 pF standard value capacitor. With the compensator design complete the gain and phase margin of the power supply must be verified for the calculated compensator values. This is done by plotting the loop transfer from $V1$ to $V2$ with the compensator in the loop as shown in Figure 4-19. The measurement is made at minimum input voltage and maximum equivalent load. The Bode plot of the loop transfer from $V1$ to $V2$ with the compensator in the loop is shown in Figure 4-21.

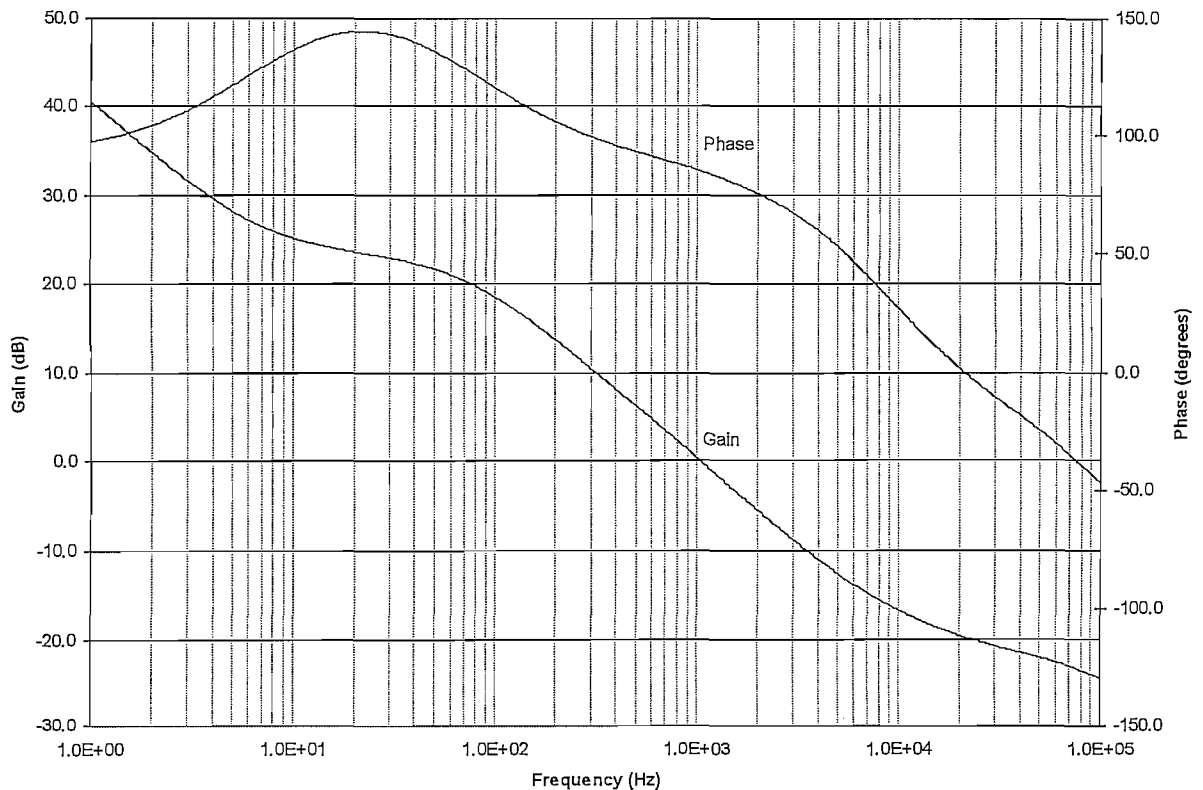


Figure 4-21 Flyback power supply compensated loop transfer Bode plot

From Figure 4-21 the cross over frequency is fractionally higher than the selected value of 1 kHz. The compensated system has a phase margin of 86 degrees and a gain margin of 20 dB.

The final step in the compensator design is to plot the closed loop transfer of the power supply at minimum input voltage and maximum load. This represents a worst case condition in terms of minimum gain and maximum damping. The closed loop transfer of the power supply is plotted from the point marked V3 to the point marked V4 in Figure 4-19, effectively from the reference to the measured output. The closed loop transfer of the flyback power supply is shown in Figure 4-22.

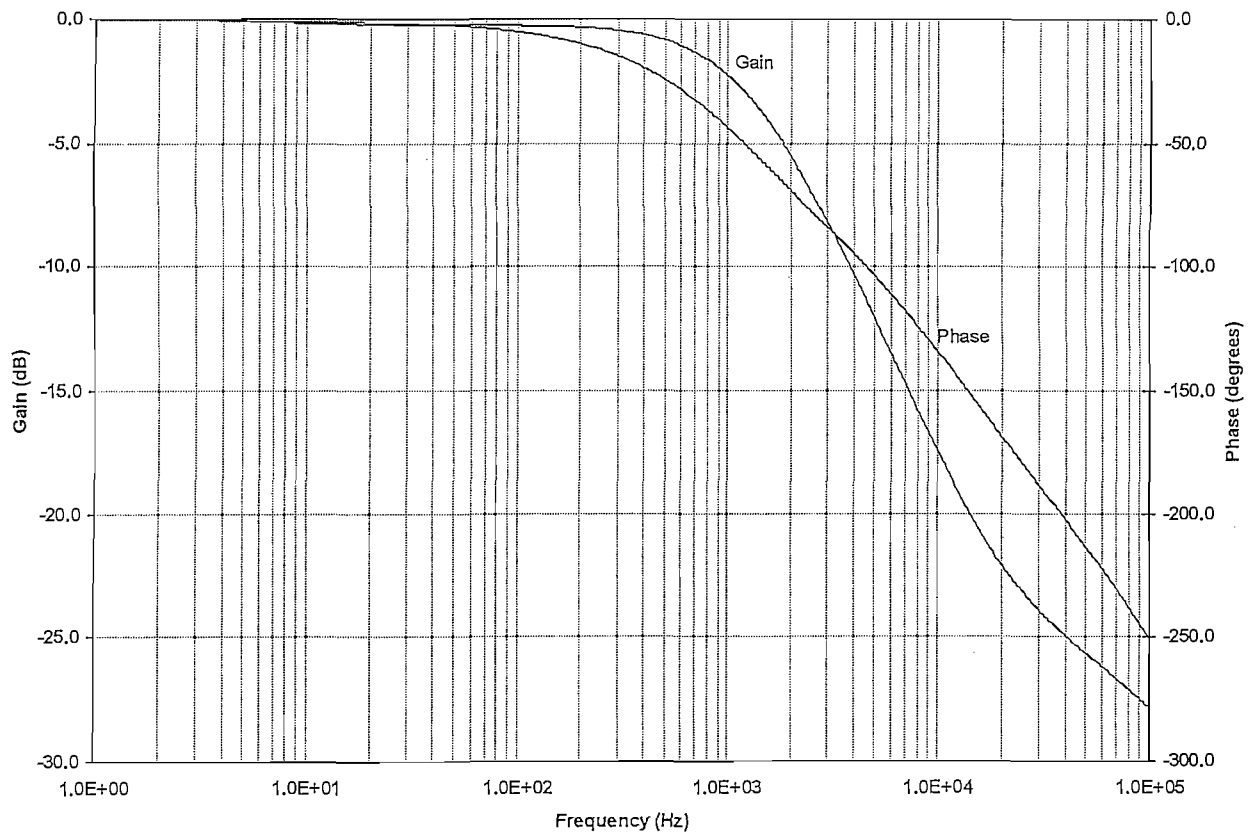


Figure 4-22 Flyback power supply closed loop transfer

From Figure 4-22, the closed loop bandwidth of the flyback power supply is 1200 Hz, slightly higher than anticipated.

4.3.2 FPGA supply

The TPS75003 power management IC from Texas Instruments supplies the FPGA 1.2 V core supply voltage V_{CCINT} , the 2.5 V auxiliary supply voltage V_{CCAUX} and the 3.3 V I/O supply voltage V_{CCO} . The FPGA has a built-in power on reset (POR) circuit therefore there is no specific voltage sequencing requirement, however the 2.5 V auxiliary supply V_{CCAUX} is enabled before the V_{CCINT} supply to minimize the FPGA start-up current. The FPGA power supply requirements are listed in Table 4-9.

Table 4-9 FPGA power supply requirements

Output	Voltage	Current
V_{CCINT}	1.2 V	3 A
V_{CCAUX}	2.5 V	0.3 A
V_{CC0}	3.3 V	3 A

The current required by the FPGA is dependant on the application size and speed. This will vary for various self-sensing algorithms so the FPGA power supply will be designed to deliver the maximum current capable by the TPS75003 power management IC. A schematic representation of the FPGA power supply is shown in Figure 4-23.

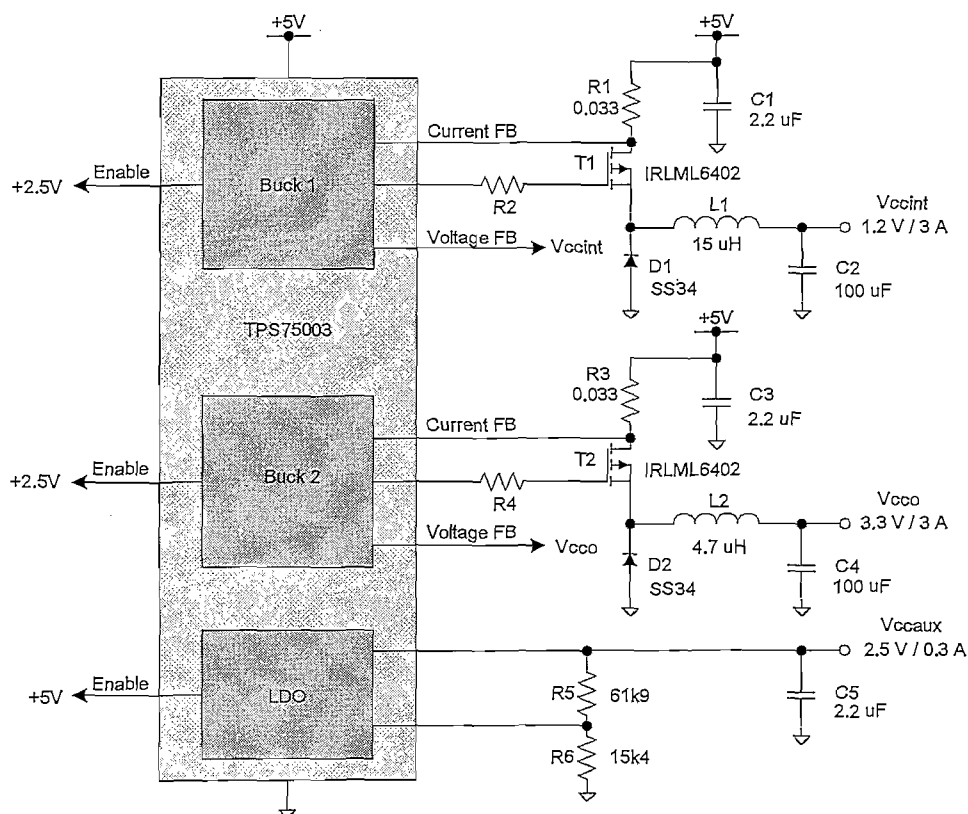


Figure 4-23 FPGA power supply

As shown in Figure 4-23 the TPS75003 consists of two 3 A buck regulators and a 0.3 A low dropout (LDO) regulator. The TPS75003 is supplied with input power from the flyback converter +5 V output. The component values shown in Figure 4-23 are determined using the data sheet for the TPS75003 power management IC [55].

The LDO dissipates 0.75 W while the two buck regulators are 94 % efficient and dissipate 0.22 W and 0.59 W respectively giving a total power dissipation of 1.56 W for the TPS75003 regulator. The TPS75003 is packaged in a 20 pin QFN package with an exposed lead frame on

the underside of the package. The exposed lead frame is used to remove heat from the component and is soldered to the PCB in accordance with the manufacturers recommendation for thermal protection.

4.3.3 DSP supply

The Texas Instruments TPS767D301 dual LDO regulator supplies the DSP with 1.8 V and 3.3 V in the correct power-up sequence. The power-up sequence requires that the 3.3 V supply be enabled prior to ramping up the 1.8 V core supply. The TPS767D301 has individual enable inputs for the 1.8 V and 3.3 V outputs. Power sequencing is implemented by permanently enabling the 3.3 V regulator and using the 3.3 V output to enable the 1.8 V regulator. The TPS767D301 is supplied with input power from the flyback converter +5 V output.

The TPS767D301 has dual active low reset signals that are used to reset the DSP based on the voltage levels of the 1.8 V and 3.3 V outputs. The reset threshold for the 1.8 V and 3.3 V outputs is 95% of the respective output voltage. The reset signals are open drain signals that are tied together through a single pull-up resistor thus forming a single active low reset signal for the DSP. During power down the DSP reset is asserted low by the TPS767D301 before the 1.8 V core supply goes below 1.5 V in order to keep the on-chip flash logic in reset.

As estimated in section 4.1.1 the DSP will require approximately 255 mA of current when operating at 150 MIPS with the 3.3 V drawing 0.09 A and the 1.8 V drawing 0.165 A. The total power dissipation for the TPS767D301 is calculated as follows

$$\begin{aligned} P_{total} &= (5 - 3.3) \cdot 0.09 + (5 - 1.8) \cdot 0.165 \text{ W} \\ &= 0.68 \text{ W} \end{aligned} \quad (4-70)$$

The TPS767D301 is packaged in a 28-pin power pad TSSOP package with a maximum junction temperature of 125 °C and a junction-to-ambient thermal resistance of 27.9 °C/W. The maximum power dissipation for the TPS767D301 at an ambient temperature of 25 °C is calculated as follows

$$\begin{aligned} P_{max} &= \frac{T_J - T_A}{R_{\Theta(JA)}} \\ &= \frac{125 - 25}{27.9} \text{ W} \\ &= 3.58 \text{ W} \end{aligned} \quad (4-71)$$

Since the total power dissipated by the TPS767D301 is less than maximum allowable power dissipation at 25 °C, the TPS767D301 power pad TSSOP package will provide adequate heat sinking.

4.4 PCB design

The integrated controller consists of three PCB assemblies namely, the power amplifier substrate, the digital controller PCB and the analog interface PCB. The analog interface PCB was designed by members of the McTronX research group and will thus not be discussed in detail, however the grounding philosophy and interconnection between the digital controller PCB and the analog interface PCB will be discussed. The integrated controller PCBs were designed in strict accordance with the IPC-2221A generic standard on printed board design.

The power amplifier, digital controller and analog interface circuitry are partitioned in order to minimize the interference between these circuits. The PCBs and power amplifier substrate are stacked on top of each other using appropriate connectors with brass pillars providing the necessary mechanical rigidity between the various PCB assemblies. The PCB stacking arrangement is shown in Figure 3-31.

4.4.1 *Power amplifier substrate*

The dual three-phase bridges consist of six identical half-bridge stages that are situated on the power amplifier substrate. Figure 4-24 shows the component layout for one half-bridge stage.

The primary objective for the power amplifier substrate layout is to minimize the loop area for the high current path in each half-bridge leg and to minimize the stray inductance between the emitter of the top IGBT and the collector of the bottom IGBT shown in Figure 4-24. This can only be accomplished by proper circuit layout and component placement.

Placing the power components as close as possible to one another is further complicated by the fact that the substrate is a single sided layout. Considering the size of the substrate and the number of half-bridge stages required, the component layout shown in figure 4-24 arguably represents the minimum loop area achievable for the high current path in each half-bridge leg.

The decoupling capacitors shown in Figure 4-24 are placed directly across the half bridge leg in order to attenuate high frequency noise that exists as a result of the connection between the IGBTs and the power supply.

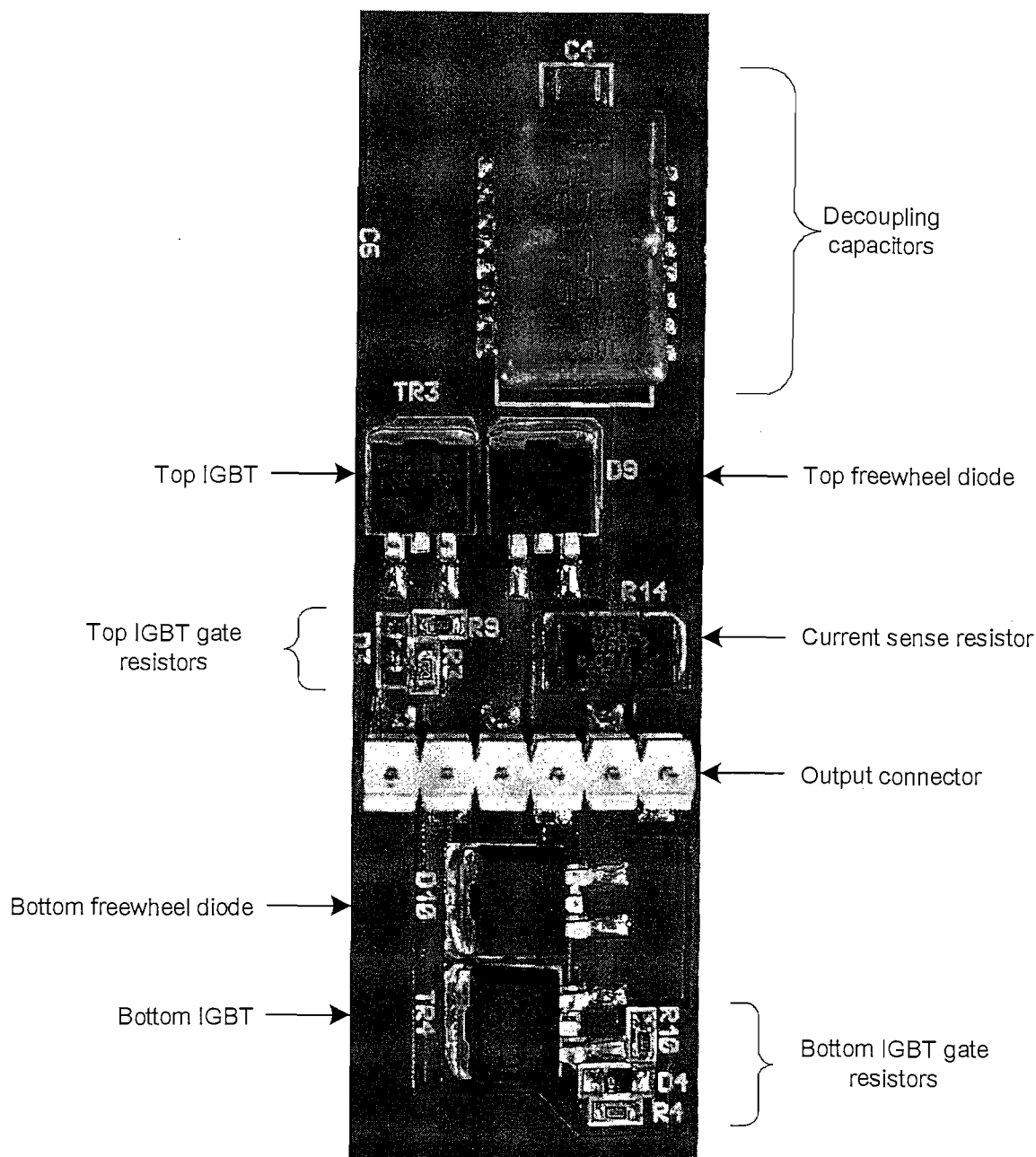


Figure 4-24 Power amplifier half-bridge stage

The power amplifier substrate is at the bottom of the PCB stack with the digital controller PCB directly above it. The connector shown in figure 4-24 is used as an interface between these assemblies.

Figure 4-25 shows the complete power amplifier substrate layout with the six half-bridge stages. The labels indicate the position of each half-bridge output and the position of the connector that supplies the +150 V to the power amplifier. These connectors form the interface between the power amplifier substrate and the digital controller PCB. The layout is symmetrical with three half-bridge stages on either side of the incoming power supply.

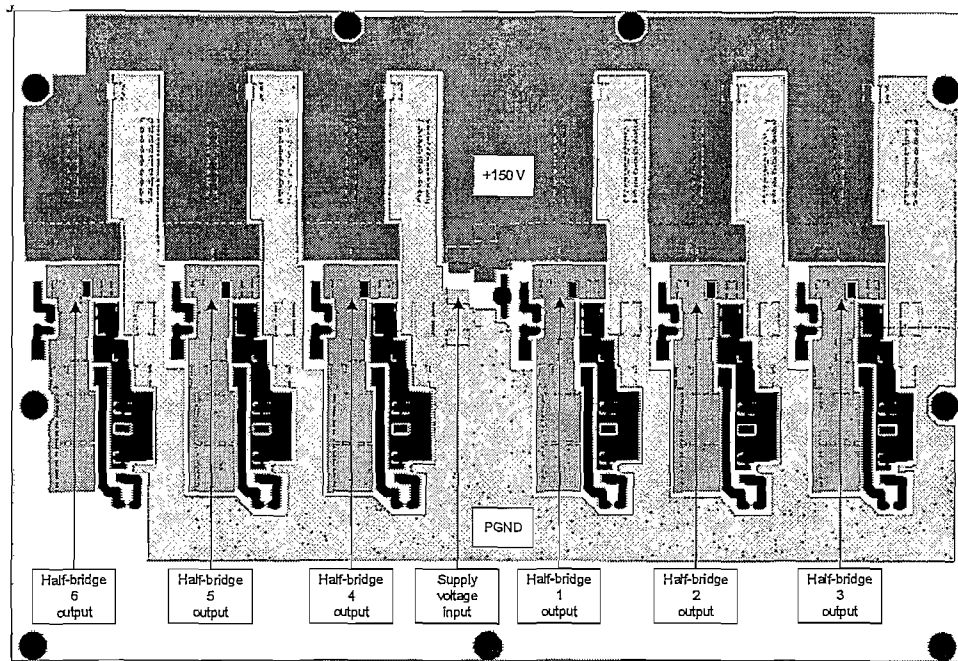


Figure 4-25 Power amplifier substrate layout

The layout shown in Figure 4-25 makes optimum use of the available copper on the substrate resulting in reduced current density of the high current path in each half-bridge leg and thus improving the thermal performance of the power amplifier.

4.4.2 Digital controller PCB

The first step in the design of the digital controller PCB is to determine the critical length of the PCB tracks for the operational characteristics of the design. This will indicate to what extent transmission line models of the PCB tracks and signal integrity simulation is necessary. Since most of the high speed signals will be routed to and from the FPGA, the I/O slew rate of the FPGA is set to slow and its output drive current is set to 8 mA. With the slew rate set to slow, the 10% to 90% rise time of the signal is approximately 1.85 ns. The length of the signal rising edge in cm is given by (4-72)

$$\begin{aligned}
 \ell_{rise} &= \frac{t_{rise}}{33.36 \cdot \sqrt{\epsilon_r}} \\
 &= \frac{1850}{33.36 \cdot \sqrt{4.5}} \text{ cm} \\
 &= 26.14 \text{ cm}
 \end{aligned} \tag{4-72}$$

where:

- t_{rise} = 10% to 90% rise time of the signal in ps
- ϵ_r = Relative permittivity of the PCB dielectric material, 4.5 for FR4.

The PCB track length of the high speed signals is limited to the conservative guideline $t_{rise}/6$ thus avoiding the use of signal integrity simulation and transmission line modeling. Using the upper limit of $t_{rise}/4$ the critical track length of the high speed signals becomes 65 mm. To comply with this requirement, the FPGA and the components that interface directly to it such as the DSP, the 30 MHz clock oscillator, the JTAG interface, the external RAM and platform flash are all placed within 65 mm of each other.

A grounding philosophy that implements a dedicated layer of solid ground plane is implemented for the digital controller PCB as shown in Figure 4-26. A solid ground plane offers the most flexibility in terms of where components may be placed since it provides the lowest possible *return path impedance for the signals and minimizes cross talk*. The solid ground plane also improves the capacitive decoupling to the power plane thus providing an effective high frequency decoupling mechanism.

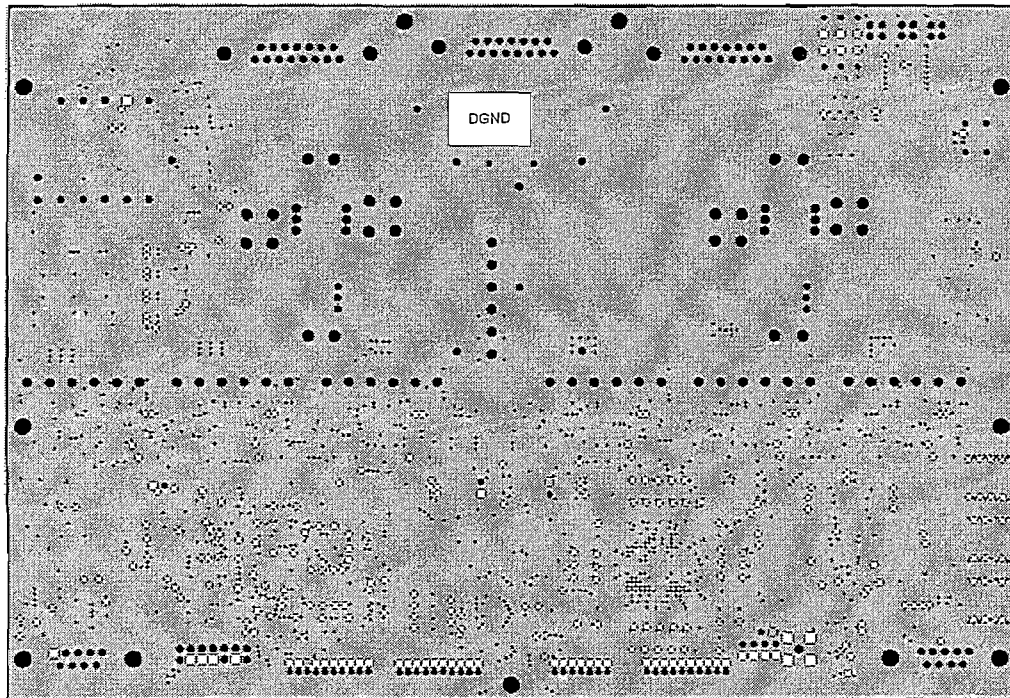


Figure 4-26 Digital controller PCB dedicated solid ground plane

A solid ground plane will also be implemented on the analog interface PCB. The most critical connection between the digital controller PCB and the analog interface PCB is the ± 12 V analog supply return, or analog ground. A common analog ground reference is established between the two PCB ground planes by means of a single inter PCB connection as shown in Figure 4-27, thus minimizing the possibility of creating unwanted ground loops. The inter PCB connection is placed as close as possible to the ADC converter on the digital controller PCB.

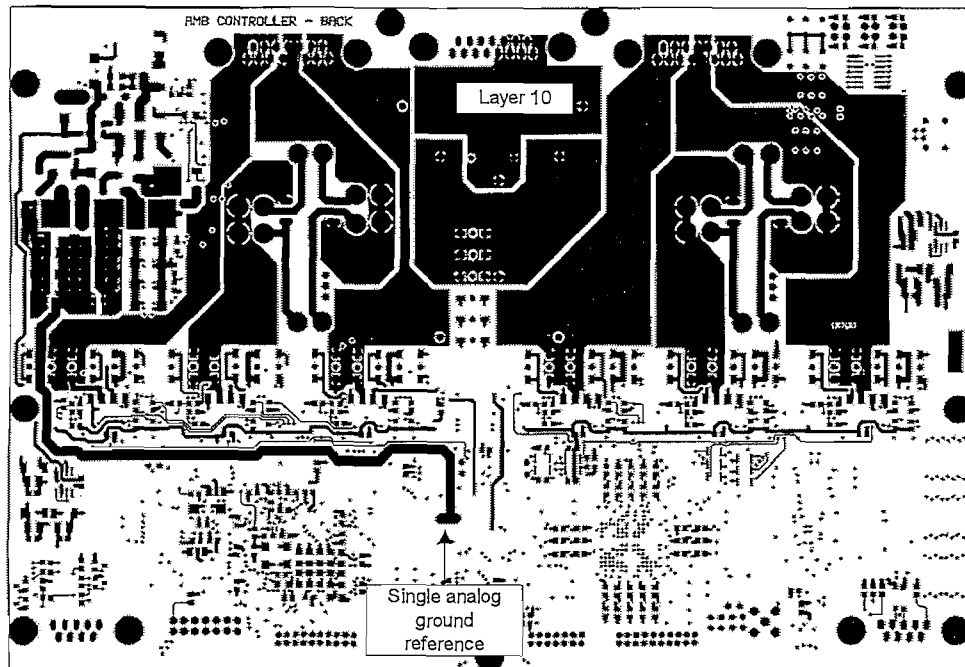


Figure 4-27 Layer 10 with single analog ground reference

The power amplifier outputs are routed via the digital controller PCB and thus require special attention from a PCB layout perspective. These high current tracks are physically separated from the signal tracks on the digital controller PCB by dividing the PCB into two areas, one area for the digital controller signals and the other area for the power amplifier output signals as shown in Figure 4-28 and Figure 4-29.

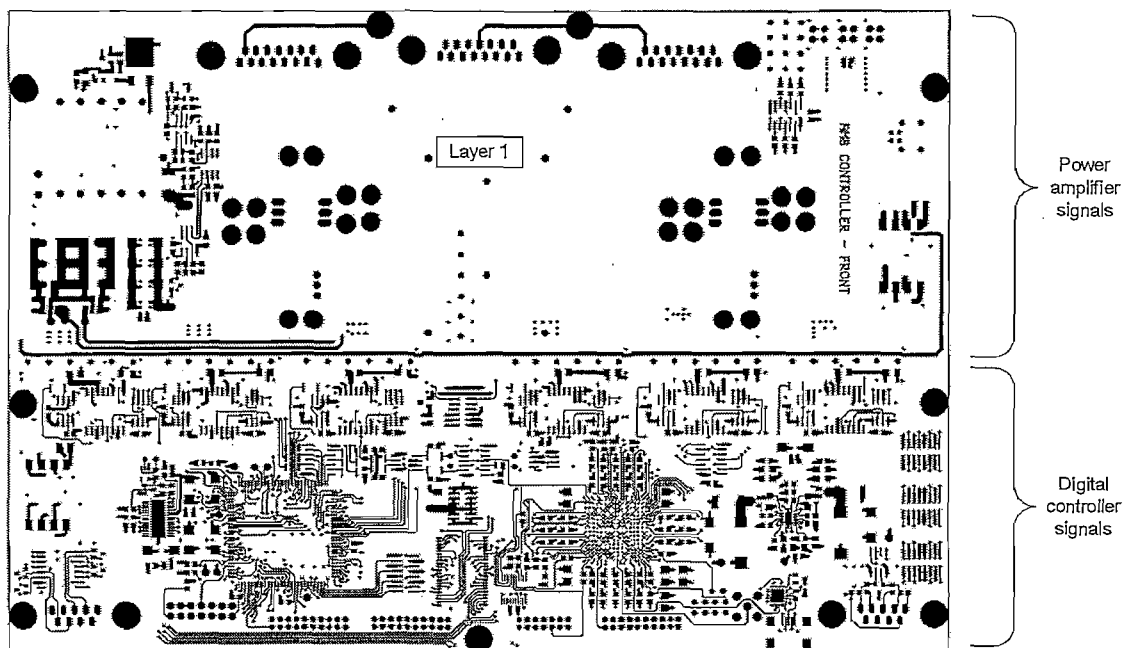


Figure 4-28 Digital controller PCB layout, layer 1

A comparison of Figure 2-28 and Figure 4-29 clearly shows the two separate areas for the power amplifier signals and the digital controller signals on layer 1 and layer 9.

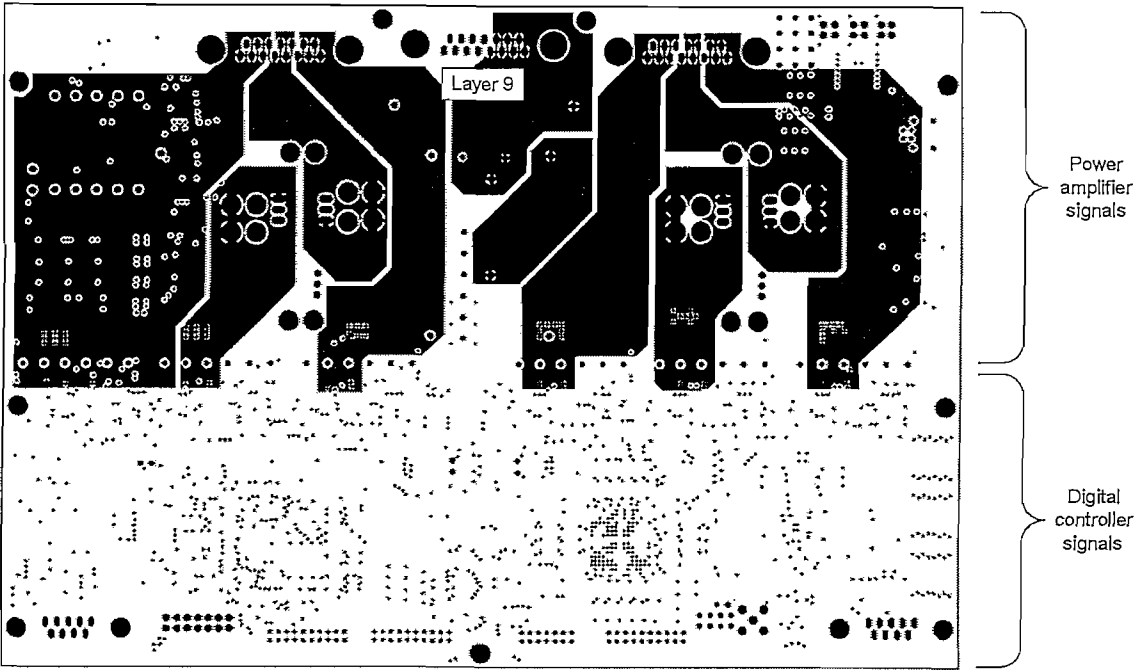


Figure 4-29 Digital controller PCB layout, layer 9

Although not shown, layer 2 and layer 3 also contain only digital controller signals. Similarly layer 8 and layer 9 only contain power amplifier signals. A dedicated layer of solid ground plane is also implemented for the power amplifier ground.

The size of the BGA package plays a major role in determining the number of layers required to route the PCB effectively. The FPGA is packaged in a 256-ball fine pitch ball grid array package. Applying the BGA design rule shown in Figure 2-15 to the 256-ball fine pitch ball grid array package, a minimum of four PCB layers are used to route the FPGA. Additional layers are added for routing the solid ground plane, the power supply and power amplifier signals, resulting in a final layer count of ten for the digital controller PCB. The layer structure of the digital controller PCB is given in Table 4-10.

Table 4-10 Digital controller PCB layer structure

Layer number	Layer type
1	Digital controller signals
2	Digital controller signals
3	Digital controller signals
4	Split power plane
5	Digital controller ground plane
6	Power amplifier ground plane
7	Power amplifier signals
8	Power amplifier signals

9	Power amplifier signals
10	Digital controller and power amplifier signals

A single PCB layer is allocated as a dedicated split power plane for the digital controller PCB. The split power plain accommodates the +5 V, +3.3 V and +1.8 V supplies for the DSP and the +1.2 V, +2.5 V and +3.3 V supplies for the FPGA. The dedicated split power plane is shown in Figure 4-30. As shown in Table 4-10, the split power plane and the digital controller ground plane are placed next to each other in the layer structure to minimize the distance between them and thus increase the effective power plane decoupling.

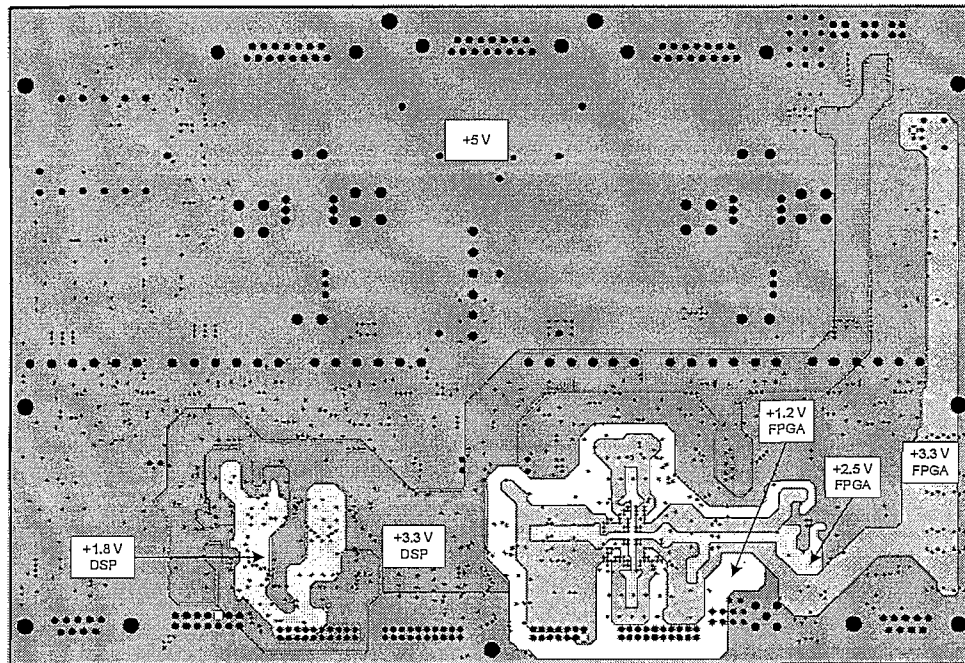


Figure 4-30 Digital controller PCB dedicated split power plane

4.5 Conclusion

In Chapter 4 a detail design was proposed for the power amplifier, digital controller and electronic supply. Component selection, thermal considerations and PCB design were covered in detail. A complete set of circuit diagrams for the integrated controller design is available in the Appendix of this document. In Chapter 5 the integrated controller design will be verified according to certain measured circuit parameters as well as its performance in a self-sensing experimental setup.

Chapter 5

Design verification

In Chapter 5 the performance of the integrated co-processor based power electronic drive is evaluated in terms of hardware measurements and system performance. The hardware measurements are taken from an integrated co-processor based power electronic drive in a 1 DOF self-sensing experimental setup. The self-sensing system performance obtained with the integrated co-processor based power electronic drive is briefly presented.

5.1 Hardware evaluation

The intended purpose of the integrated co-processor based power electronic drive is to provide a hardware platform to facilitate the research of various self-sensing techniques for AMBs. The hardware evaluation of the integrated co-processor based power electronic drive is thus based on measurements taken from a 1 DOF self-sensing experimental setup. Figure 5-1 shows the integrated drive with the power amplifier substrate at the bottom of the assembly, the digital controller PCB in the middle and the analog interface PCB at the top of the assembly.

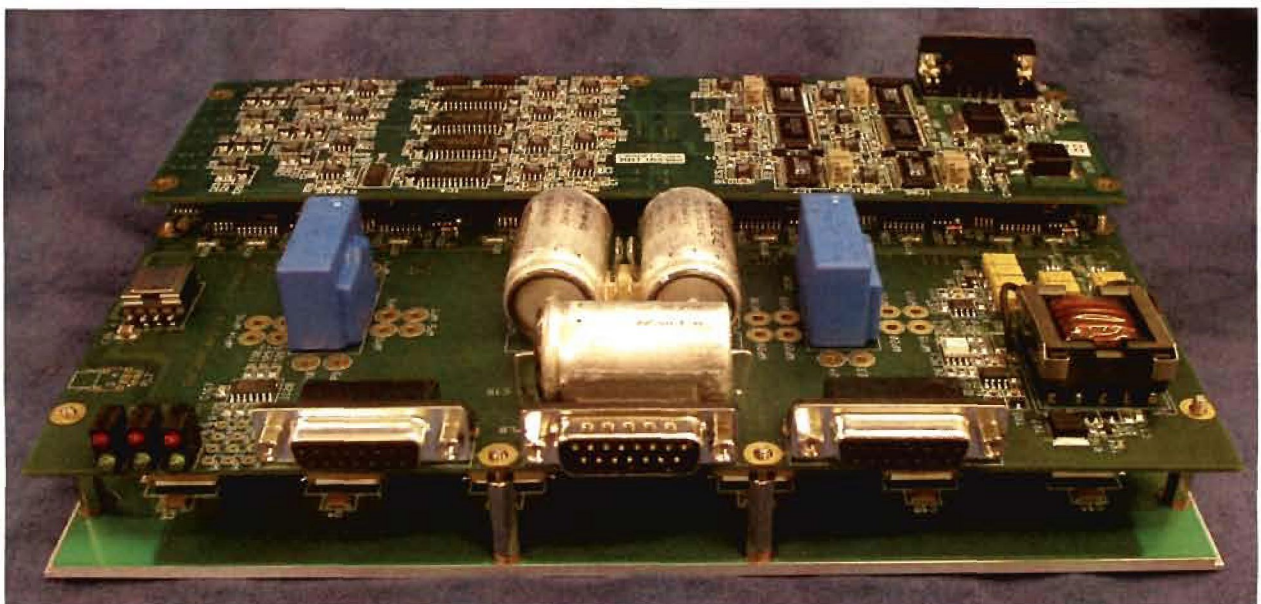


Figure 5-1 Integrated co-processor based power electronic drive

Appendix A of this document contains the detail schematic diagram of the digital controller circuitry and Appendix B contains the detail schematic diagram of the power amplifier. Throughout this Chapter where reference is made to a specific component by number, that component may be traced in the relevant Appendix.

The power amplifier, digital circuitry and electronic supply will be evaluated individually in the subsequent sections. The analog interface PCB was designed by members of the McTronX research group and will thus not form part of this hardware evaluation.

5.1.1 Power amplifier

The hardware evaluation of the power amplifier will be partitioned according to gate drive, floating supply, protection circuitry, sense circuitry, power circuit and amplifier bandwidth. The thermal performance of the power amplifier will be addressed where applicable. The power amplifier substrate assembly is shown in Figure 5-2.

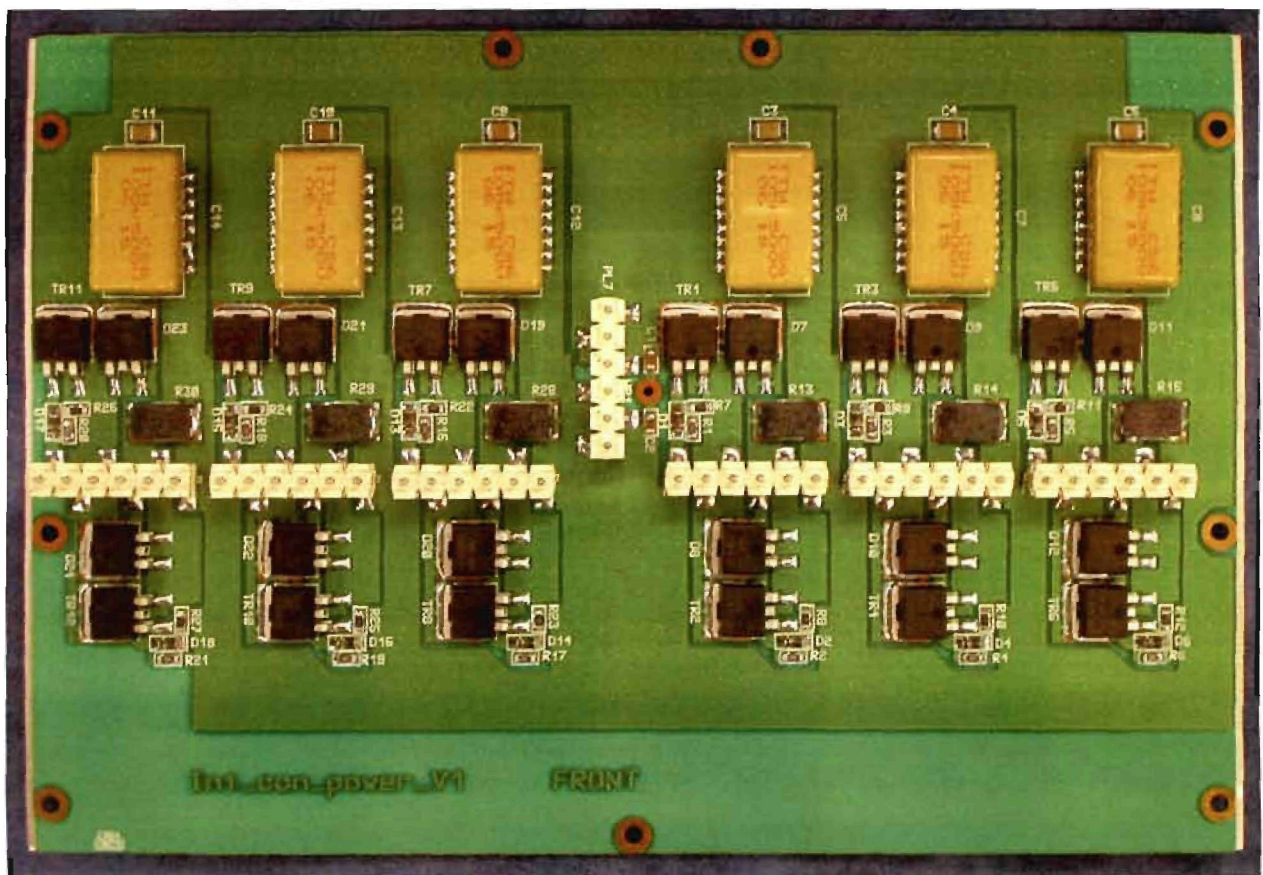


Figure 5-2 Power amplifier substrate assembly

The power amplifier is configured as two modified H-bridges in order to drive the 1 DOF AMB. One modified H-bridge is formed by combining TR2, TR3, D7 and D10. The other modified H-

bridge is formed by combining *TR8*, *TR9*, *D19* and *D22*. The measurements are made with a Le Croy model 424 Wave Surfer oscilloscope.

Gate drive

The IR2113 integrated gate drive IC inputs are TTL compatible and thus connected directly to the open collector output of the isolation circuitry opto-coupler. The input signal to pin 12 of the IR2113 *IC20* is shown in Figure 5-3.

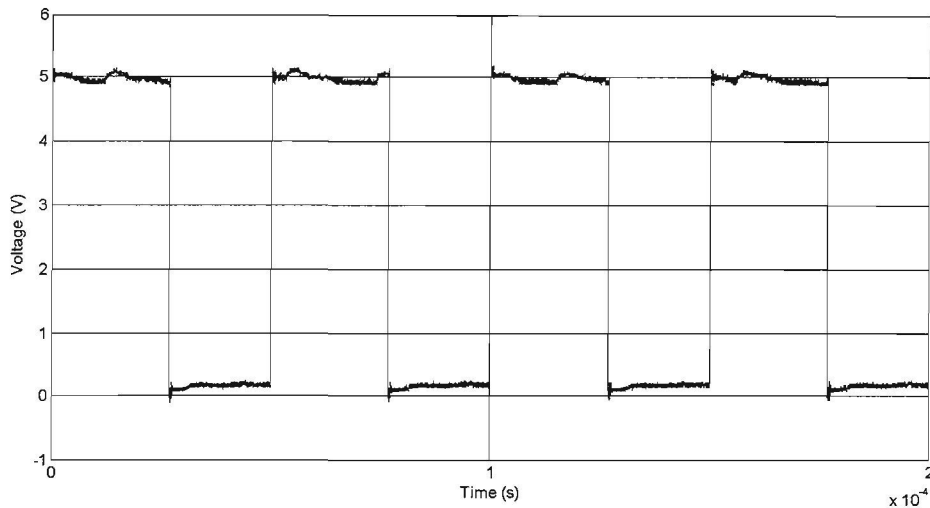


Figure 5-3 IR2113 input signal

IC20 drives the upper IGBT *TR9* with a level shifted gate drive signal that is referenced to its emitter. The upper IGBT gate drive signal is approximately 15 V higher than its collector potential that is connected directly to the 50 V DC supply voltage. The gate drive signal of the upper IGBT, *TR9* is shown in Figure 5-4, measured at pin 8 of *IC20* with respect to the H-bridge supply return, PGND.

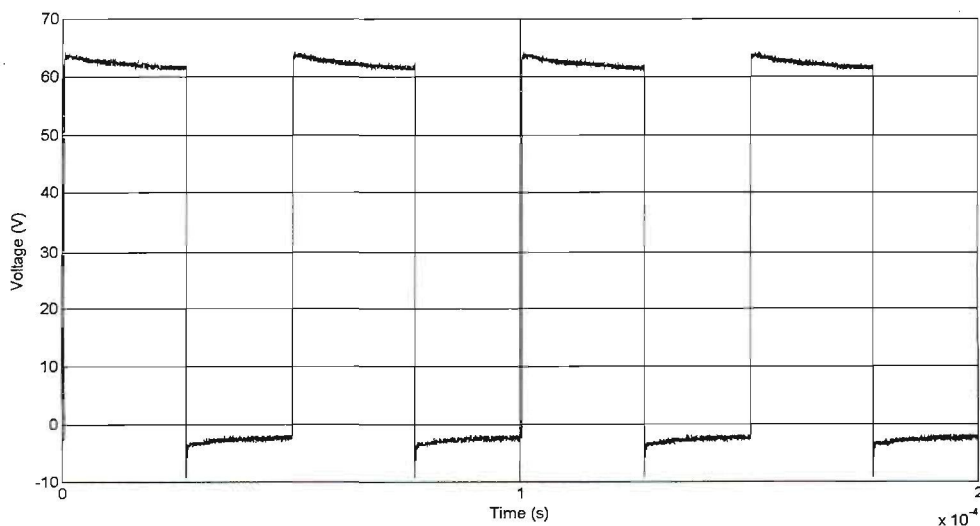


Figure 5-4 Upper IGBT gate drive signal

Floating supply

The IR2113 gate driver *IC20* requires a floating supply of approximately 15 V in order to drive the upper IGBT *TR9*. The DC output voltage of the floating supply *V5* that supplies *IC20* is shown in Figure 5-5. The floating supply voltage *V5* is measured at pin 7 of *IC20* with respect to pin 6 of *IC20*.

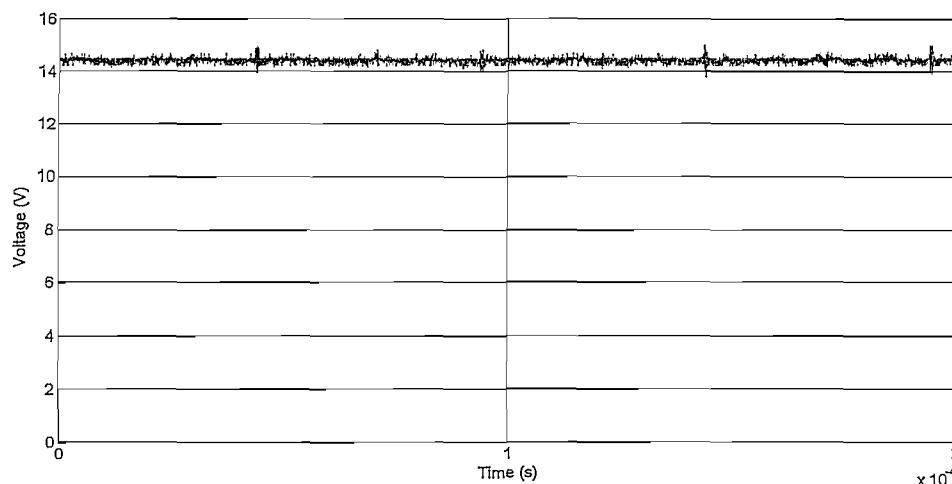


Figure 5-5 Floating supply voltage

The floating supply transformer will experience a temperature rise as a result of power loss. The temperature of the floating supply transformer *T2* was measured while the system was operational and found to stabilize at 44 °C. Since the measurements were made at a room temperature of 25 °C, this represents a temperature rise of 19 °C for the floating supply transformer due to power loss. A temperature rise of approximately 20 °C above ambient is acceptable for a transformer such as this.

Protection circuitry

Over temperature protection is provided by the DS18S20 digital thermometer. Since this device only measures temperature its performance will not be discussed here.

The pulse-for-pulse current limit is a critical function that protects the power amplifier during short circuit conditions. The pulse-for-pulse current limit occurs at the rate of the PWM switching frequency and is implemented via the IR2113 integrated gate drive IC shutdown pin. Figure 5-6 shows the shutdown signal at pin 13 pin of *IC 11* an IR2113 integrated gate drive IC while the output of the modified H-bridge formed by *TR2*, *TR3*, *D7* and *D10* is short circuited.

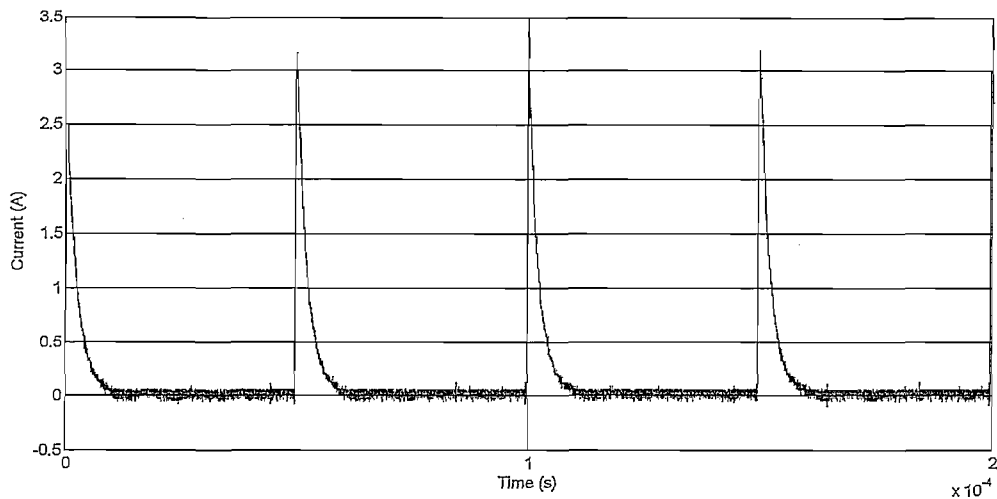


Figure 5-6 Shutdown pin with the output short circuited

The short circuit current is measured with a current clamp and shown in Figure 5-7. The peak current limit scaling is set for 15 A however the short circuit current reaches a peak of 30 A with the supply voltage at 50 V. This is due to the inevitable delay through the current limit comparator and the delay associated with the shutdown pin of the IR2113. The current limit scaling is adjustable and can thus be adapted to make provision for this delay.

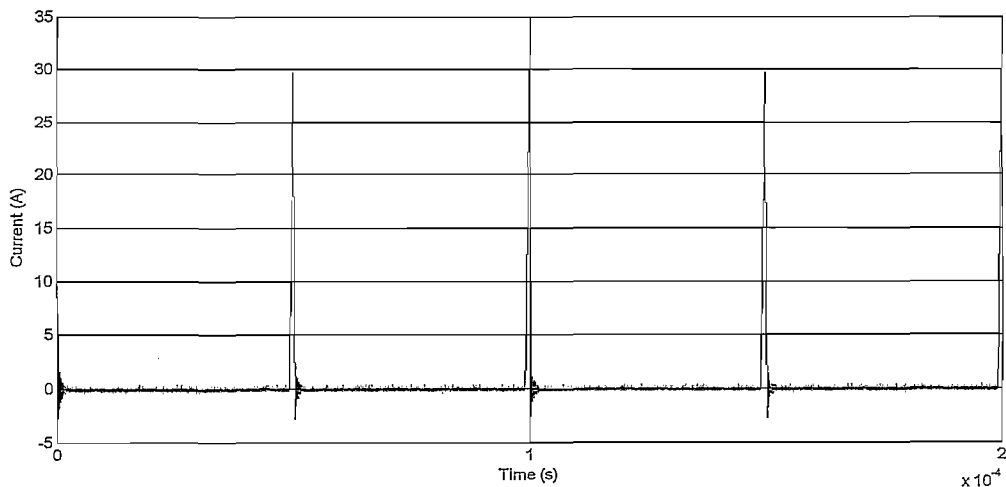


Figure 5-7 Power amplifier short circuit current

Sense circuitry

The LAH 25-NP current transducer is used to measure the AMB coil current. The current transducer has a bandwidth of 200 kHz that assists in removing high frequency noise from the measured current while preserving the current information required for self-sensing purposes. The coil current as measured by the current transducer *IC15* is shown in Figure 5-8. The current measurement in Figure 5-8 is AC coupled and representative of the AMB rotor centre position.

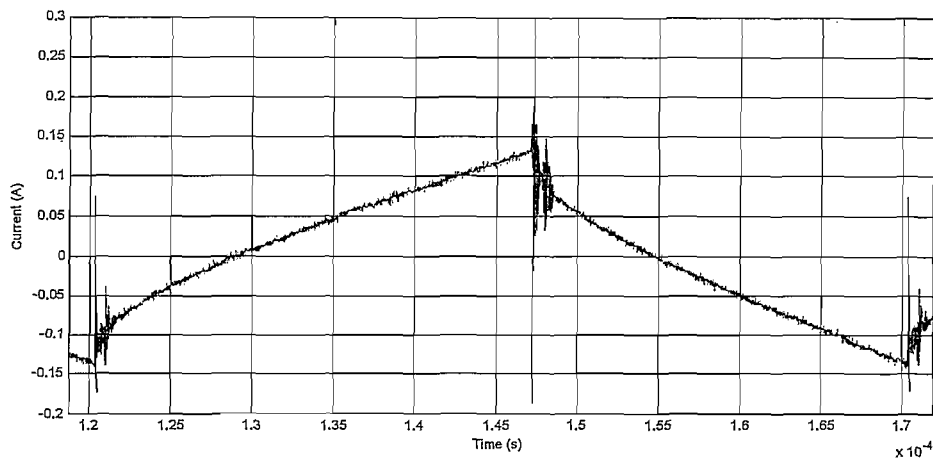


Figure 5-8 LAH 25-NP current transducer output

A voltage divider, configured from discrete resistors, is used to attenuate the AMB coil voltage to an acceptable level before being measured by the analog interface circuitry. The sense voltage from the divider output formed by $R77$ and $R78$ is shown in Figure 5-9.

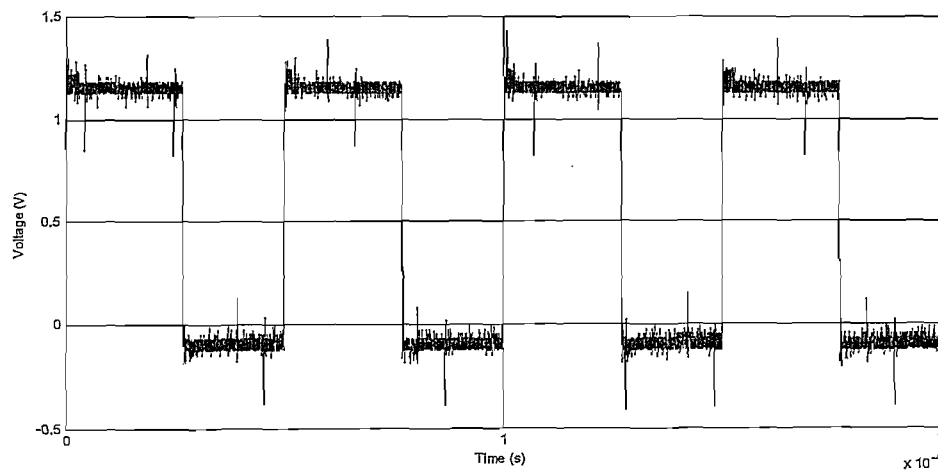


Figure 5-9 Voltage sense output

Although the sensed current and voltage signals contain switching noise, these signals are filtered in the self-sensing algorithm before the rotor position information is extracted.

Power circuit

The modified H-bridge output voltage is shown in Figure 5-10 for a supply voltage of 50 V with the duty cycle at 53.8%. The output voltage is measured differentially between the emitter of $TR9$ and the collector of $TR8$. The output voltage is +50 V when the IGBTs $TR8$ and $TR9$ are switched on. When the IGBTs are switched off the freewheel diodes $D19$ and $D22$ conduct allowing the output voltage to reverse to -50 V.

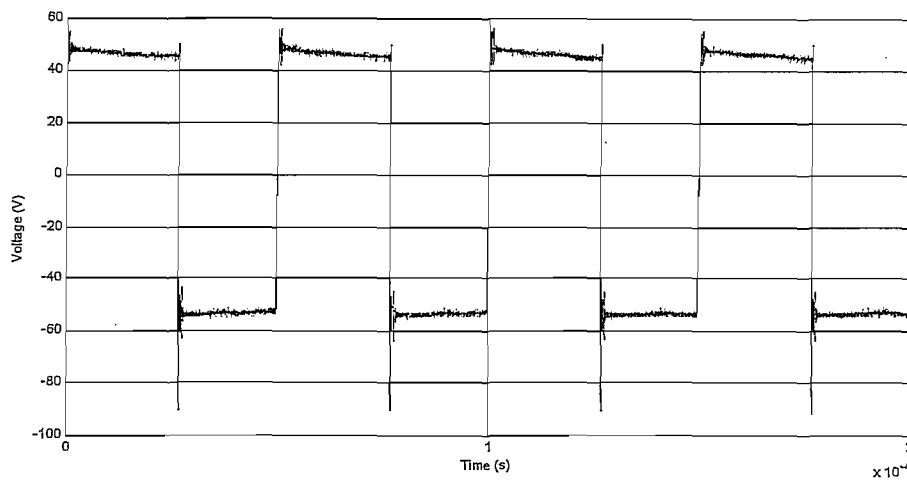


Figure 5-10 Modified H-bridge output voltage

The modified H-bridge load current for a duty cycle of 53.8% is 2.9 A. The DC coupled load current measurement is shown in Figure 5-11. The DC level of 2.9 A represents the bias current required to suspend the AMB rotor at the centre position while the slope and amplitude of the ripple current component is determined by the electromagnet characteristics and the position of the rotor.

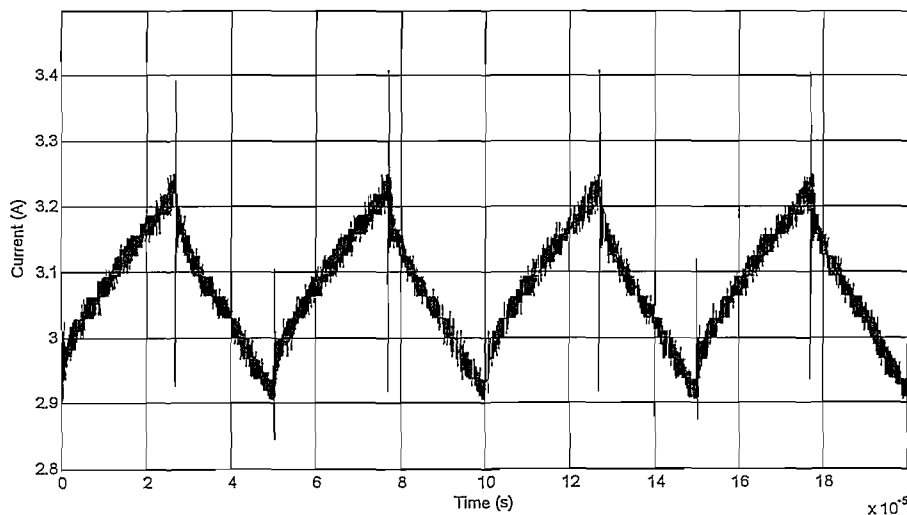


Figure 5-11 Modified H-bridge load current

The thermal performance of the power amplifier is quantified by operating both modified H-bridges at the nominal load current of 7.5 A and measuring the temperature rise of the components once thermal equilibrium is reached. Thermal equilibrium was reached after approximately 15 minutes of operation. The measurements were made at a room temperature of 25 °C without forced air cooling. The additional heat sink referred to in section 3.6 was not attached to the power amplifier substrate during this evaluation. The results of the temperature measurements are listed in Table 5-1.

Table 5-1 Power amplifier thermal measurements

Component	Measured temperature	Temperature rise above ambient
IGBT, TR3	78 °C	53 °C
Diode, D10	75 °C	50 °C
Sense resistor, R13	81 °C	56 °C
Capacitor, C7	66 °C	41 °C
Substrate	81 °C	56 °C

The measured results from Table 5-1 are well within the thermal limit, as calculated in section 4.2.2, for the IGBT, diode and sense resistor. The substrate temperature rise is approximately 13.4 °C higher than the value of 67.6 °C calculated in section 4.2.2. This may be due to the actual switching loss of the IGBT being higher than the calculated value since the calculated switching loss is based on an ideal freewheel diode. In reality when the IGBT switches on, it dissipates the reverse recovery charge from the freewheel diode. Once the additional heat sink is attached to the power amplifier substrate the thermal capacity of the system will increase.

Amplifier small signal bandwidth

In order to suspend the 1 DOF AMB, a current loop is closed around the power amplifier. The current loop is implemented in the digital controller. The small signal bandwidth of the power amplifier is measured by applying a sinusoidal current reference to the controller. The sinusoidal reference is swept in frequency from 100 Hz to 2500 Hz. The reference current and the measured current are stored in memory for each measurement point in the frequency sweep. The amplitude of the reference current must be chosen small enough to ensure that the power bandwidth of the power amplifier does not influence the small signal measurement. This criteria is given by (5-1) which is used to calculate the reference current amplitude for the Bode plot.

$$\begin{aligned}
 I_{ref} &\leq \frac{V}{2 \cdot \pi \cdot f \cdot L} \text{ A} \\
 &\leq \frac{50}{2 \cdot \pi \cdot 2500 \cdot 7.2 \times 10^{-3}} \text{ A} \\
 &\leq 0.44 \text{ A}
 \end{aligned}
 \tag{5-1}$$

where:

- V = amplifier supply voltage in V
- f = maximum frequency of the reference current in Hz
- L = inductance of the coil in H.

The current amplitude given by (5-1) is the RMS current therefore the peak to peak current reference is 1.25 A. The captured data is used to generate the Bode plot of the closed loop response shown in Figure 5-12. As can be seen from Figure 5-12, the small signal bandwidth of the power amplifier current loop is 1780 Hz while the -90 degree phase shift occurs at 900 Hz. A +5 dB resonant peak occurs at 900 Hz.

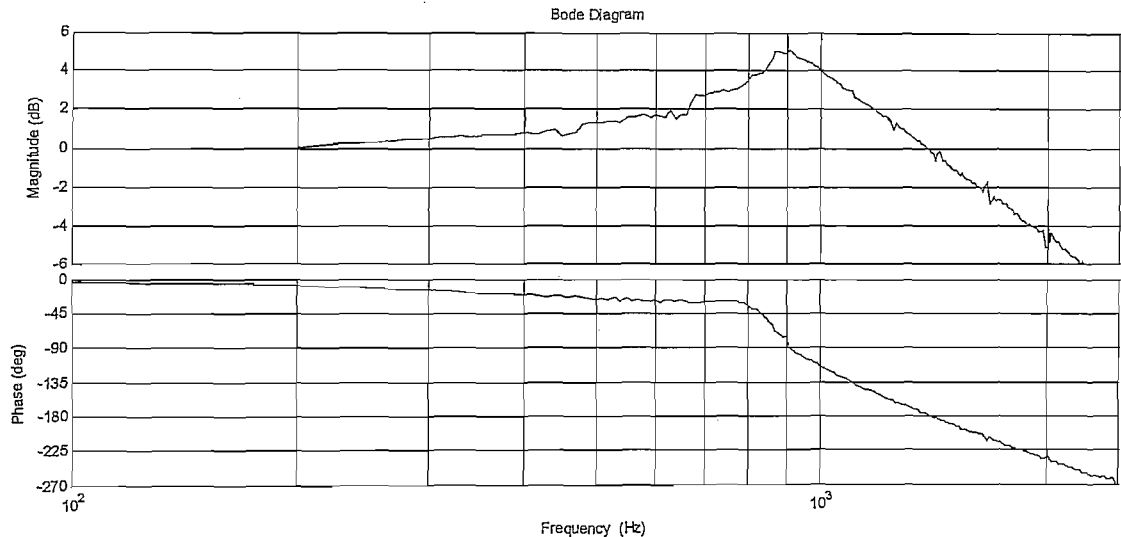


Figure 5-12 Power amplifier current loop small signal response

The bandwidth of the current loop is below the theoretically predicted 2500 Hz. This may be due to the inductance and resistance of the electromagnetic coil differing from the values used to calculate the current loop compensator. The amplitude of the reference current signal used to measure the small signal bandwidth may be too large.

5.1.2 Electronic supply

The hardware evaluation of the electronic supply will consider the flyback converter, the FPGA power supply and the DSP power supply individually. The DC voltage output of each supply and the AC ripple component of each supply output are evaluated. Since the power supply load can't be manually adjusted, it is impractical to measure performance parameters such as transient response and load regulation in the assembled hardware. The power supply load condition is determined by the hardware it supplies and will thus be considered as the nominal load condition for the purpose of this evaluation.

Flyback converter

The flyback power supply has been designed to operate in discontinuous mode across the input voltage range at the nominal load determined by the hardware with the worst case condition being minimum input voltage. Figure 5-13 shows the primary switching waveform of the flyback

converter measured at 50 V, the minimum input voltage. The measurement is made at the drain of the flyback power MOSFET switch, *TR8* with respect to the input supply return PGND. From Figure 5-13 the switch on-time is 4.5 μs and the switching period is 20.4 μs . This equates to a duty cycle of 22.1 % that indicates that the flyback power supply is operating in discontinuous mode at minimum input voltage.

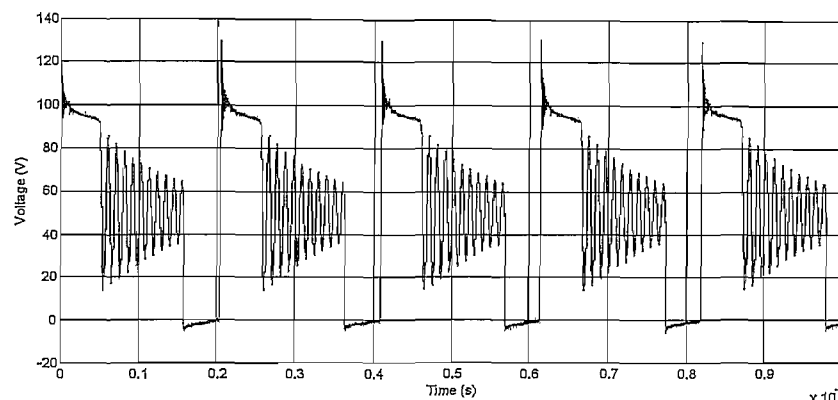


Figure 5-13 Flyback power supply primary switching voltage

The primary current switching waveform of the flyback power supply, while operating in discontinuous mode at minimum input voltage is shown in Figure 5-14. This measurement is made at pin 3 with respect to pin 5 of *IC2*, the flyback power supply PWM controller IC. The scale factor for the current measurement in Figure 5-14 is 0.27 V/A that translates to a peak current of 1.22 A.

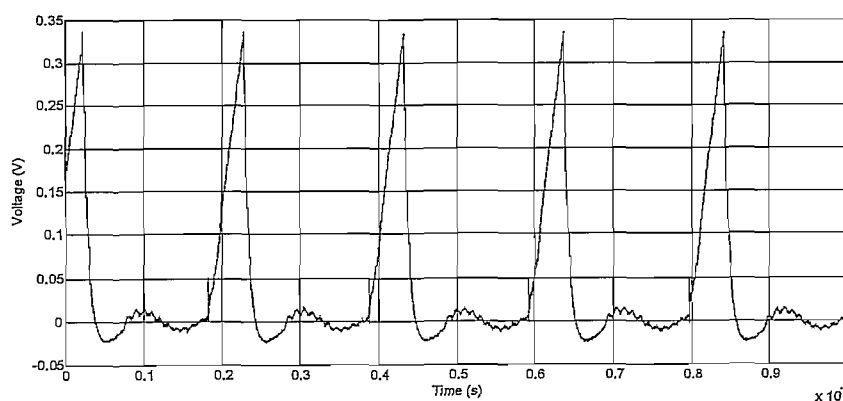


Figure 5-14 Flyback primary switching current

The DC output voltage of the +5 V output of the flyback power supply is shown in Figure 5-15. This is the controlled output and as expected measures exactly +5 V.

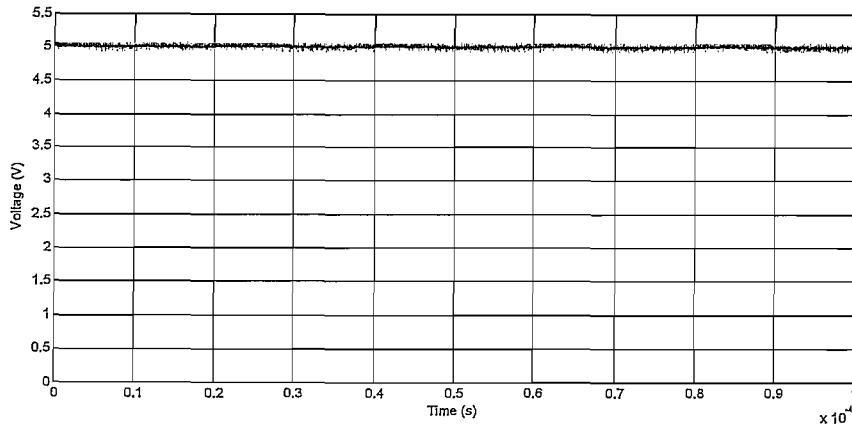


Figure 5-15 Flyback +5 V output voltage

The AC ripple component of the +5 V supply output is shown in Figure 5-16. The peak to peak ripple voltage is approximately 33 mV at the nominal load, 0.66% of the output voltage.

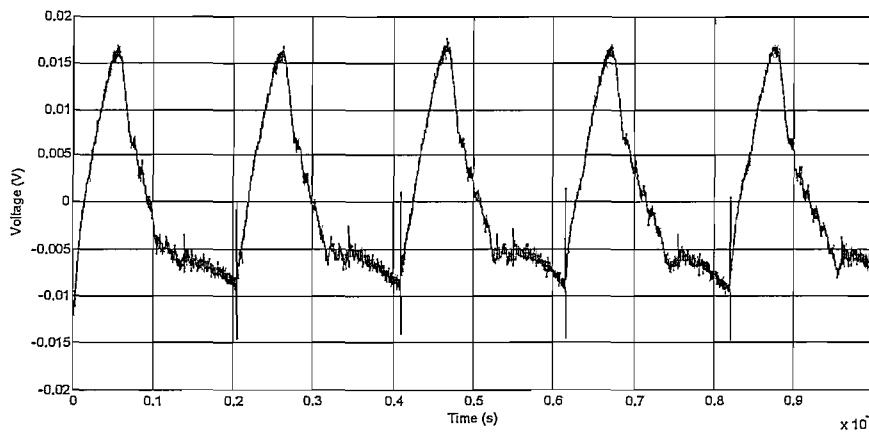


Figure 5-16 Flyback +5 V output voltage ripple

The DC output voltages of the ± 12 V_A outputs of the flyback power supply are shown in Figure 5-17. Although these outputs rely on the cross coupling between the transformer secondary windings and turns ratio for output voltage regulation, they are extremely accurate with the positive output measuring +12.10 V and the negative output measuring -12.15 V.

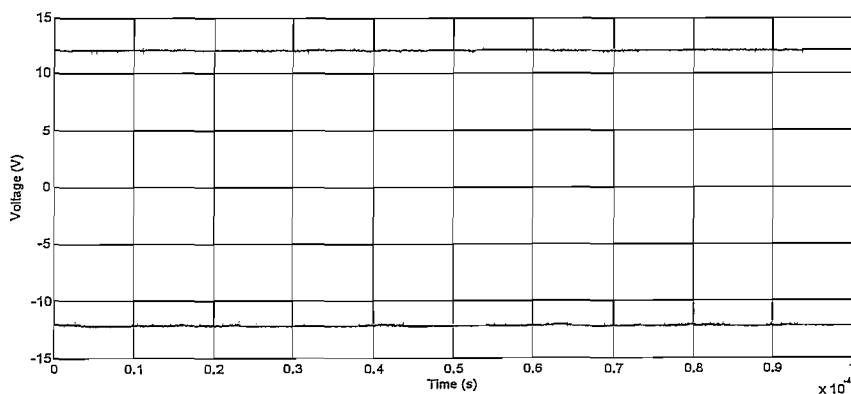


Figure 5-17 Flyback +/- 12 V_A output voltages

The AC ripple component of the +12 V_A supply output is shown in Figure 5-18.

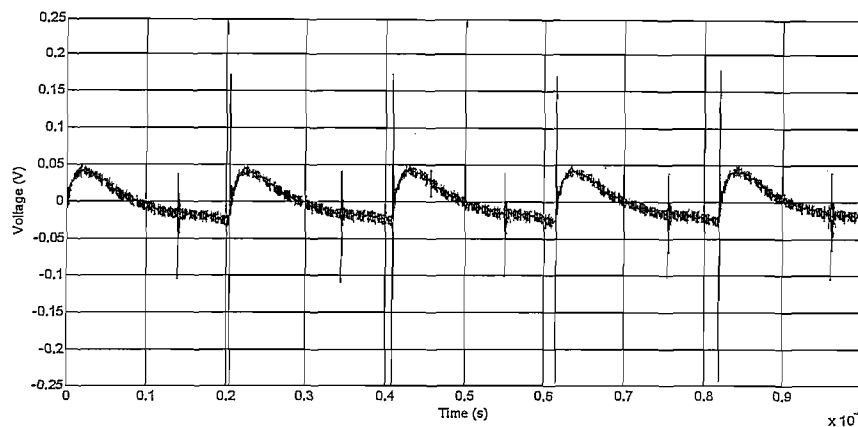


Figure 5-18 Flyback +12 V output voltage ripple

The peak to peak ripple voltage, including the common mode spike, is approximately 0.4 V. The AC ripple component of the -12 V_A supply output is shown in Figure 5-19. The peak to peak ripple voltage, including the common mode spike, is approximately 0.4 V.

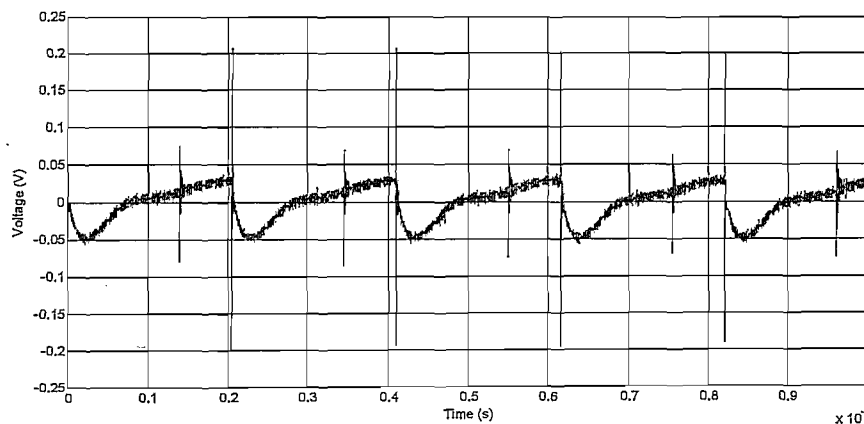


Figure 5-19 Flyback -12 V_A output voltage ripple

The remaining outputs of the flyback power supply are not included in this evaluation since their load currents are an order size smaller than those of the +5 V and ± 12 V_A outputs. The flyback power transformer will experience a temperature rise as a result of power loss. The temperature of T1, the flyback power transformer, was measured while the system was operational and found to stabilize at 48 °C. Since the measurements were made at a room temperature of 25 °C, this represents a temperature rise of 23 °C for the flyback supply transformer due to power loss. This correlates well with the predicted temperature rise of 20 °C for copper loss with an additional temperature rise of 3 °C due to core loss.

FPGA power supply

The TPS75003 power management IC from Texas Instruments supplies the FPGA 1.2 V core supply voltage V_{CCINT} , the 2.5 V auxiliary supply voltage V_{CCAUX} and the 3.3 V I/O supply voltage V_{CCO} . The 1.2 V core supply voltage and the 3.3 V I/O supply voltage are each regulated by a 3

A buck regulator while the 2.5 V auxiliary supply voltage is regulated by a 0.3 A low dropout (LDO) regulator. The FPGA power supply is supplied with input power from the flyback converter +5 V output. The DC output voltage of the +1.2 V core supply voltage of the FPGA power supply is shown in Figure 5-20 and measures +1.28 V.

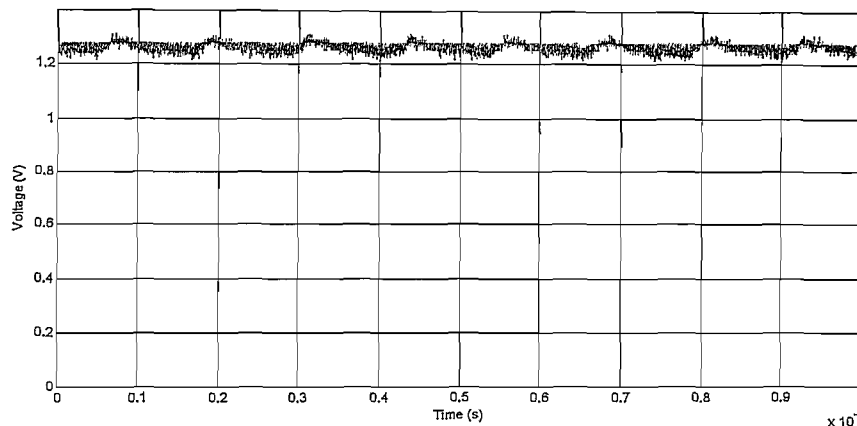


Figure 5-20 FPGA 1.2 V core supply voltage

The AC ripple component of the +1.2 V core supply voltage output is shown in Figure 5-21. The peak to peak ripple voltage is approximately 35 mV.

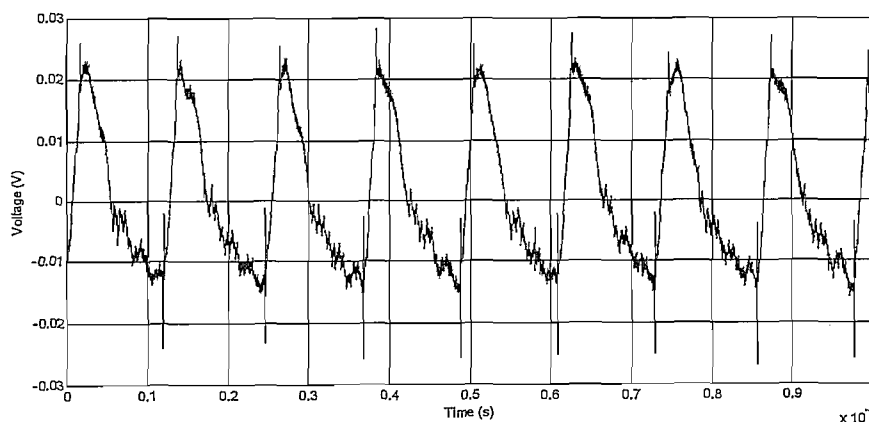


Figure 5-21 FPGA 1.2 V core supply voltage ripple

According to the manufacturers data for the FPGA the minimum limit for the +1.2 V core supply is +1.14 V while the absolute maximum limit, including the ripple voltage component, is +1.32 V. The +1.2 V core supply voltage of the FPGA power supply is thus well within these limits. The DC output voltage of the +2.5 V auxiliary supply voltage of the FPGA power supply is shown in Figure 5-22 and measures +2.6 V.

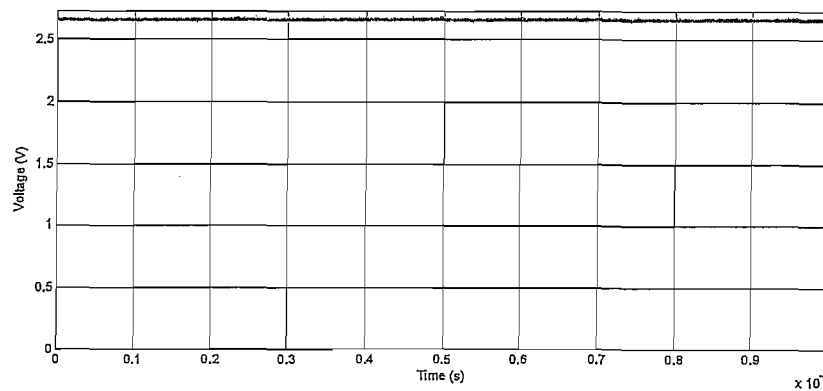


Figure 5-22 FPGA 2.5 V auxiliary supply voltage

The AC ripple component of the +2.5 V auxiliary supply voltage output is shown in Figure 5-23. The peak to peak ripple voltage is approximately 6 mV.

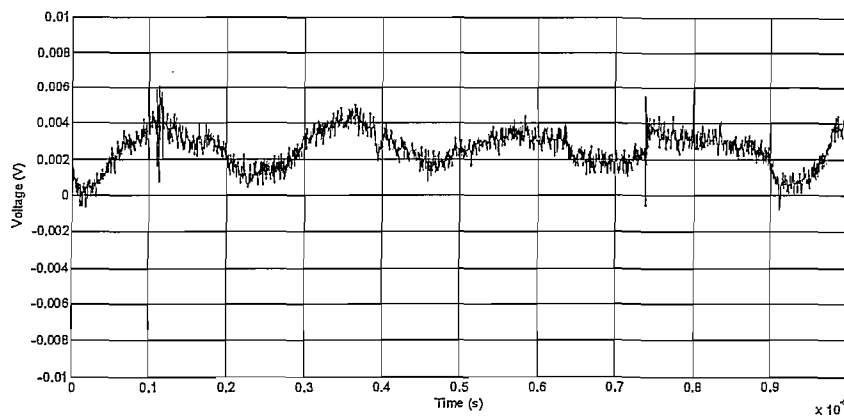


Figure 5-23 FPGA 2.5 V auxiliary supply voltage ripple

According to the manufacturers data for the FPGA the minimum limit for the +2.5 V auxiliary supply is +2.375 V while the absolute maximum limit, including the ripple voltage component, is +3.0 V. The +2.5 V auxiliary supply voltage of the FPGA power supply is thus well within these limits. The DC output voltage of the +3.3 V I/O supply voltage of the FPGA power supply is shown in Figure 5-24 and measures +3.4 V.

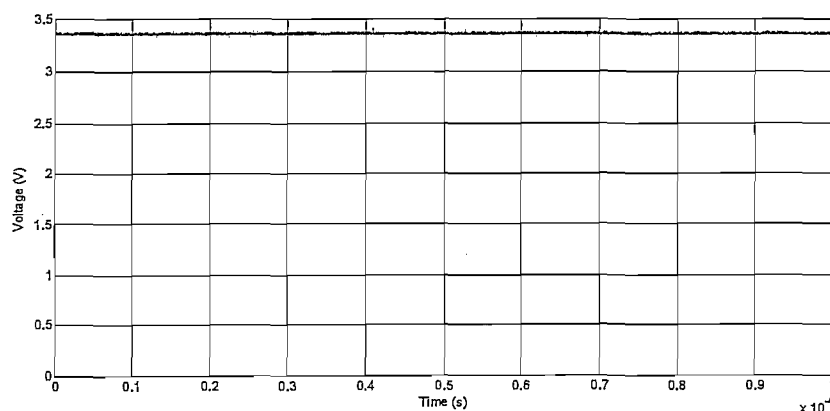


Figure 5-24 FPGA 3.3 V I/O supply voltage

The AC ripple component of the +3.3 V I/O supply voltage output is shown in Figure 5-25. The peak to peak ripple voltage is approximately 40 mV.

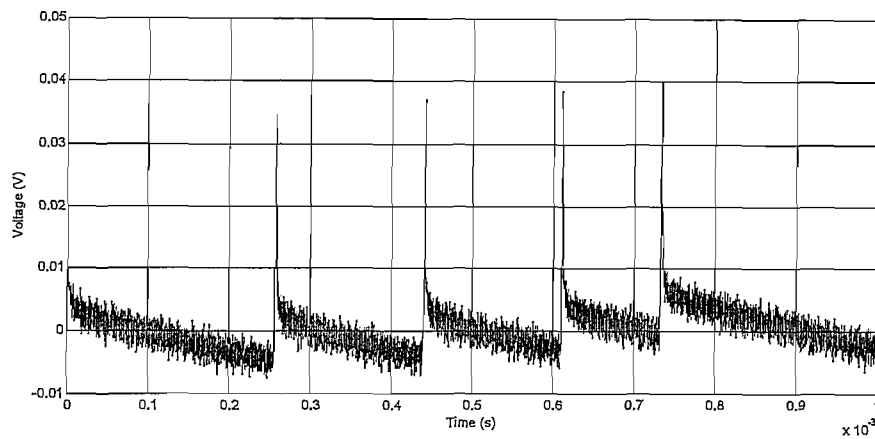


Figure 5-25 FPGA 3.3 V I/O supply voltage ripple

According to the manufacturers data for the FPGA the minimum limit for the +3.3 V I/O supply is +1.10 V while the absolute maximum limit, including the ripple voltage component, is +3.75 V. The +3.3 V I/O supply voltage of the FPGA power supply is thus well within these limits.

DSP power supply

The Texas Instruments TPS767D301 dual LDO regulator supplies the DSP with 1.8 V and 3.3 V. The DSP power supply is supplied with input power from the flyback converter +5 V output. The DC output voltage of the +1.8 V core supply voltage of the DSP power supply is shown in Figure 5-26 and measures +1.9 V.

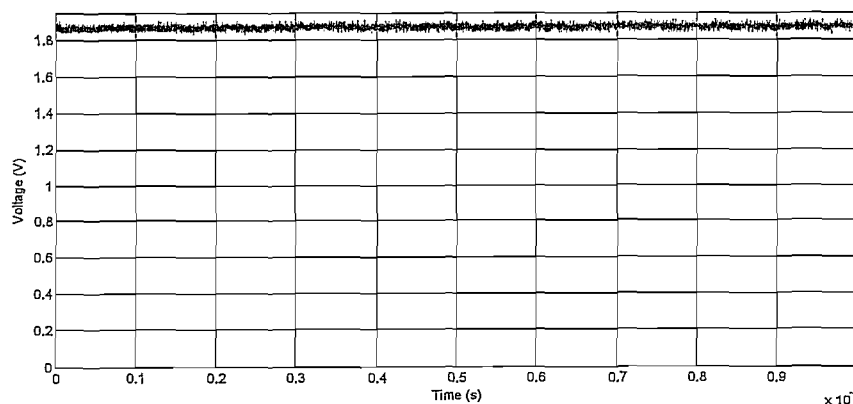


Figure 5-26 DSP 1.8 V core supply voltage

The AC ripple component of the +1.8 V core supply voltage output is shown in Figure 5-27. The peak to peak ripple voltage is approximately 16 mV.

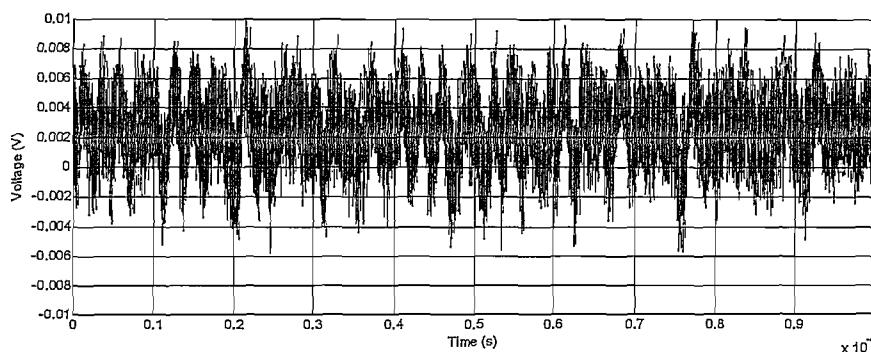


Figure 5-27 DSP 1.8 V core supply voltage ripple

According to the manufacturers data for the DSP the minimum limit for the +1.8 V core supply is +1.71 V while the absolute maximum limit, including the ripple voltage component, is +2.5 V. The +1.8 V core supply voltage of the DSP power supply is thus well within these limits.

The DC output voltage of the +3.3 V supply voltage of the DSP power supply is shown in Figure 5-28 and measures +3.3 V.

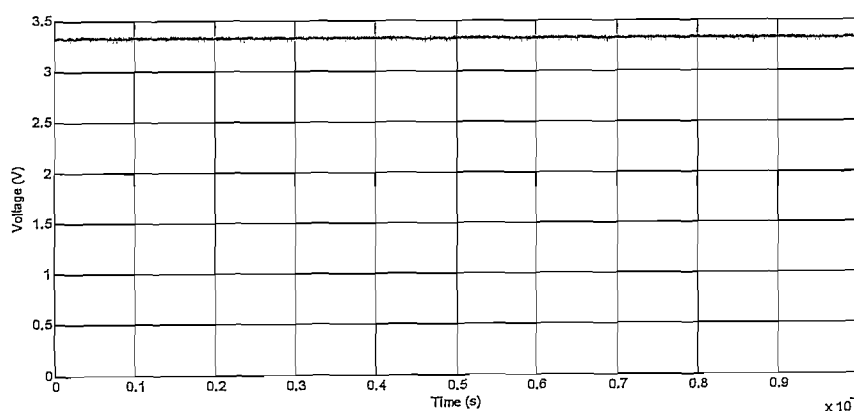


Figure 5-28 DSP 3.3 V supply voltage

The AC ripple component of the +3.3 V supply voltage output is shown in Figure 5-29. The peak to peak ripple voltage is approximately 5 mV.

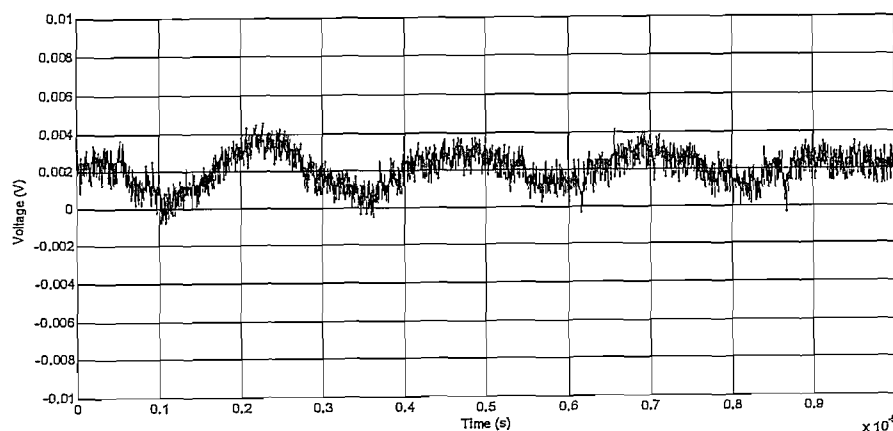


Figure 5-29 DSP 3.3 V supply voltage ripple

According to the manufacturers data for the DSP the minimum limit for the +3.3 V supply is +3.14 V while the absolute maximum limit, including the ripple voltage component, is +4.6 V. The +3.3 V supply voltage of the DSP power supply is thus well within these limits.

5.1.3 Digital controller

The digital controller PCB assembly is shown in Figure 5-30.

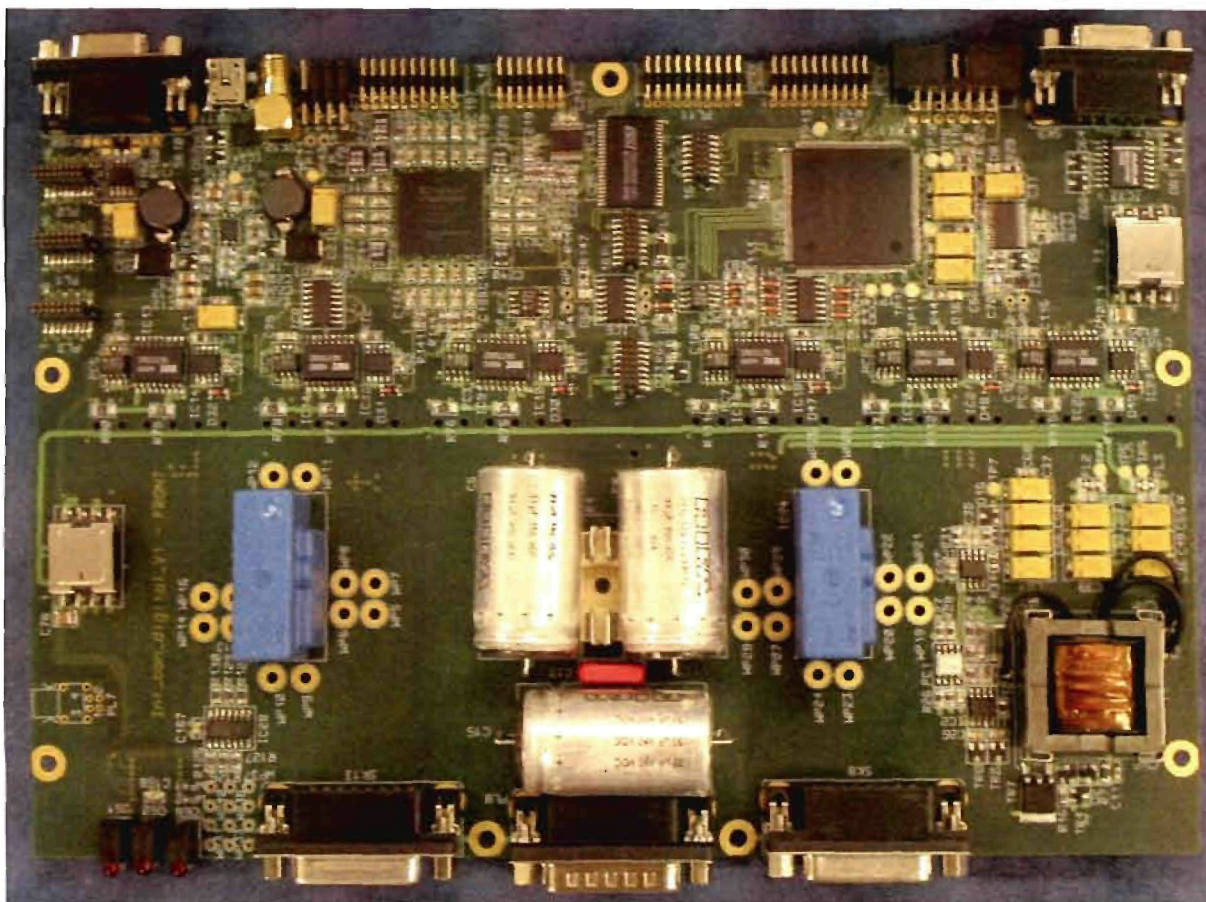


Figure 5-30 Digital controller PCB assembly

The evaluation of the digital controller involves a description of the resource usage, execution time and algorithm partitioning between the DSP and the FPGA co-processor for two self-sensing techniques that were successfully implemented on the integrated co-processor based power electronic drive. The two self-sensing techniques that were successfully implemented are the digital demodulation method, also referred to as Schammas's method, and the direct current measurement (DCM) method. The research that resulted in these self-sensing implementations is documented in [57].

Digital demodulation method

The block diagram in Figure 5-31 shows how the implementation of this method is partitioned between the FPGA and the DSP. The digital demodulation method has been described in

section 2.2.2 however the method implemented here uses an analog BPF, instead of a digital BPF.

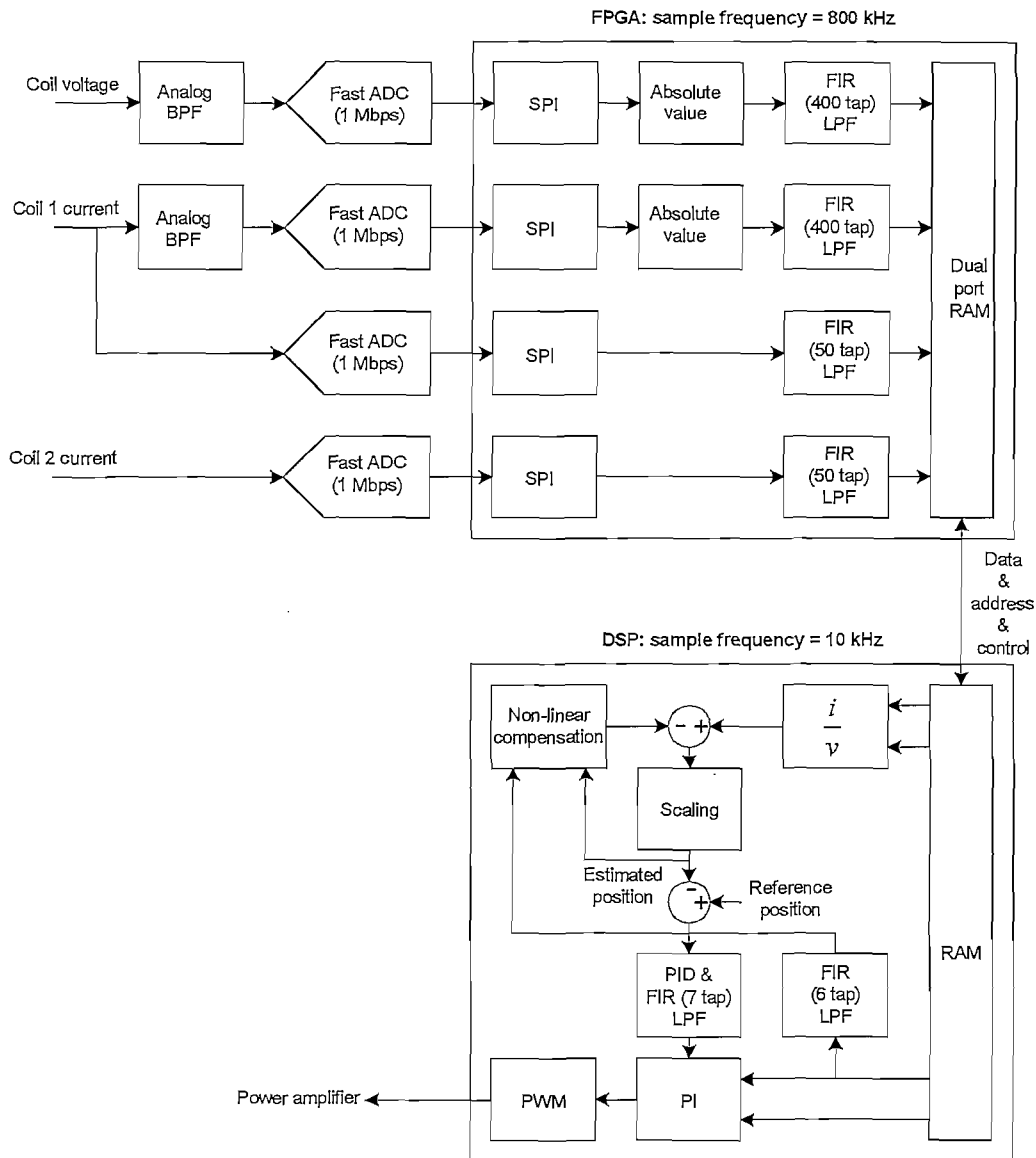


Figure 5-31 Digital demodulation block diagram

This is done to increase the resolution of the ripple component of the measured current to the full scale range of the ADC. The absolute value of the digitized current and voltage is calculated by the FPGA. The absolute values of the current and voltage are each filtered by a 400 tap, low pass FIR filter with a sampling frequency of 800 kHz. The two coil currents used to close the power amplifier current loop are also filtered by a 50 tap, low pass FIR filter with a sampling frequency of 800 kHz. The four high speed ADCs are individually interfaced to the FPGA via a SPI bus with four SPI master controllers' instantiated on the FPGA. Data is transferred between the FPGA and the DSP via a dual port RAM. The FPGA resources used to implement the digital demodulation self-sensing method are listed in table 5-2.

Table 5-2 FPGA resource usage, digital demodulation method

Resource	Number used	Number available	% used
Multipliers	14	20	70
Block RAM	16	20	80
Slices	1905	4656	40
CLBs	476	1164	40

The FPGA execution time is dominated by the 400 tap, low pass FIR filter since it is the most computationally intensive function performed by the FPGA. The number of times the FIR filter is instantiated doesn't affect the FPGA execution time since multiple instantiations of the filter are processed concurrently. The execution time of the 400 tap FIR filter is 880 ns consuming approximately 70 % of the 1.25 μ s sample time.

The DSP accommodates the non-linear compensation function including a 6 tap low pass FIR filter, a PID position loop controller with a 7 tap low pass FIR filter in the path of the derivative term and two PI current loop controllers. The sampling frequency for the DSP control function is 10 kHz. The DSP execution time for the digital demodulation self-sensing method was measured by setting the XF pin on the DSP at the beginning of the control interrupt and resetting the XF pin before exiting the interrupt. The XF pin is used because it takes a single clock cycle to set or reset thus only adding 13.3 ns of latency to the timing measurement. Each rising edge in the timing measurement in Figure 5-32 indicates the start of a control sampling period.

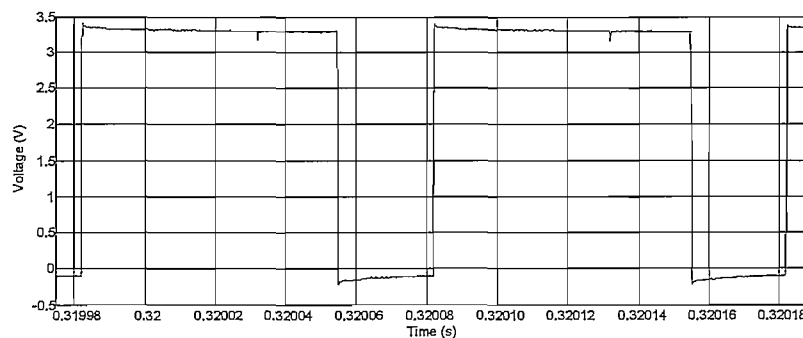


Figure 5-32 DSP execution time, digital demodulation method

Figure 5-32 shows the control sample time is exactly 100 μ s and that the DSP takes approximately 72 μ s to complete a control cycle.

Direct current measurement method

The block diagram in Figure 5-33 shows how the implementation of this method is partitioned between the FPGA and the DSP. The direct current measurement (DCM) method of self-sensing hasn't been described in this dissertation, therefore a brief explanation of this method

follows. The aim of the DCM method is to rescale the ripple current component of the measured current to the full scale range of the ADC before being digitized and to minimize phase loss due to filtering of the current during the demodulation process.

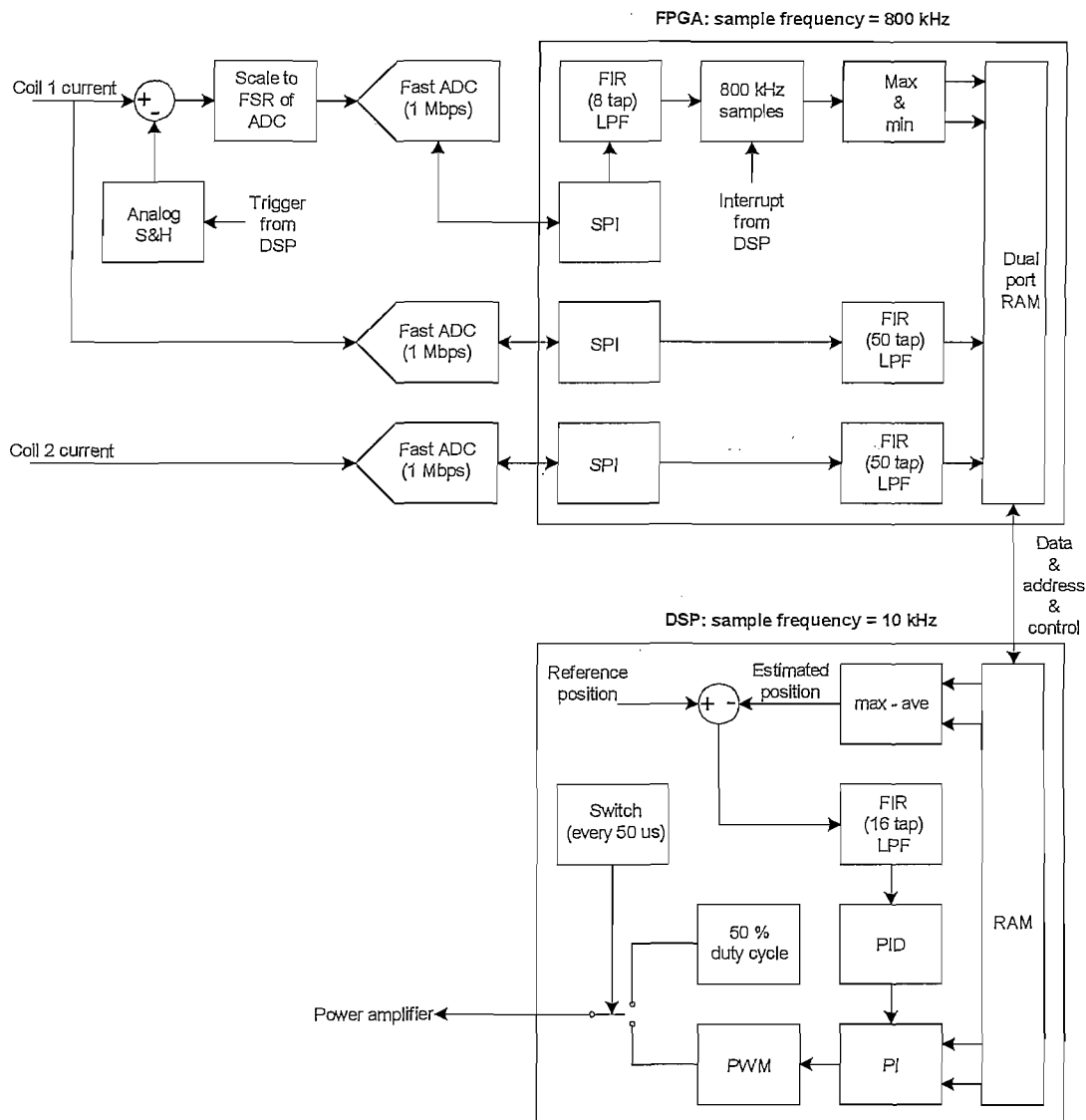


Figure 5-33 Direct current measurement block diagram

The DCM self-sensing technique only requires one coil current measurement for self-sensing. The DCM method eliminates the effect of duty cycle variation on the measured current by forcing the duty cycle to 50 % every alternate PWM cycle while the current is being measured. The control is executed every other PWM cycle. The DCM method virtually eliminates all filtering during the demodulation process thus reducing phase shift and improving the self-sensing performance of this method. A single 8 tap low pass FIR filter is used in this implementation to remove switching noise from the measured current. The pass band frequency of this filter is 20 kHz and the stop band frequency is 200 kHz, thus the shape of the triangular current waveform essentially remains unchanged.

At the start of a measurement period, while the duty cycle is forced to 50 %, a sample and hold is triggered to hold the control current at a constant level. The constant level is subtracted from the actual current measurement with only the ripple current remaining. The ripple current is scaled to the full scale range of the ADC before being digitized. During a control cycle the sample action of the sample and hold is activated thus the output of the sample and hold merely tracks the measured current [57].

As stated previously the sampled current is filtered by an 8 tap, low pass FIR filter with a sampling frequency of 800 kHz. The FPGA also calculates the maximum and minimum values of the sampled current. The two coil currents used to close the power amplifier current loop are each filtered by a 50 tap, low pass FIR filter with a sampling frequency of 800 kHz. The three high speed ADCs are individually interfaced to the FPGA via a SPI bus with three SPI master controllers' instantiated on the FPGA. Data is transferred between the FPGA and the DSP via a dual port RAM. The FPGA resources used to implement the DCM self-sensing method are listed in table 5-3.

Table 5-3 FPGA resource usage, DCM method

Resource	Number used	Number available	% used
Multipliers	1	20	5
Block RAM	3	20	15
Slices	742	4656	16
CLBs	186	1164	16

The FPGA execution time is dominated by the 50 tap, low pass FIR filter since it is the most computationally intensive function performed by the FPGA. The number of times the FIR filter is instantiated doesn't affect the FPGA execution time since multiple instantiations of the filter are processed concurrently. The execution time of the 50 tap FIR filter is 700 ns consuming approximately 56 % of the 1.25 μ s sample time.

The DSP subtracts the maximum and minimum values of the sampled current, executes a 16 tap low pass FIR filter, executes a PID position loop controller and two PI current loop controllers. The sampling frequency for the DSP control function is 10 kHz. The DSP execution time for the DCM self-sensing method was also measured by setting and resetting the XF pin on the DSP. The rising edge of the wider pulse in the timing measurement in Figure 5-34 indicates the start of a control sampling period.

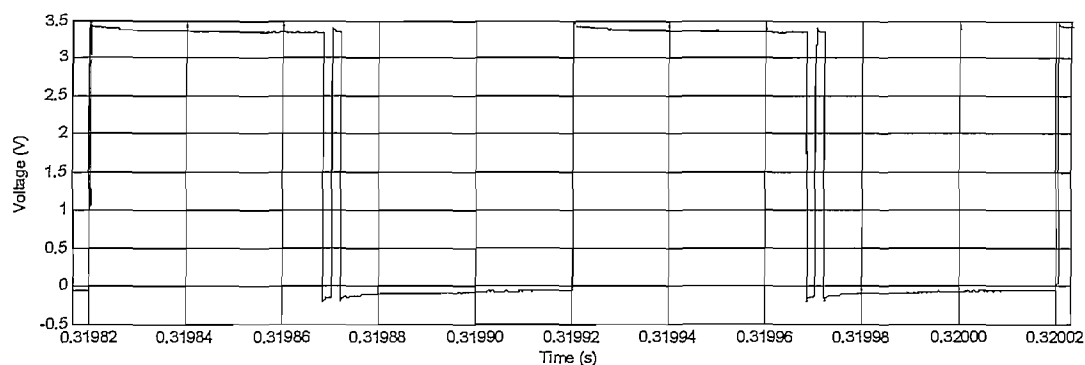


Figure 5-34 DSP execution time, DCM method

Figure 5-34 shows the control sample period is exactly 100 μs . During the wider 48 μs period, the DSP is executing a control cycle. During the narrower 1.85 μs period the DSP is forcing the PWM duty cycle to 50 % to take a current measurement. The switching between the control cycle and the measurement cycle takes place every 50 μs .

Both the DSP and the FPGA temperatures were measured to determine temperature rise and were found to be consistent. The DSP case temperature measured 68 $^{\circ}\text{C}$ that is higher than the predicted case temperature of 44 $^{\circ}\text{C}$. The predicted temperature rise is based on the manufacturer's typical data for the DSP and the assumption that all the unused peripheral clocks are disabled.

The FPGA case temperature measured 57 $^{\circ}\text{C}$ that is also higher than its predicted case temperature of 31 $^{\circ}\text{C}$. The FPGA temperature rise was estimated using the XPower Estimator (XPE) tool from Xilinx. The calculations were not based on the actual self-sensing algorithm implementation but on a design similar to the self-sensing algorithm. The difference in the predicted temperature rise versus the measured temperature rise indicates that the actual self-sensing algorithm is more complex than the algorithm used to estimate the temperature rise.

The resource usage and execution time of the DSP and the FPGA, for both self-sensing methods, is a highly pleasing result. For the digital demodulation method the DSP has 28% spare processing time available while the FPGA resource usage does not exceed 80%. The direct current measurement method only occupies the DSP for 50% of the available processing time while the FPGA resource usage does not exceed 16%. The combination of the TMS320F2812 DSP and the XC3S500E FPGA to form a co-processor proved to be more than adequate for this application. It is evident from the execution time measurements that the DSP would not have been able to provide the required processing power without the use of the FPGA as a co-processor.

5.2 System performance

It is beyond the scope of this dissertation to analyze the results of self-sensing research obtained using the integrated co-processor based power electronic drive as a hardware platform. However the definitive verification of the integrated co-processor based power electronic drive is its ability to facilitate the implementation of various self-sensing methods. For this reason two sets of position measurements obtained using the integrated co-processor based power electronic drive for self-sensing research are briefly illustrated here.

Digital demodulation method

The position measurement setup for this method involves applying a reference position to the system as indicated in Figure 5-31. In a practical system the reference position is maintained at 0 m, however for this measurement a dynamic reference position is applied to the system. The estimated position is measured at the point indicated in Figure 5-31. For comparison the actual position is measured with an eddy current sensor. Figure 5-35 shows the estimated position and measured position for the digital demodulation self-sensing method. The upper plot is the measured position and the lower plot is the estimated position. Figure 5-35 shows a high degree of correlation between the measured and estimated position.

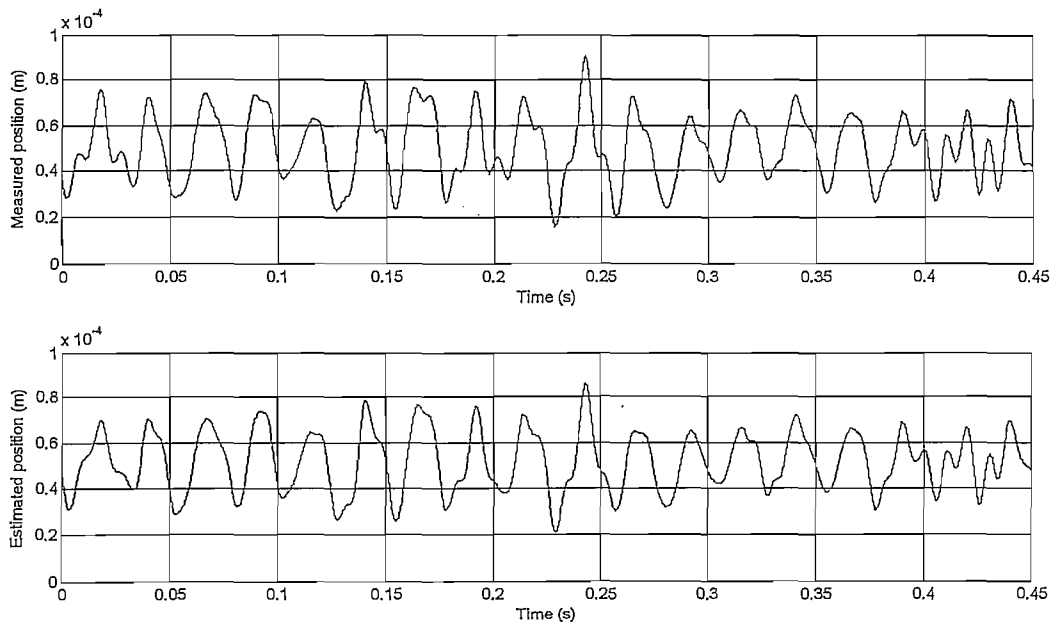


Figure 5-35 Measured and estimated position, digital demodulation method

Direct current measurement method

The position measurement setup for this method also involves applying a dynamic reference position to the system as indicated in Figure 5-33. The estimated position is measured at the point indicated in Figure 5-33. Once again the actual position is measured with an eddy current

sensor. Figure 5-36 shows the estimated position and measured position for the DCM self-sensing method.

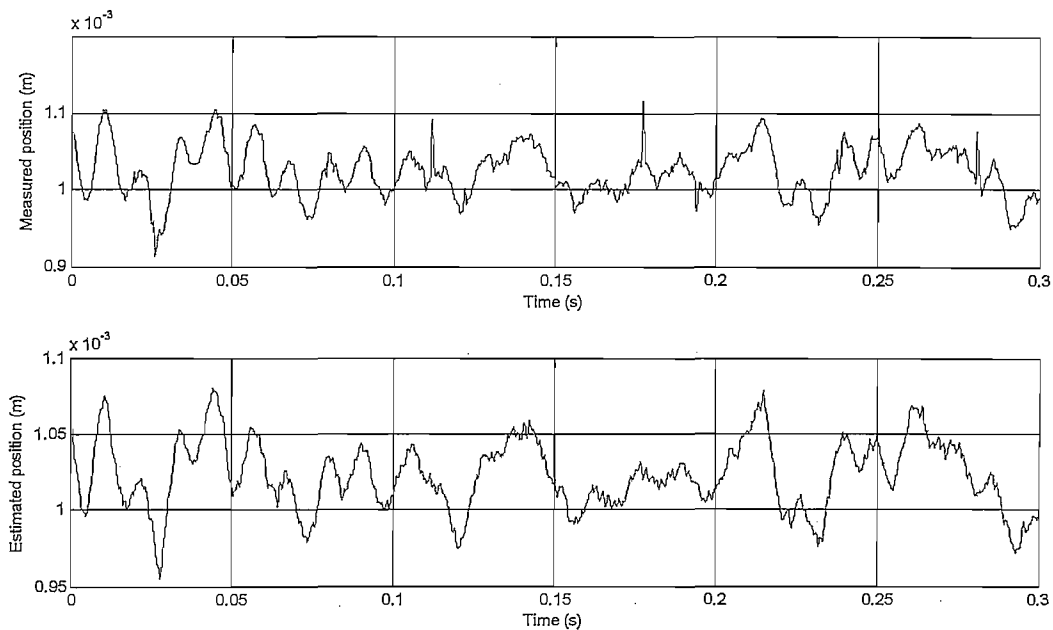


Figure 5-36 Measured and estimated position, DCM method

The upper plot is the measured position and the lower plot is the estimated position. This self-sensing method also shows a high degree of correlation between the measured and estimated position.

5.3 Conclusion

In Chapter 5 the integrated co-processor based power electronic drive was evaluated in terms of hardware measurements taken from a 1 DOF experimental self-sensing setup. The electronic supply, power amplifier and digital controller were evaluated individually. The system performance of the integrated co-processor based power electronic drive was briefly illustrated based on self-sensing results obtained in [57]. In Chapter 6 the result, recommendations and conclusion of this work is discussed

Chapter 6

Conclusion and recommendations

In Chapter 6 the results obtained with the integrated co-processor based power electronic drive are discussed. Recommendations for future work are proposed. The conclusion from this work is stated at the end of the chapter.

6.1 Results

Power amplifier

The large signal performance of the power amplifier proved to be reliable with adequate thermal performance when configured as a modified H-bridge. Although the pulse-for-pulse current limit function required a reference limit adjustment to compensate for circuit time delays, the power amplifier is capable of withstanding a short circuit operating condition. It was found that when the power amplifier is configured as an H-bridge, conduction occurs, between the IGBT in the high side and the IGBT in the low side of each half-bridge leg, during the PWM dead-time. This is related to the configuration options of the DSP on-chip PWM peripheral and will be addressed in future development. The small signal performance of the power amplifier requires further investigation since the measured small signal bandwidth differs from the simulated value. The resistance and the inductance of the electromagnet coil have to be verified as well as the amplitude of the current reference used to generate the small signal response.

Electronic supply

The electronic supply performed as expected with the DC and AC levels of all the outputs measuring within acceptable limits for all the output voltages. The load requirements for the flyback power supply were realistic since the power supply remained in the discontinuous operating mode at minimum input voltage.

Digital controller

The co-processor based architecture of the digital controller provided sufficient resources, processing speed and flexibility to accommodate a variety of self-sensing algorithms. Although

the digital controller performed adequately, by addressing a few hardware shortcomings that were identified during the self-sensing research, its performance can be further enhanced. The recommended hardware improvements include a 16 bit dual port RAM data interface between the FPGA and the DSP, anti-aliasing filters for the DSP on-chip ADC, a DAC interface between the FPGA and the analog interface PCB.

PCB design

The PCB design proved to be highly successful considering the complexity of the ten layer digital controller PCB. The signal integrity of this PCB proved to be satisfactory, however the SPI interface between the FPGA and the analog interface PCB was limited to a clock frequency of 16 MHz. From a mechanical rigidity perspective, a less rigid interface is required between the power amplifier substrate and the digital controller PCB.

System performance

The integrated co-processor based power electronic drive, although far from optimal, is extremely capable of functioning as a hardware platform for self-sensing AMB research. The DCM self-sensing method achieved the sensitivity required by an AMB system for unrestricted long-term operation [57].

6.2 Recommendations

The use of the integrated co-processor based power electronic drive in a 1 DOF experimental self-sensing setup provided the ideal opportunity to identify its functional limitations. The list of recommendations that follow may be considered for future work on integrated power electronic drives for self-sensing AMBs:

- The overall performance of the integrated drive may be improved by reducing all levels of noise present in the existing hardware. The analog interface PCB is the most susceptible to noise since it forms an interface with both the DSP and FPGA, complicating the grounding strategy. Revising the grounding strategy while limiting the interface to the analog interface PCB to the FPGA will improve the performance with respect to noise.
- The performance of the DCM self-sensing method may be improved by replacing the analog sample and hold device, on the analog interface electronics PCB, with a digital to analog converter (DAC). The communication interface for the DAC can be implemented in the FPGA on the controller PCB. The digital signal used to control the power amplifier determines the DC level and can thus be converted to an analog value by the DAC. The analog value is then subtracted from the measured current leaving only the ripple

component that is then scaled to the full scale range of the ADC. The advantage of the DAC method is that unwanted dynamic effects in the current measurement can be eliminated. The disadvantage of the DAC method is the complexity of routing the digital signals for the DAC to the analog interface PCB.

- The existing dual port RAM interface between the DSP and the FPGA on the digital controller PCB only makes provision for 8 bit data transfer. This limits the throughput of this interface because two 8 bit data transfers are required for each 16 bit data value. Future designs will benefit from a 16 bit data interface.
- The inputs to the ADC on the DSP are interfaced directly to the analog PCB. Provision for anti-aliasing filters on the controller PCB, before the inputs of ADCs, will be useful. A trade-off between attenuation and phase shift will be necessary in order to realize an optimal design.
- The method used by the DSP to implement PWM dead-time can be made more flexible by routing all the PWM outputs to the IR2113 integrated gate drive ICs via the FPGA. The FPGA can then route the PWM signals to the appropriate gate drive IC for a particular power amplifier configuration. In the present H-bridge configuration conduction occurs, between the IGBT in the high side and the IGBT in the low side of each half-bridge leg, during the dead-time.
- The physical interface between the digital controller and the analog interface PCB has to be optimized. The SPI interface signals between the FPGA and the high speed ADCs become distorted above 16 MHz which limits the sample rate of the ADCs to 800 Kbps instead of 1 Mbps.
- The inter PCB connectors between the power amplifier substrate and the digital controller PCB are extremely rigid and require a large force to assemble or disassemble. As a result the multi-layer controller PCB is at risk of being damaged. A less rigid interface is required between these assemblies.

6.3 Closure

In Chapter 1 of this dissertation a problem statement was developed that clearly identified the need for a co-processor based architecture to address the processing requirements for self-sensing AMBs. The problem identification also pointed to the necessity for a suitable power amplifier topology and the importance of signal integrity issues related to high speed PCB design.

A critical and comprehensive literature study was performed in Chapter 2 that provided the necessary insight into current technology trends. The literature study commenced with a review

of the AMB principle that was then extended to self-sensing AMB methods. The signal processing requirements of self-sensing algorithms were considered in terms of the capabilities of various signal processor architectures, ultimately justifying the co-processor architecture. Power amplifiers including linear, hybrid and switching amplifiers were reviewed. The switching PWM amplifier was identified as the most suitable for this application. The uni-polar PWM, bipolar PWM and SVPWM modulation techniques were reviewed. The integrated co-processor based power electronic drive makes provision for the implementation of all these PWM techniques. Various aspects of PCB design were considered including signal integrity and layer structure.

Chapter 3 and Chapter 4 of this dissertation focused on design synthesis and simulation. A conceptual design was conducted in Chapter 3 where trade-off studies and circuit simulation were used to determine the architecture, interfaces and functionality, of the integrated co-processor based power electronic drive. Where possible, circuit topologies were simulated to assist in the design process, trade-off studies were used elsewhere. A detail design was performed where specific issues such as component selection, power supply requirements and thermal design were considered.

Design verification and validation was reported in Chapter 5. The integrated co-processor based power electronic drive was evaluated in terms of hardware measurements and system performance. The verification shows that, in spite of a few minor functional limitations, the integrated co-processor based power electronic drive performed extremely well as a hardware platform for implementing various self-sensing techniques.

A number of recommendations are made to address the functional limitations that were identified while using the integrated co-processor based power electronic drive. These recommendations may be considered for future work on integrated drives for self-sensing AMBs.

In conclusion, the aim of this dissertation was to develop a hardware platform suitable for researching various self-sensing techniques for AMBs. To this end the development can be considered a success since the members of the McTronX research group were able to effectively use the integrated co-processor based power electronic drive for its intended purpose.

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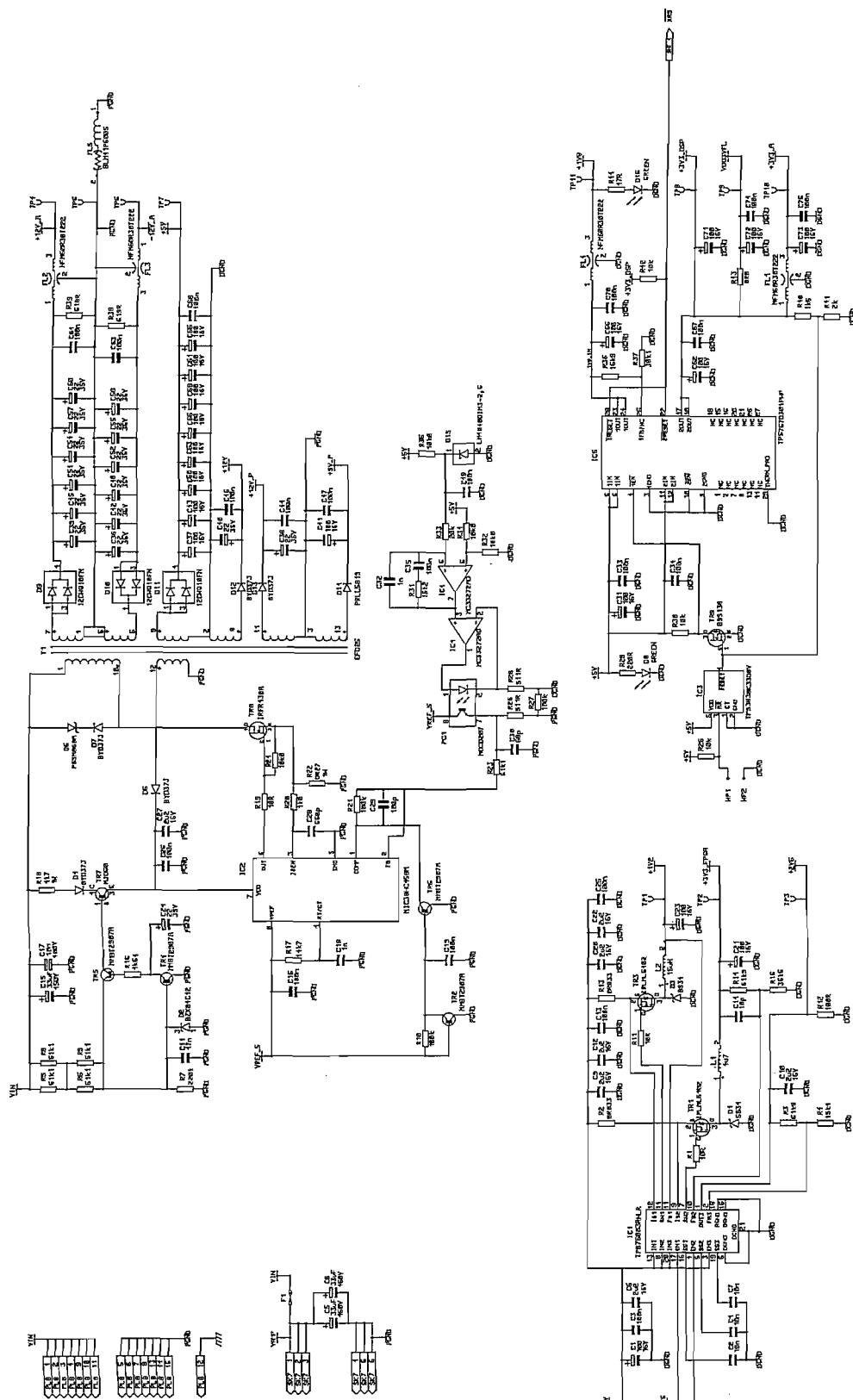
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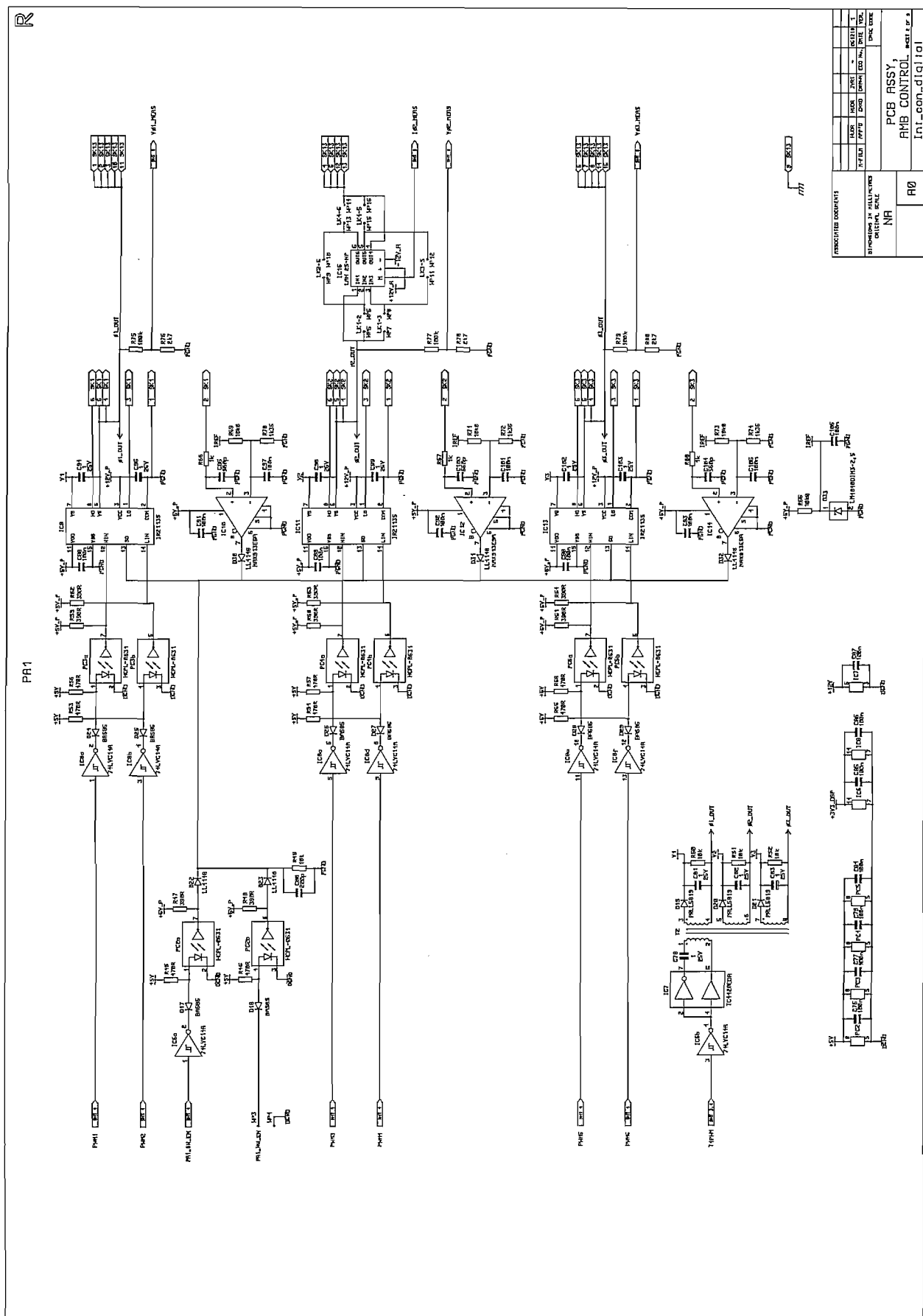
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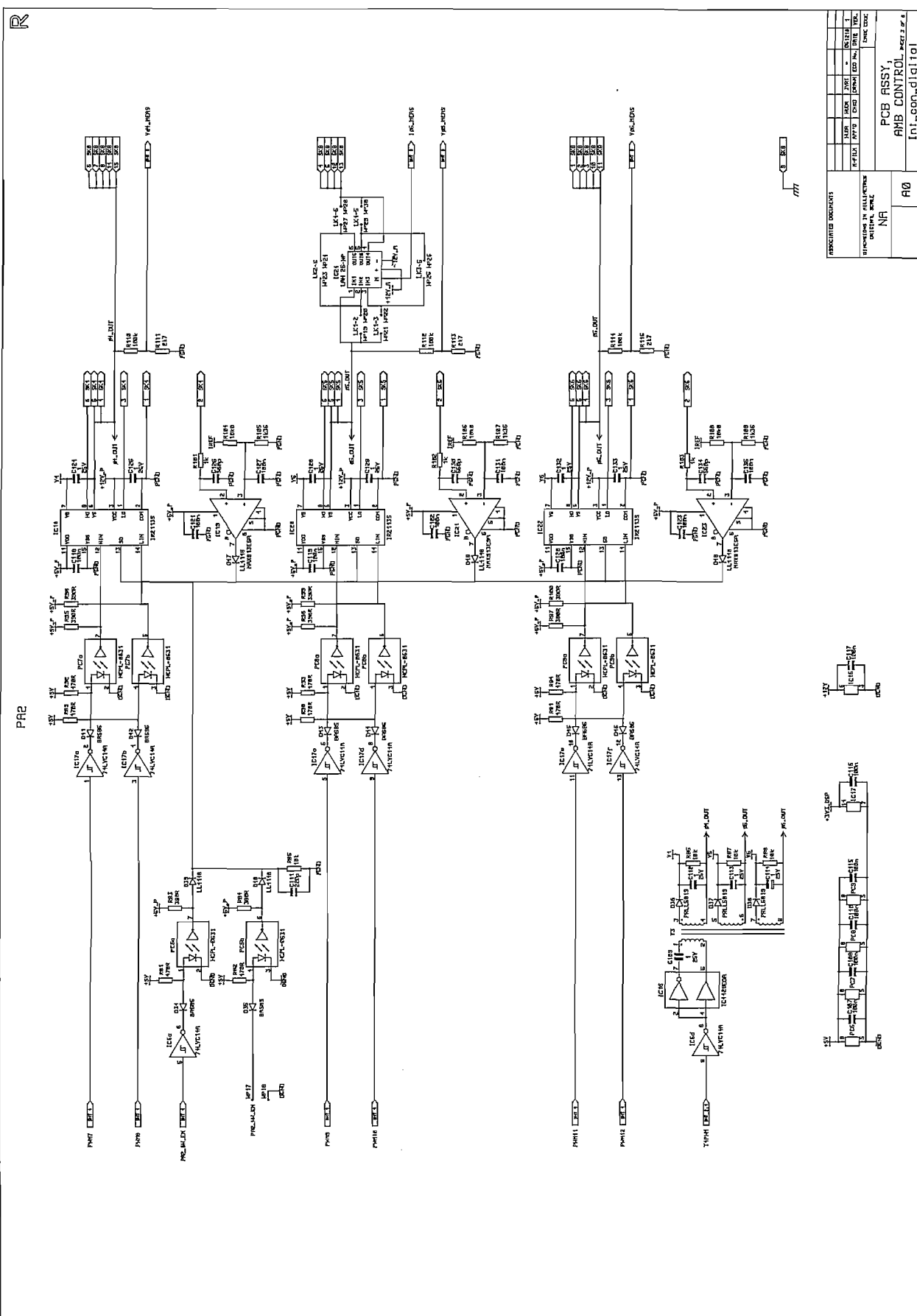
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Appendix

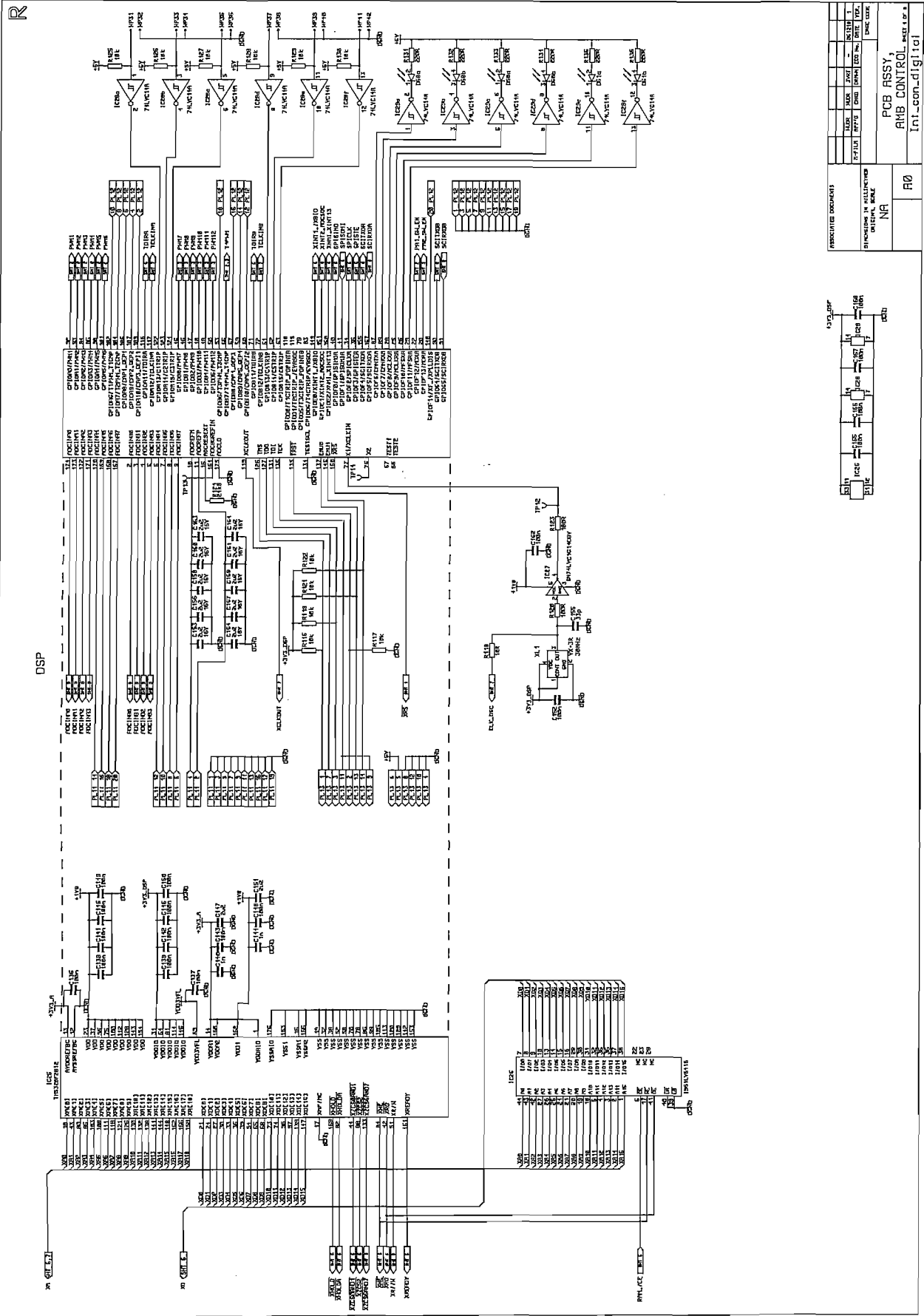
Appendix A: Digital controller schematic diagram

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UNCLASSIFIED DOCUMENTS		NA INFORMATION IN ALL/CITIZENS UNLAWFUL, SCALPEL		PCB ASSY; AMB CONTROL		PAGE 2 OF 8 Int-con-digital	
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UNCLASSIFIED DOCUMENTS							

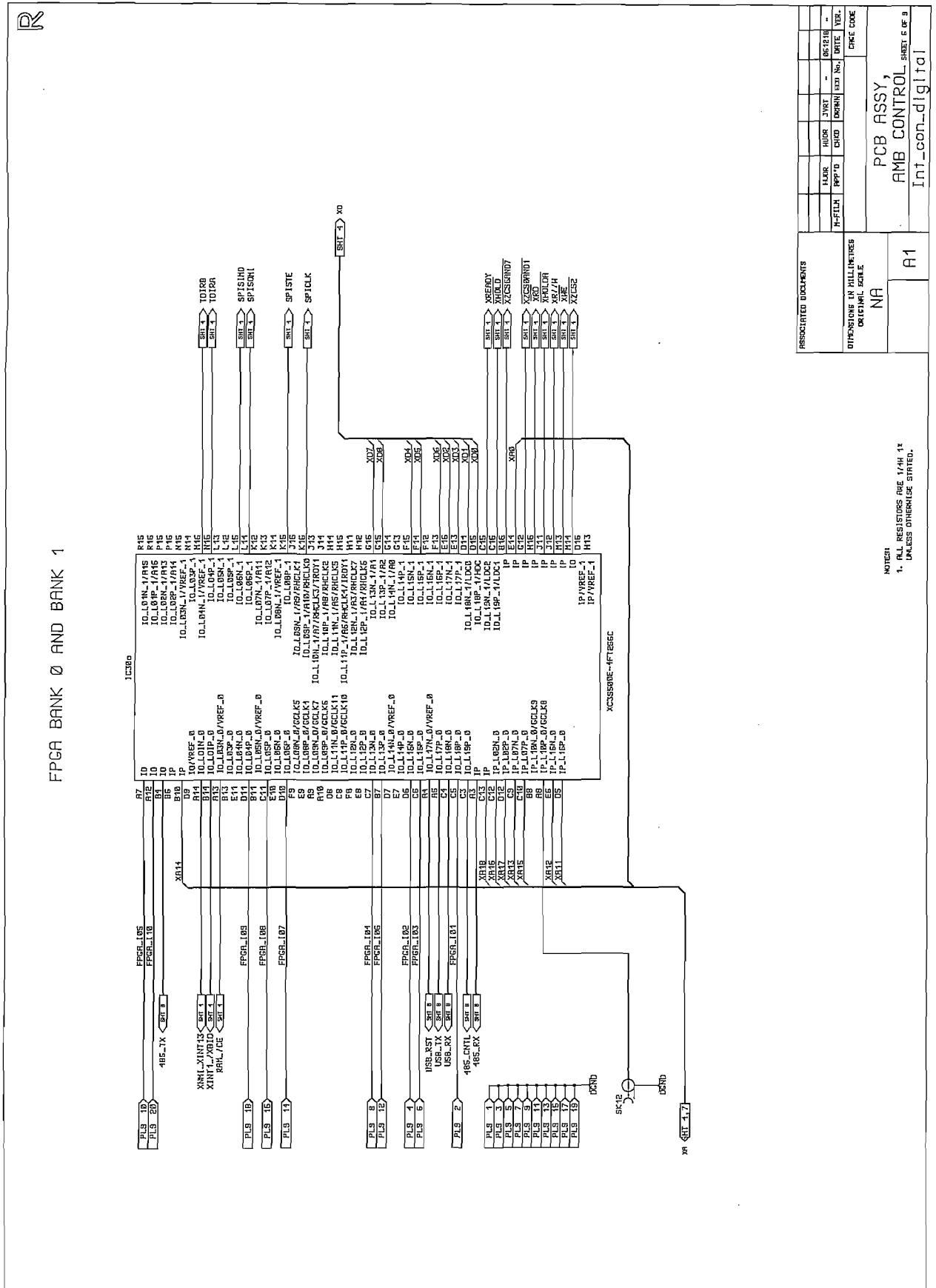


The diagram shows a complex PCB layout for a microcontroller-based system. Key components include:

- Microcontroller:** A central IC, likely a microcontroller, with various pins connected to the power supply, ground, and peripheral components.
- Power Supply:** A +3V3_FPGA supply is shown, connected to the microcontroller and other components. A +2V5 supply is also indicated.
- Resistors:** Numerous resistors are placed throughout the board, including R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R197, R198, R199, R200, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R227, R228, R229, R230, R231, R232, R233, R234, R235, R236, R237, R238, R239, R240, R241, R242, R243, R244, R245, R246, R247, R248, R249, R250, R251, R252, R253, R254, R255, R256, R257, R258, R259, R260, R261, R262, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R278, R279, R280, R281, R282, R283, R284, R285, R286, R287, R288, R289, R290, R291, R292, R293, R294, R295, R296, R297, R298, R299, R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R310, R311, R312, R313, R314, R315, R316, R317, R318, R319, R320, R321, R322, R323, R324, R325, R326, R327, R328, R329, R330, R331, R332, R333, R334, R335, R336, R337, R338, R339, R340, R341, R342, R343, R344, R345, R346, R347, R348, R349, R350, R351, R352, R353, R354, R355, R356, R357, R358, R359, R360, R361, R362, R363, R364, R365, R366, R367, R368, R369, R370, R371, R372, R373, R374, R375, R376, R377, R378, R379, R380, R381, R382, R383, R384, R385, R386, R387, R388, R389, R390, R391, R392, R393, R394, R395, R396, R397, R398, R399, R400, R401, R402, R403, R404, R405, R406, R407, R408, R409, R410, R411, R412, R413, R414, R415, R416, R417, R418, R419, R420, R421, R422, R423, R424, R425, R426, R427, R428, R429, R430, R431, R432, R433, R434, R435, R436, R437, R438, R439, R440, R441, R442, R443, R444, R445, R446, R447, R448, R449, R450, R451, R452, R453, R454, R455, R456, R457, R458, R459, R460, R461, R462, R463, R464, R465, R466, R467, R468, R469, R470, R471, R472, R473, R474, R475, R476, R477, R478, R479, R480, R481, R482, R483, R484, R485, R486, R487, R488, R489, R490, R491, R492, R493, R494, R495, R496, R497, R498, R499, R500, R501, R502, R503, R504, R505, R506, R507, R508, R509, R510, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R540, R541, R542, R543, R544, R545, R546, R547, R548, R549, R550, R551, R552, R553, R554, R555, R556, R557, R558, R559, R560, R561, R562, R563, R564, R565, R566, R567, R568, R569, R570, R571, R572, R573, R574, R575, R576, R577, R578, R579, R580, R581, R582, R583, R584, R585, R586, R587, R588, R589, R590, R591, R592, R593, R594, R595, R596, R597, R598, R599, R600, R601, R602, R603, R604, R605, R606, R607, R608, R609, R610, R611, R612, R613, R614, R615, R616, R617, R618, R619, R620, R621, R622, R623, R624, R625, R626, R627, R628, R629, R630, R631, R632, R633, R634, R635, R636, R637, R638, R639, R640, R641, R642, R643, R644, R645, R646, R647, R648, R649, R650, R651, R652, R653, R654, R655, R656, R657, R658, R659, R660, R661, R662, R663, R664, R665, R666, R667, R668, R669, R670, R671, R672, R673, R674, R675, R676, R677, R678, R679, R680, R681, R682, R683, R684, R685, R686, R687, R688, R689, R690, R691, R692, R693, R694, R695, R696, R697, R698, R699, R700, R701, R702, R703, R704, R705, R706, R707, R708, R709, R710, R711, R712, R713, R714, R715, R716, R717, R718, R719, R720, R721, R722, R723, R724, R725, R726, R727, R728, R729, R730, R731, R732, R733, R734, R735, R736, R737, R738, R739, R740, R741, R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753, R754, R755, R756, R757, R758, R759, R760, R761, R762, R763, R764, R765, R766, R767, R768, R769, R770, R771, R772, R773, R774, R775, R776, R777, R778, R779, R780, R781, R782, R783, R784, R785, R786, R787, R788, R789, R790, R791, R792, R793, R794, R795, R796, R797, R798, R799, R800, R801, R802, R803, R804, R805, R806, R807, R808, R809, R810, R811, R812, R813, R814, R815, R81

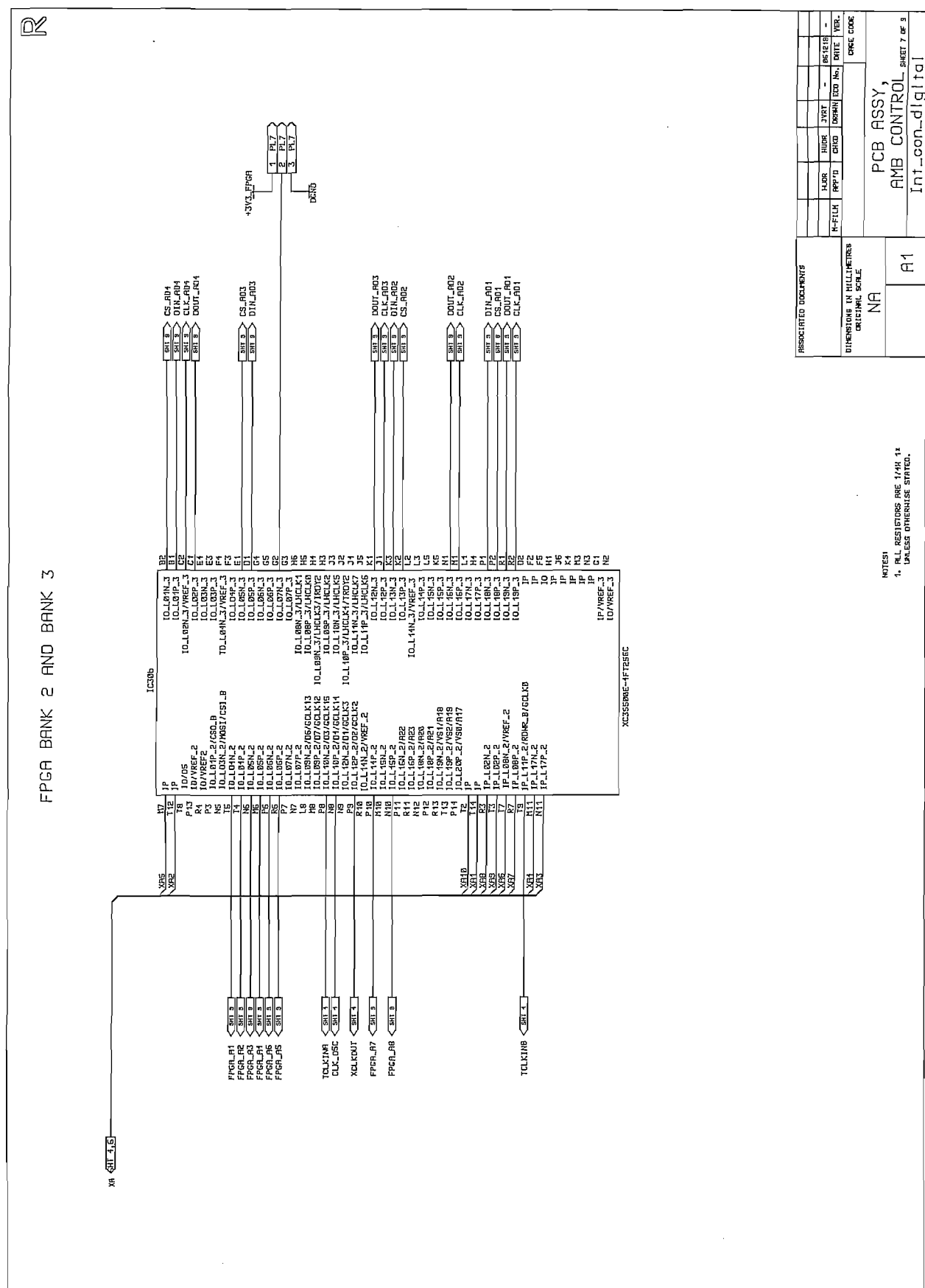
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1. ALL RESISTORS ARE 1/4W 1% UNLESS OTHERWISE STATED.

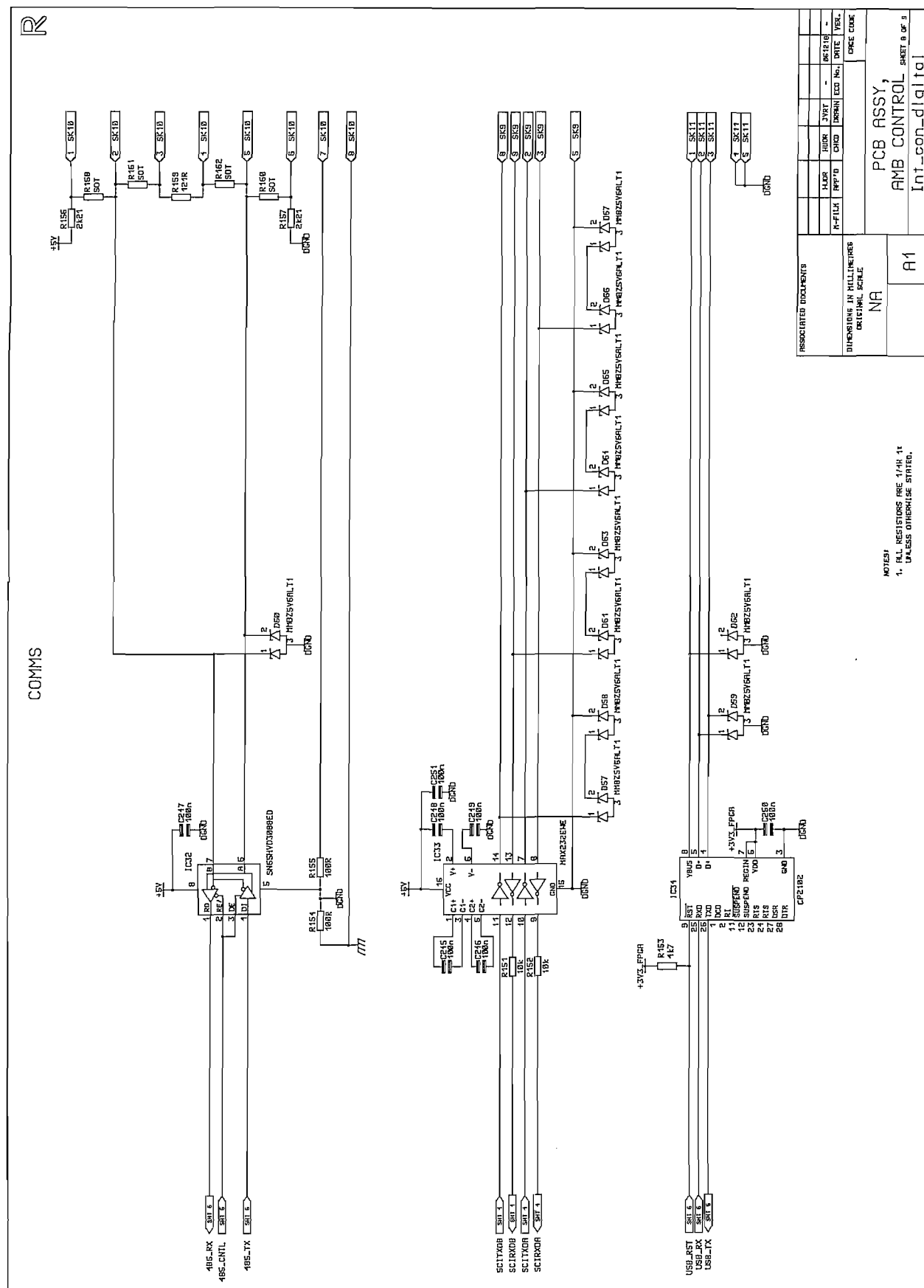
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NOTES:
1. ALL RESISTORS ARE 1/4W 1%
UNLESS OTHERWISE STATED.

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FILE	REV	DATE	VER.
FILE	REV	DATE	VER.
ORIGINAL SCALE			
PCB ASSY,			
AMB CONTROL			
Int_con_digital			
A1			





NOTES:
1. ALL RESISTORS ARE 1/4W 1% UNLESS OTHERWISE STATED.

	ASSOCIATED DOCUMENTS							
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Appendix B: Power amplifier schematic diagram

