24th International Conference & Exhibition on Electricity Distribution (CIRED)

12-15 June 2017

Session 2: Power quality and electromagnetic compatibility

Dc-bus voltage balancing controllers for split dc-link four-wire inverters and their impact on the quality of the injected currents

ISSN 2515-0855
doi: 10.1049/oap-cired.2017.0662
www.ietdl.org

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Abstract: The increasing share of single-phase distributed generation units in low-voltage grids causes voltage unbalance problems and overvoltages. Therefore, the need for power quality improving control strategies of grid-connected inverters emerges. Some control strategies require three-phase four-wire inverter topologies. The simplest way to connect the fourth wire is by connecting it to the mid-point of the dc-bus. This sometimes causes challenges in the stabilisation of the mid-point. In this article, two algorithms for stabilising the midpoint of a three-phase four-wire inverter are proposed. Both algorithms are described in detail and validated experimentally. The results showed that both algorithms perform well under perturbations and are able to maintain the midpoint potential close to zero, while the quality of the injected currents is not deteriorated.

1 Introduction

The continuous increase in small distributed generation units connected to low-voltage distribution grids already has a negative impact on the power quality such as overvoltages, voltage unbalance, and increase in voltage waveform distortions. Many control strategies that are able to mitigate voltage unbalance were developed, but their main disadvantage is that they impact only the negative-sequence component, while the zero-sequence component remains. In [1], an inverter-based control algorithm named three-phase damping control strategy is proposed that is able to mitigate voltage unbalance by emulating a resistive behaviour towards the zero- and the negative-sequence voltage components. The control strategy relies on local measurements at the inverter terminals and reacts very fast to perturbations (in the order of one grid cycle). In [2, 3], the same control strategy was extended with a drooping controller that determines the injected active power based on the rms value of the grid voltage. The study showed that the penetration level of renewables can be increased while maintaining the power quality within the prescribed limits by the standard EN50160 [4]. Therefore, control strategies that are able to improve the power quality become more attractive.

In order to have an impact on the zero-sequence voltage component, these control strategies are interfaced to the grid via a three-phase four-wire inverter where the neutral is formed via additional hardware such as capacitors, inductors, semiconductor switches, or a combination. However, the neutral point drifts from its original value due to circulating currents, common-mode currents, neutral currents, and other perturbations. This leads to the increase in harmonic distortion of the injected currents, possible dc component injection, and the malfunction of the inverter.

Therefore, keeping the midpoint stable is of great importance. For multi-level neutral point clamped inverters, solutions based on space vector modulation are proposed in the literature [5, 6]. Unfortunately, these inverters require complex control and this makes them less attractive for low-voltage DG units. On the other hand, the two-level neutral point clamped inverter topologies are less complex, but maintaining the midpoint potential requires additional hardware [5–7]. Figs. 1*a* and *b* depict two state-of-the-art topologies that are able to maintain the potential of the midpoint actively. The disadvantages of both topologies are the additional power-electronic leg and also its control.

Therefore, it is better to keep the control complexity and the inverter topology as little as possible. Consequently, the additional switches and complex modulation strategy can be avoided; therefore, the topology depicted in Fig. 1*c* is preferred due to its simplicity. In this article, the topology shown in Fig. 1*c* is used and two software solutions that are able to maintain the voltage potential of C_1 and C_2 equal are proposed and maintain the midpoint potential equal to zero.

This paper is organised as follows. In Section 2, a detailed description on the operation of the three-phase damping control strategy is given. In Section 3, the proposed midpoint control algorithms are mathematically described and the open-loop transfer functions are extracted. In Section 4, the proposed control algorithms are experimentally validated on a three-phase four-wire inverter equipped with the three-phase damping control strategy. In the last section, some conclusions are drawn.

2 Three-phase damping control strategy

The three-phase damping control strategy is used to experimentally validate the proposed control algorithms for maintaining the midpoint potential. In order to mitigate the voltage unbalance, the three-phase damping control strategy injects more current in the phase with the lowest voltage and less currents in the phases with the highest voltage. This can result in high neutral current that can further shift the midpoint potential and it can be used to validate the proposed algorithms.

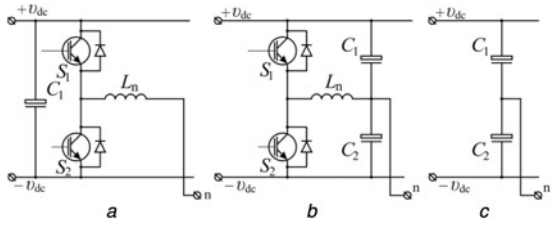

Fig. 1 *Fourth leg topologies which*

(a) Fourth wire formed by additional leg, ***(b)*** Fourth wire formed by additional leg and split capacitors, ***(c)*** Fourth wire formed by using only split capacitors

2.1 Mathematical description

Harmonic distortions of the voltage waveforms will not be considered in this paper. The phase currents can be written as: (see (1))where $\underline{v}_a$, $\underline{v}_b$, and $\underline{v}_c$ are the phase voltages, θ_a, θ_b, and θ_c are the respective phase angles, g_d is the damping conductance and g_1 the input conductance. The terms in (1) related to g_1 can be interpreted as the steady-state value of the fundamental component of the injected current. These terms are adapted by the dc-bus voltage controller in order to balance the power exchanged with the grid. Since the dc-bus voltage controller is slow, g_1 is slowly varying. The terms related to g_d emulate the resistive behaviour towards the zero- and negative-sequence voltage components.

2.2 Block diagram

The used control strategy is interfaced to the grid as shown in Fig. 2 and the block diagram of the three-phase damping control strategy is depicted in Fig. 3. The power balance is maintained by the dc-bus voltage controller and its output signal g_1 is the fundamental input conductance. All phase voltages $v_{g,a}$, $v_{g,b}$, and $v_{g,c}$ are

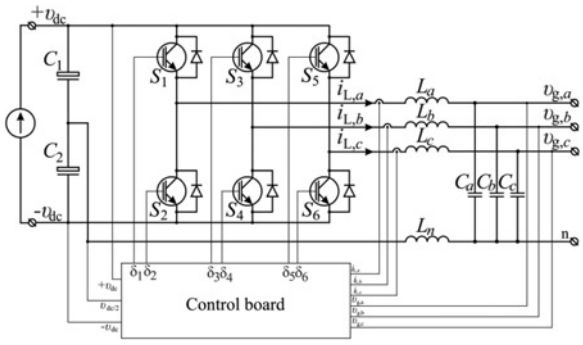

Fig. 2 *Block diagram of a three-phase four-wire inverter with a split dc link capacitor*

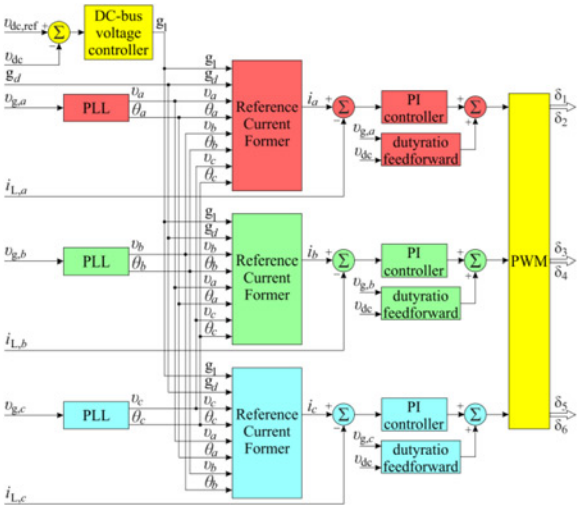

Fig. 3 *Block diagram on the three-phase damping control strategy*

normalised and passed to a phase locked loop (PLL) which extracts the phase voltage magnitude and the phase angle v_a, θ_a, v_b, θ_b, v_c, and θ_c. The damping conductance g_d sets the resistive behaviour of the inverter [2, 3]. These signals are used for the calculation of the reference currents i_a, i_b, and i_c in the reference current former blocks. The calculated reference currents are added to the measured currents $i_{L,a}$, $i_{L,b}$, and $i_{L,c}$ and PI controllers calculate the needed action to zero the error between the reference and the measured value. Since the PI controller has poor performance in tracking second-order reference signals, its output is added to a duty ratio feed-forward block [8]. The output of this block is used to generate the driving signals for the semiconductor switches. The dc-bus controller is sampled with 100 Hz sampling frequency, while the current controller is sampled with 20 kHz.

The dc-bus controller ensures the power balance between the ac and the dc side and it also maintains the dc-bus voltage to enable current injection into the grid [9]. The power balance between the ac and the dc side can be written as:

$$\begin{aligned} p_1(t) = {} & v_{g,a}(t) + i_{L,a}(t) - \frac{L_a + L_n}{2}\frac{\mathrm{d}(i_{L,a}(t))^2}{\mathrm{d}t} \\ & + v_{g,b}(t) + i_{L,b}(t) - \frac{L_b + L_n}{2}\frac{\mathrm{d}(i_{L,b}(t))^2}{\mathrm{d}t} \\ & + v_{g,c}(t) + i_{L,c}(t) - \frac{L_c + L_n}{2}\frac{\mathrm{d}(i_{L,c}(t))^2}{\mathrm{d}t} \end{aligned} \tag{2}$$

where, $p_1(t)$ is the power of the fundamental component, $v_{g,x}$ and $i_{g,x}$ are the respective phase voltages and currents L_x and L_n are the differential filter inductances for the corresponding phase and

$$\begin{aligned} \underline{i}_a &= \frac{1}{3}\cdot\left\{\begin{array}{l} g_1\left[|\underline{v}_a|\cdot\exp(\mathrm{j}\theta_a) + |\underline{v}_b|\cdot\exp\left(\mathrm{j}\left(\theta_b + \frac{2\cdot\pi}{3}\right)\right) + |\underline{v}_c|\cdot\exp\left(\mathrm{j}\left(\theta_c - \frac{2\cdot\pi}{3}\right)\right)\right] \\ + g_d\cdot\left[2\cdot|\underline{v}_a|\cdot\exp(\mathrm{j}\theta_a) - |\underline{v}_b|\cdot\exp\left(\mathrm{j}\left(\theta_b + \frac{2\cdot\pi}{3}\right)\right) - |\underline{v}_c|\cdot\exp\left(\mathrm{j}\left(\theta_c - \frac{2\cdot\pi}{3}\right)\right)\right] \end{array}\right\} \\ \underline{i}_b &= \frac{1}{3}\cdot\left\{\begin{array}{l} g_1\left[|\underline{v}_b|\cdot\exp(\mathrm{j}\theta_b) + |\underline{v}_a|\cdot\exp\left(\mathrm{j}\left(\theta_a - \frac{2\cdot\pi}{3}\right)\right) + |\underline{v}_c|\cdot\exp\left(\mathrm{j}\left(\theta_c + \frac{2\cdot\pi}{3}\right)\right)\right] \\ + g_d\cdot\left[2\cdot|\underline{v}_b|\cdot\exp(\mathrm{j}\theta_b) - |\underline{v}_a|\cdot\exp\left(\mathrm{j}\left(\theta_a - \frac{2\cdot\pi}{3}\right)\right) - |\underline{v}_c|\cdot\exp\left(\mathrm{j}\left(\theta_c + \frac{2\cdot\pi}{3}\right)\right)\right] \end{array}\right\} \\ \underline{i}_c &= \frac{1}{3}\cdot\left\{\begin{array}{l} g_1\left[|\underline{v}_c|\cdot\exp(\mathrm{j}\theta_c) + |\underline{v}_a|\cdot\exp\left(\mathrm{j}\left(\theta_a + \frac{2\cdot\pi}{3}\right)\right) + |\underline{v}_b|\cdot\exp\left(\mathrm{j}\left(\theta_b - \frac{2\cdot\pi}{3}\right)\right)\right] \\ + g_d\cdot\left[2\cdot|\underline{v}_c|\cdot\exp(\mathrm{j}\theta_c) - |\underline{v}_a|\cdot\exp\left(\mathrm{j}\left(\theta_a + \frac{2\cdot\pi}{3}\right)\right) - |\underline{v}_b|\cdot\exp\left(\mathrm{j}\left(\theta_b - \frac{2\cdot\pi}{3}\right)\right)\right] \end{array}\right\} \end{aligned} \tag{1}$$

neutral inductor, respectively. By replacing the phase currents with the corresponding input conductance $g_x(t)$, then the power balance equation can be written as:

$$\begin{aligned} p_1(t) &= g_a(t)v_{g,a}(t)^2 + -\frac{L_a + L_n}{2}\frac{\mathrm{d}(g_a(t)v_{g,a}(t))^2}{\mathrm{d}t} \\ &+ g_b(t)v_{g,b}(t)^2 + -\frac{L_b + L_n}{2}\frac{\mathrm{d}(g_b(t)v_{g,b}(t))^2}{\mathrm{d}t} \\ &+ g_c(t)v_{g,c}(t)^2 + -\frac{L_c + L_n}{2}\frac{\mathrm{d}(g_c(t)v_{g,c}(t))^2}{\mathrm{d}t} \\ &= \eta p_{dc}(t) - \eta\frac{C_{dc}}{2}\frac{\mathrm{d}(v_{dc}(t))^2}{\mathrm{d}t} \end{aligned} \tag{3}$$

where η is the efficiency of the power electronic inverter, C_{dc} is the dc-bus capacitor value, and $v_{dc}(t)$ is the instantaneous value of the dc-bus voltage. Knowing that:

$$x = X + \hat{x} \tag{4}$$

and with the phase voltage equal to:

$$V_{g,x} = \sqrt{2}V_{rms}\sin(\omega t + \theta_x) \tag{5}$$

The small signal model can now be obtained after substituting (4) and (5) in (3) and simplifying it to (6):

$$g_{tot}(t)V_{rms}^2 - (L_a + L_n)GV_{rms}^2 = \eta\hat{p}_{dc}(t) - \eta\frac{C_{dc}\mathrm{d}V_{dc}\hat{v}_{dc}(t)}{\mathrm{d}t} \tag{6}$$

Equation (6) can be expressed in the Laplace domain as follows:

$$\hat{v}_{dc}(s) = \hat{p}_{DC}(s)\frac{1}{\eta s V_{dc}C_{dc}} + \hat{g}_{tot}(s)\frac{3V_{rms}(sL_fG_{tot} - 1)}{\eta s V_{dc}C_{dc}} \tag{7}$$

Further simplification to:

$$\frac{\hat{v}_{dc}(s)}{\hat{g}_{tot}(s)} = \frac{1}{\eta\tau}\frac{-1}{s} \tag{8}$$

where $\hat{g}_{tot} = \hat{g}_a + \hat{g}_b + \hat{g}_c$ is the total input conductance and $\tau = \eta V_{dc}C_{dc}/3V_{rms}$.

The open-loop transfer function in the z-domain becomes:

$$G(z) = \frac{T}{2\tau}\frac{z+1}{z(z-1)} \tag{9}$$

The sampling time of this PI controller is 10 ms and it calculates its new output value at every zero crossing of phase a.

3 Midpoint stabilisation

3.1 Split dc-bus controller

The first solution is depicted in Fig. 4*a* and it uses two identical dc-bus controllers to maintain the equilibrium between v_{C1} and v_{C2}. A detailed block diagram of this algorithm is shown in Fig. 5. In this diagram, only one of the phases is depicted, but the principle is the same as the other two phases. The output of the dc-bus controllers is $g_{1,n}$ and $g_{1,p}$, where the first one is used to determine the negative half-sine and the other, the positive half sine of the reference currents. The output of the two controllers is passed to a multiplexer that switches between $g_{1,n}$ and $g_{1,p}$ depending on the output of the sign detector. A sign detector block generates its output state based on the zero-crossing of the synchronised PLL signal for the respective phase. The total input conductance $g_{1,tot}$, together with the other signals voltage

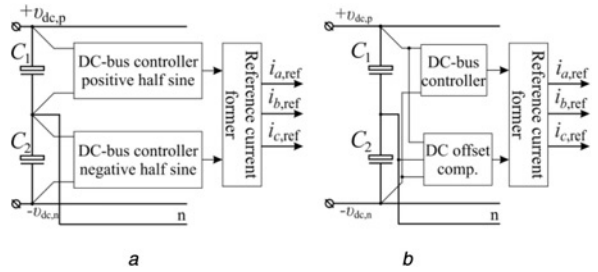

Fig. 4 *Midpoint stabilisation*
(a) By using split dc-bus controller, ***(b)*** By offsetting the reference currents

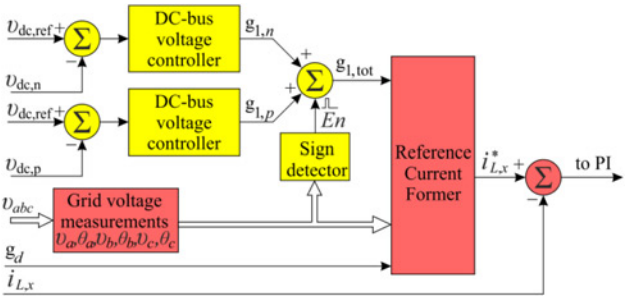

Fig. 5 *Block diagram of the split dc-bus controller*

magnitudes and phase angles, are used to calculate the magnitude of the reference currents. Index 'x' represents the respective reference phase current. The rest of the control algorithm is the same as shown in Fig. 3.

From (2) and (7), it can be seen that the power balance depends on the rms value of the grid voltage V_{rms}. Therefore, the open-loop transfer function for each controller will be the same as (8) and (9).

3.2 Reference current offset

The second solution is proposed in Fig. 4*b* and a simplified block diagram is shown in Fig. 6. This algorithm uses only one dc-bus voltage controller to ensure the power balance between dc and ac side and a second controller that maintains the difference between v_{C1} and v_{C2} to be zero. If, for example, $v_{C1} > v_{C2}$, then the midpoint offset controller will add a small positive offset to all reference currents and the voltage difference will be restored to zero.

The mathematical expression can be written as:

$$3i_{comp} = 4C_{dc}\frac{\mathrm{d}v_{dc}}{\mathrm{d}t} \tag{10}$$

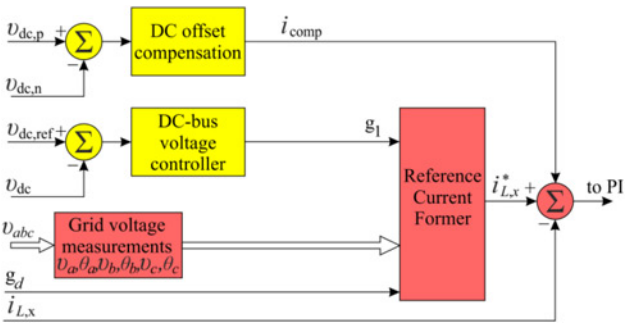

Fig. 6 *Midpoint stabilisation by offsetting the reference currents*

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where i_{comp} is the needed offset current. Then taking into account the difference between the capacitor voltages, $\Delta v_{dc} = v_{C1} - v_{C2}$ yields to:

$$\frac{d\Delta v_{dc}}{dt} = -2\frac{dv_{dc}}{dt} \tag{11}$$

The open-loop transfer function can now be derived:

$$\frac{\Delta v_{dc}}{i_{comp}} = -\frac{3I_{ref}}{2sC_{dc}V_{dc,ref}} = \frac{-1}{\tau s} \tag{12}$$

This leads to the same transfer function as (8), but the time constant is different as well as the sampling frequency which is 20 kHz. It is assumed that current controllers are working perfectly such that the measured current tracks the reference current perfectly.

4 Experimental validation

The experimental validation of the proposed control algorithms for midpoint balancing is presented in Fig. 7.

The three-phase four-wire inverter is connected to a three-phase programmable voltage source via a power analyser and a cable. More information about the setup parameters can be found in Table 1. The programmable voltage source is able to deliver asymmetrical voltages which forces the three-phase damping control strategy to inject asymmetrical currents. The proportional and integral coefficients used for the PI controllers used in the set-up are listed in Table 2.

The measured waveforms of the phase voltages and the dc-bus voltages at the inverter terminals are shown in Fig. 8. As can be seen, the positive and negative dc-bus voltages are relatively smooth, despite the injected asymmetrical currents which are

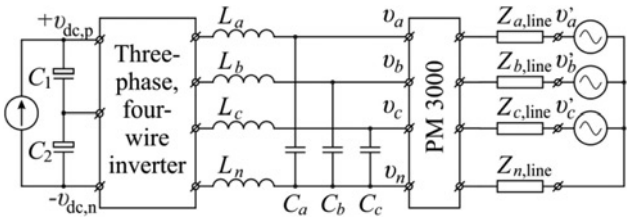

Fig. 7 *Configuration of the test set-up*

Table 1 Test set-up parameters

Parameter	Value
v'_a, v'_b, v'_c	100 V, 110 V, 110 V (50 Hz)
$Z_{a,line}$, $Z_{b,line}$, $Z_{c,line}$, and $Z_{n,line}$	(0.470 + j0.201) Ω
power analyser	PM3000
C_a, C_b, and C_c	5 μF
L_a, L_b, and L_c	2 mH
L_n	0.666 mH
three-phase inverter	1.8 kVA
C_1 and C_2	2000 μF
$v_{dc,p} + v_{dc,n}$	400 V
switching frequency	20 kHz

Table 2 PI controller values used in the set-up

Controller	Parameter
split dc-bus controller	
dc-bus controller 1	$P = 3.48$, $I = 0.95$
dc-bus controller 2	$P = 3.48$, $I = 0.95$
reference current offset	
dc-bus controller 1	$P = 7.48$, $I = 0.96$
offset controller	$P = 1.07$, $I = 0.91$

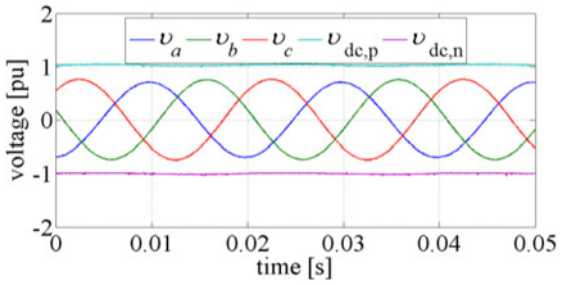

Fig. 8 *Phase voltages and dc-bus voltages ant the inverter terminals*

depicted in Fig. 8. This implies that the 100 Hz component at the dc level does not introduce any additional error concerning the correctness of the dc-bus controller sampling. Note that the spikes in the phase current are due to oscilloscope aliasing problems (Fig. 9). The asymmetrical current injection leads to a neutral current with the rms value of 2 A. The waveforms of the voltages and the currents are identical when both algorithms for stabilising the midpoint are used because they are tested under the same conditions.

Waveforms of the input conductance signals $g_{1,tot}$, when two dc-bus controllers are used, are presented in Fig. 10. The three

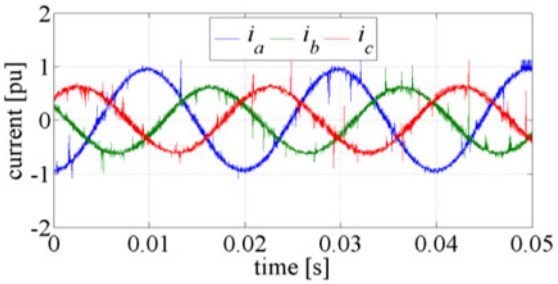

Fig. 9 *Injected phase currents by the inverter*

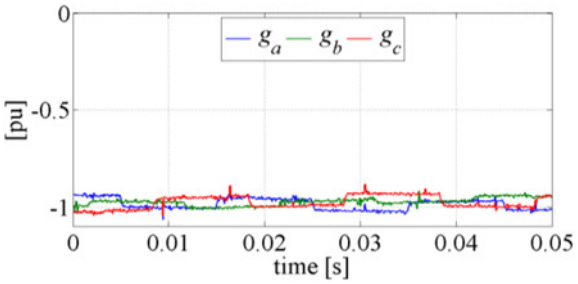

Fig. 10 *Input conductance when two dc-bus controllers are used*

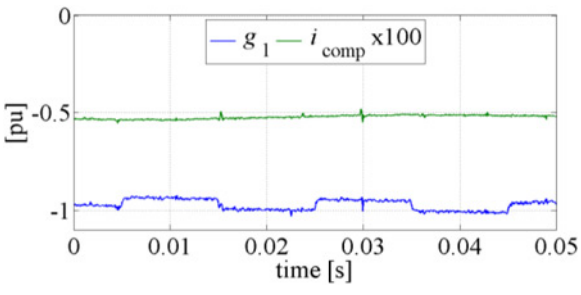

Fig. 11 *Input conductance and compensation current waveforms when reference current offset is used*

Table 3 Obtained measurements under unbalanced current injection

Parameter	Split dc-bus controller			Reference current offset			Std[a]
	a	*b*	*c*	*a*	*b*	*c*	
V_{rms}, V	104.5	112.0	111.8	104.5	112.0	111.8	—
PF	0.999	0.997	0.997	0.999	0.997	0.996	—
I_{rms}, A	6.95	4.381	4.483	6.948	4.387	4.474	—
THD, %	1.6	2.5	2.7	2.6	2.7	3.1	5%
H1, A	6.952	4.391	4.477	6.943	4.389	4.469	16.0
H2, A	0.100	0.071	0.086	0.096	0.070	0.084	1.08
H3, A	0.01	0.011	0.01	0.012	0.014	0.014	2.3
H4, A	0.006	0.007	0.006	0.003	0.001	0.001	0.43
H5, A	0.012	0.009	0.007	0.011	0.012	0.012	1.14
I_n, A		2.018			2.043		—
I_{dc}, A	−0.04	0.02	0.02	−0.02	0.02	0.01	$0.01I_{nom}$

a IEC 61000-3-2 [10].

signals g_a, g_b, and g_c represent the assembled signal after summing signals $g_{1,n}+g_{1,p}$ and updated when a zero-crossing occurs of the respective phase voltage.

Waveforms of the input conductance g_1 and the compensating current i_{comp} needed for the reference current offset are depicted in Fig. 11. For better visualisation, the compensating current is multiplied with a factor of 100.

From the obtained experimental measurements listed in Table 3, it can be seen that the rms values of the phase voltages, phase currents, neutral current, and the power factors are almost equal when comparing the two algorithms. Although the reference current algorithm injects a slightly higher neutral current, the performance of both algorithms is very similar.

The harmonic content of the injected currents is also similar. Total harmonic distortion (THD) is slightly better when the split dc-bus controller is used, but overall both algorithms manage to keep the THD below 5% as required by the standard IEC 61000-3-2 [10]. The main difference between the proposed algorithms is that the split dc-bus injects a slightly higher magnitude of even harmonics, but overall the performance of both algorithms is very similar. Both algorithms are studied up to the fifth harmonic because the higher order current harmonics have insignificant contribution to the THD of the injected currents.

In Table 3, the IEC 61000-3-2 limit values for harmonic currents [10] are compared with the measured values it was found out to be lower in order of magnitude.

The last comparison is related to the injection of a dc current. According to [10], the injection of the dc current must be limited to 1% of the nominal current of the inverter. The nominal inverter current is 5.1 A (in the case of balanced conditions) and the absolute value of the dc current injection from both algorithms does not exceed 40 mA which is an excellent key performance indicator.

5 Conclusions

Two different control algorithms for stabilising the midpoint voltage of a three-phase four-wire inverter with split dc-bus capacitor are proposed. Both algorithms were analysed and the performance then validated against the same conditions in a controllable experimental environment. It was found that both algorithms are able to maintain the midpoint potential stable while the quality of the injected currents is kept within the limits set by IEC 61000-3-2 [10].

6 Acknowledgment

This work was supported by EC-FP7 project 'INCREASE' with Grant agreement: 608998.

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