DEVELOPMENT OF A SYNCHRONOUS GALVANICALLY ISOLATED MEASURING SYSTEM

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Dissertation submitted in partial fulfilment of the requirements for the degree Magister Engineriae at the North West University (Potchefstroom Campus)

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Potchefstroom

2005

Abstract

Perhaps the most useful area of electronic engineering involves the gathering and manipulation of data from an industrial process or a scientific experiment. The industrial process can be electrical, mechanical, thermo dynamical, or combinations thereof. Once data are collected from the process, modelling, parameter estimation, condition monitoring and fault detection can be done on the system. Data acquisition devices are used to capture the needed data. These devices are usually purchased off-the-shelf but custom-made systems are designed when commercially available systems fall short.

The purpose of this project is to develop a custom-made measuring system. This system must generate and acquire waveforms at multiple points synchronously. Intended applications include input-output mapping and determining the transfer function of a process. This system should be a less costly alternative to commercially available systems, flexible and user-friendly. In addition, the system should be able to take high speed high resolution measurements and should have superior galvanic isolation.

A complete measuring system capable of signal injection and data acquisition was developed. Hardware, firmware and software were developed by following a simple systems engineering approach. The system was tested to close the engineering design loop. Although a 16-bit data acquisition system requires high precision instruments for testing, simpler tests were designed to test certain aspects of the system. These tests proved to be sufficient to illustrate the concept of a synchronous, multi-node, galvanic isolated measurement system.

This project was done, based on a requirement in the industry. The requirement was to have a low-cost high accuracy, high speed, galvanic isolated, synchronous measurement system to inject signals into a system and to measure signals in a system. Many off-the-shelf systems exist, but are either too complex for the intended purpose or costly. The solution to this problem was to develop a low cost measuring system that could accomplish tasks such as input-output mapping at multiple points.

Uittreksel

Die insameling en manipulasie van data vanaf 'n industriële proses of wetenskaplike eksperiment is een van die nuttigste toepassings in die veld van elektroniese ingenieurswese. Hierdie industriële proses kan elektries, meganies, termodinamies of kombinasies hiervan wees. Wanneer data vanaf die proses verkry word, kan modellering, parameter benadering, kondisie monitering en foutdeteksie op die stelsel gedoen word. Data versameling toestelle word gebruik om hierdie fisiese data te verkry. Toestelle vir data versameling word gewoonlik van die rak af gekoop maar wanneer hierdie stelsels onvoldoende is kan 'n unieke stelsel ontwerp word om die probleem op te los.

Die doel van hierdie projek is om 'n meetstelsel te ontwikkel wat golfvorms kan genereer en meet by veelvuldige punte. Hierdie stelsel moet 'n goedkoper alternatief tot kommersiële stelsels bied, meer buigsaam en ook gebruiker vriendelik wees. Hoë spoed hoë resolusie sinkrone metings by multi punte moet deur die stelsel geneem kan word en die stelsel moet galvanies geïsoleer wees.

'n Stelselingenieurswese benadering is gevolg om die hardeware en sagteware vir die stelsel te ontwerp. Na afloop van die ontwerp is toetse gedoen om die ontwerplus te voltooi. Eenvoudiger toetse is ontwerp om die stelsel te toets aangesien hierdie 'n 16-bis stelsel is en hoë presisie instrumente nodig is om so 'n stelsel te toets. Hierdie toetse was voldoende om die konsep van 'n sinkrone, multi punt, galvanies geïsoleerde meetstelsel te illustreer.

Hierdie projek is gedoen omdat daar 'n behoefte in die industrie vir so 'n stelsel is. Die behoefte is 'n lae koste, hoë akkuraatheid, hoë spoed, galvanies geïsoleerde, sinkrone meetstelsel wat golfvorms kan aftas en golfvorms kan genereer. Baie stelsels kan van die rak af gekoop word maar is of te ingewikkeld of te duur vir die spesifieke doel. Die oplossing vir die probleem is om 'n lae koste meetstelsel te ontwikkel wat take soos die bepaling van inset-uitset verwantskappe kan verrig.

Acknowledgements

First of all, I would like to thank my Creator, our Heavenly Father, for the privilege, strength, ability and perseverance He has granted me to complete this study.

I would like to thank the PBMR for the financial support they provided and Dr. Dirk Ackermann, my study leader, for his encouraging support, constructive criticism and professional guidance. A special word of thanks to Prof. J.E.W. Holm for his inputs regarding product development and product documentation.

Thank you to Mrs. Braun for proof reading this dissertation and suggesting corrections to improve the quality of the text.

On the personal side, I would like to thank my friend Arnold Helling for his academic and non-academic inputs and my parents for their continuous motivation, moral and financial support.

My most heart-felt thanks of all goes to my wonderful fiancée Thercia de Klerk for her love, eternal patience and support.

Valuable quality time was sometimes sacrificed so that this study could be finished. To everyone who had part in this study, I wish to convey my warmest thanks.

"If we knew what it was we were doing, it would not be called research, would it?"

- Albert Einstein

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Abbreviations

ADC	Analogue-to-Digital Converter
BER	Bit Error Ratio
CANbus	Controller Area Network Bus
CMRR	Common Mode Rejection Ratio
CPLD	Complex Programmable Logic Device
DAC	Digital-to-Analogue Converter
DAQ	Data Acquisition
DCG	Digital Clock Generator
DIP	Dual-in-line Package
DNL	Differential Non-Linearity
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
FPGA	Field Programmable Gate Array
HOQ	House Of Quality
I^2C	Inter-Integrated Circuit
ILD	Injection Laser Diode
INL	Integral Non-Linearity
I/O	Input/Output
ISO	International Organization for Standardization
KSPS	Kilo Samples Per Second
LED	Light Emitting Diode
LSB	Least Significant Bit
MB	Megabyte
MCU	Microcontroller Unit
OSI	Open Systems Interconnect
PC	Personal Computer
PCI	Peripheral Control Interconnect
PLCC	Plastic Leaded Chip Carrier
PPI	Peripheral Port Interface
PPM	Parts Per Million
QFD	Quality Function Deployment
RAM	Random Access Memory

SBC	Single Board Computer
SDRAM	Synchronous DRAM
SFDR	Spurious Free Dynamic Range
SINAD	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SOIC	Small Outline Integrated Circuit
SOT	Small Outline Transistor
SPI	Serial Peripheral Interface
SSOP	Shrinked Small Outline Package
SUT	System Under Test
TCP/IP	Transmission Control Protocol / Internet Protocol
TCXO	Temperature Compensated Crystal Oscillator
VCSEL	Vertical Cavity Surface-Emitting Laser

Chapter 1

Introduction

Several applications of electronic engineering such as modelling, parameter estimation, condition monitoring, and fault detection require numerical data as input. These numerical data are obtained by means of a measurement system. A wide variety of commercial measurement systems are available on the market but sometimes these systems lack the critical specifications as required by a specific application. This scenario requires the development of a customized measurement system in order to address these shortcomings.

1.1 Engineering Applications

This section discusses some of the applications in electronic engineering which are dependent on numerical data. A measurement system is required to obtain the data from a physical process.

1.1.1 Modelling

In the engineering field it is often necessary to construct, test and use a mathematical model of a physical process [1]. Models can be classified according to their purpose. In the first category are models to assist plant design and operation. This category comprises detailed, physically based models to assist in assessing plant dimensions and other basic parameters. The second category consists of models to assist control system design and operation.

In order to derive a model, experimental data in the time domain are necessary. These data can be used for modelling multiple-input multiple-output systems. It is possible to model these systems by applying deterministic signals to determine the step, ramp or sinusoidal responses.

1.1.2 Parameter estimation

Parameter estimation is a common problem in many areas of process modelling, both in on-line applications such as real time optimization and in off-line applications such as the modelling of reaction kinetics and phase equilibrium. The goal is to determine values of model parameters that provide the best fit to measured data, generally based on some type of least squares or

maximum likelihood criterion. In the most general case, this requires the solution of a nonlinear and frequently nonconvex optimization problem.

For example, to perform stability studies and post mortem analysis of power systems, the operational parameters of generators can be determined as proposed in [2]. Another example is determining the parameters of a power transformer. When these parameters are known, an analytical model can be used to estimate the hottest-spot temperature in a transformer when direct measurement is not possible [3]. Transmission lines can be protected by implementing a fault impedance estimation algorithm [4]. In all these instances system data must be acquired by means of a measurement system before parameters can be estimated.

1.1.3 Condition monitoring

Condition monitoring is the measurement, recording and analysis of machine parameters (such as acceleration) to determine machine health. The current condition of the machine is compared to original conditions. Condition monitoring is necessary to achieve efficient and profitable operation of industrial processes. The tight requirements of modern electrical machines and drives necessitate the application of real-time condition-monitoring systems. The system is monitored continually under all operating conditions. Condition-monitoring devices can provide extremely useful detailed information on the state of the machine and drive for both the operator and designer of the machine. Different forms of condition-monitoring are used for induction machines and synchronous machines [5].

An example of condition monitoring is the monitoring of the rotor-stator contacts of a turbine generator. Continuous rubbing between the shaft and surrounding seals or end-glands of turbine generator units can escalate into very severe vibration and result in costly rotor damage. These rotor–stator contacts require early diagnosis of error conditions so as to minimize the financial consequences of any unplanned shutdowns [6].

1.1.4 Fault detection

Fault detection is a model-based task that involves comparison of the observed behaviour of the process to a reference model representing fault-free behaviour, and detecting significant differences. Fault detection methods are defined by the model used to detect deviation from the normal model as in [7]. No information concerning failure modes and effects is required in the fault detection step. Certain features such as general operating conditions and product quality measurements are used to detect faults. For example, damage to large power transformers can be minimized by taking the transformer out of service as soon as a fault is detected [8]. A fault

condition can be detected by monitoring the three-phase voltages and currents. Various fault detection methods are discussed in [9].

Data acquired in a distributed and synchronized manner are required in a variety of applications, for example, in a hot strip mill that creates a long steel coil starting from a slab of steel. In this process the distance between the beginning and end of the mill exceeds 300 meters. This defines the need for a distributed data acquisition system. Another important requirement is that the measurements should be synchronized in order to determine the mill performance in snapshots [10].

Other applications requiring a distributed synchronous data acquisition system include:

- Cold steel rolling mills
- Continuous pickle lines
- Temper steel rolling mills
- Continuous steel casting
- Electric resistance weld manufacturing processes
- Seamless steel pipe mills
- Pulp and paper mills
- Web printing press
- Continuous aluminium casting
- Aluminium rolling mills.

1.2 Measurements and Error

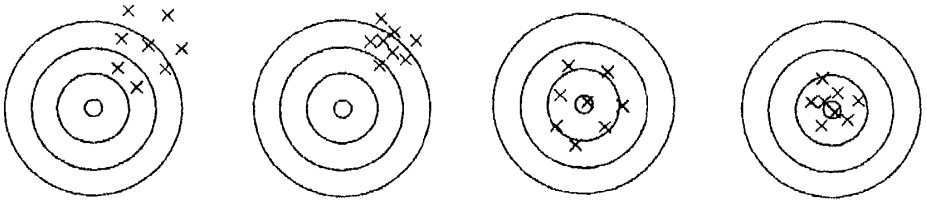
System modelling, parameter estimation, condition monitoring and fault detection all require experimental data of a physical system. A measurement system is necessary to acquire data for further application. In order to understand the measurement system, the measurement process must be understood. No discussion of measurement instruments is complete without discussing basic measurement science [11] and measurement errors beforehand.

Measurement involves using an instrument to determine the magnitude of a quantity or variable. At times our unaided human faculties are incapable of measuring a quantity, and an instrument is necessary to serve as an extension of our senses. Thus, an instrument may be defined as a device for determining the value or magnitude of a quantity or variable.

Among all instruments, electronic instruments are the most widely used in the engineering field to determine variable quantities such as voltage, current, pressure, temperature, light intensity, speed, acceleration etc. In order to use these instruments intelligently, it is important to understand their operation and the fundamental principles of measurement science.

1.2.1 Accuracy and precision

Two fundamental concepts in measurement science are accuracy and precision . The accuracy of a measurement refers to how close this measurement comes to the true value. Therefore it indicates the correctness of the result. Precision indicates the reproducibility of the measurements. Given a constant value, precision is a measure of the difference in successive measurements. The precision of a measurement does not guarantee its accuracy and good measurement technique demands continuous scepticism as to the accuracy of these results. Optimal accuracy is achieved by comparing the instrument to a known standard value, a process called calibration.



Poor accuracy **Poor accuracy** **Good accuracy** **Good accuracy**
Poor precision **Good precision** **Poor precision** **Good precision**

Figure 1.1 : Accuracy and precision.

When acquiring data, every effort should be made to increase the accuracy and precision of the measured data since this affects the quality of the data. The accuracy of a data acquisition system is limited by calibration errors and the precision is limited by the resolution of the analogue to digital converter. Even if great care is taken to maximize accuracy and precision, it is still impossible to get a perfect measurement. This is because every measurement is subject to inaccuracies and errors.

1.2.2 Types of errors

Since it is impossible to achieve perfect accuracy, it is important to determine the accuracy and to identify the errors that entered the measurement process. The errors can be divided into three categories namely gross errors, systematic errors and random errors. Gross errors are caused mainly by the human operator and systematic errors by the instrument.

These errors can be minimized or even eliminated by taking more than one reading and by calibrating the instrument. Random errors are more difficult to manage since they are caused by random variations of the variable or in the environment. The only way to reduce these errors is to increase the number of measurements and to use statistical tools to determine the true value of the quantity.

Statistical analysis includes parameters like arithmetic mean, deviation from mean, average deviation and standard deviation to determine the uncertainty of the final result. By increasing the number of measurements and decreasing the increments, a histogram showing the frequency of occurrence can be plotted. As the measurements increase to infinity, the histogram will usually become a Gaussian curve [12].

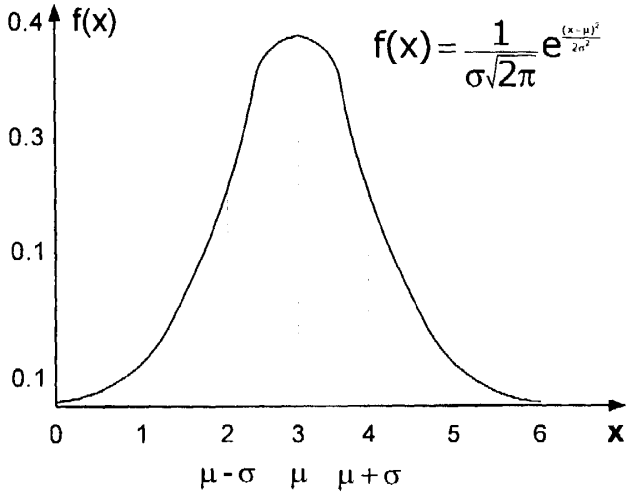


Figure 1.2 : The normal distribution

The following qualitative statements are based on the Normal law [13]:

- All observations include small disturbing effects called random errors.
- Random errors can be positive or negative.
- There is an equal probability of positive and negative random errors.

Therefore it can be expected that the measurements include an equal number of plus and minus errors. This will cause the total error to be small and the mean value will approach the true value of the measured variable.

The form of the error distribution curve dictates the following possibilities:

- Small errors are more probable than large errors.
- Large errors are very improbable.
- An equal probability of plus and minus errors exists, thus the probability of a given error will be symmetrical about the mean value.

Although a perfect measurement does not exist, it is still possible to minimize or even eliminate gross and systematic errors by refining the measurement process. The only errors left will be random errors, which will be present even in perfect experimental setups.

When using any measuring instrument or data acquisition system, it is important to keep the fundamental concepts of measurement science in mind in order to make a meaningful interpretation of the data. In the next section a discussion relating these concepts to data acquisition systems follows.

1.3 Data acquisition systems

Effective modelling, parameter estimation, condition monitoring and fault detection rely on accurate and reliable data from the system under test. The system under test usually generates multiple responses after being excited by a single stimulus as illustrated in Figure 1.3.

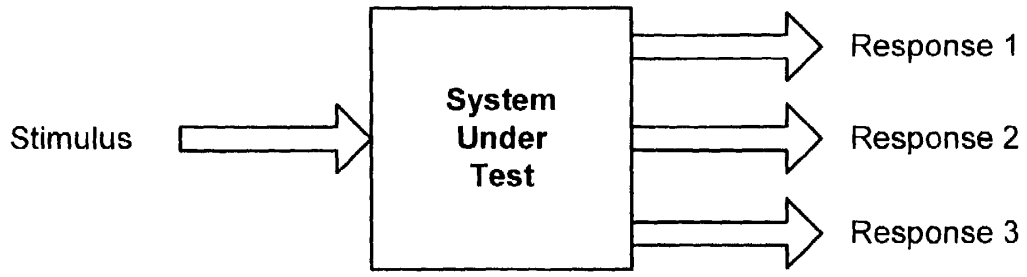


Figure 1.3 : Single input multiple output system

The data acquisition system is the link between the physical system and the mathematical model of the system. Data obtained through the data acquisition process directly affect the quality of the derived mathematical model.

Usually a data acquisition card is used to convert an analogue signal to digital format. The data acquisition card provides single-ended or differential inputs followed by amplification and filtering circuitry. Voltage ranges of the data acquisition card can be configured to accept and convert measurements more accurately. The gain stage buffers and conditions the input signal to ensure optimal dynamic range. After the input signal is amplified and filtered, it is sampled by the ADC. These digital values are logged, processed or displayed by the personal computer.

1.3.1 Transducer interfacing

Data acquisition systems need to get real-world signals into the computer for further processing. These signals come from a diverse range of instruments and sensors. Current is often used to transmit signals in noisy environments because it is much less affected by electromagnetic induced noise. The next section briefly explains some aspects regarding the 4-20 mA current-loop.

1.3.2 The 4-20 mA current-loop

Transmitting sensor information via a current loop [14], [15], [16] is particularly useful when the information has to be sent to a remote location up to three hundred meters away. The loop operates by converting the sensor's output voltage to a proportional current between 4 mA and 20 mA. This current signal is converted back to a voltage signal at the receiving endpoint. An ADC at the receiver converts the analogue voltage signal to digital for further processing by a computer or process controller.

However, transmitting a sensor's output as a voltage over long distances has several drawbacks. Unless very high input-impedance devices are used, transmitting voltages over long distances produces correspondingly lower voltages at the receiving end due to wiring and interconnect resistances and subsequent voltage drops. High-impedance instruments can be sensitive to noise pickup since the lengthy signal-carrying wires often run in close proximity to wiring with high electromagnetic radiation. Shielded wires can be used to minimize this noise pickup, but their high cost may be prohibitive when long distances are involved.

Sending a current over long distances produces voltage losses proportional to the conductor's resistance. However, these voltage losses, also known as loop drops, do not reduce the 4-20 mA current as long as the transmitter and loop supply can compensate for these drops. The magnitude of the current in the loop is not affected by voltage drops in the system wiring since the current is the same at all points.

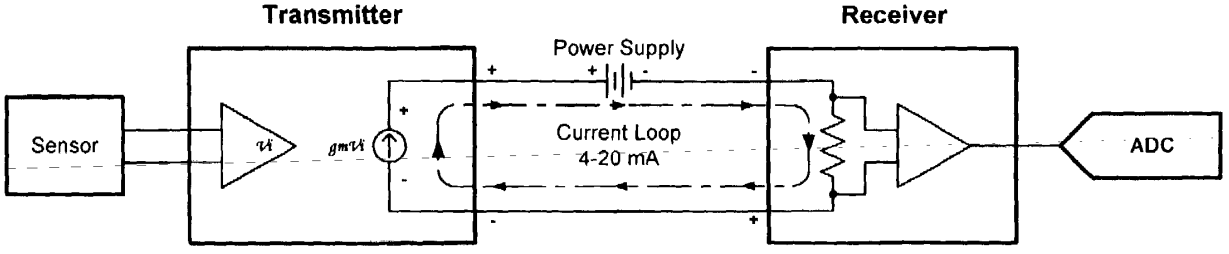


Figure 1.4 : Typical current loop

The 4-20 mA current-loop consists of four elements: a sensor; a voltage to current converter; a loop power supply; and a receiver. In loop powered applications these four elements are connected in series in a closed loop.

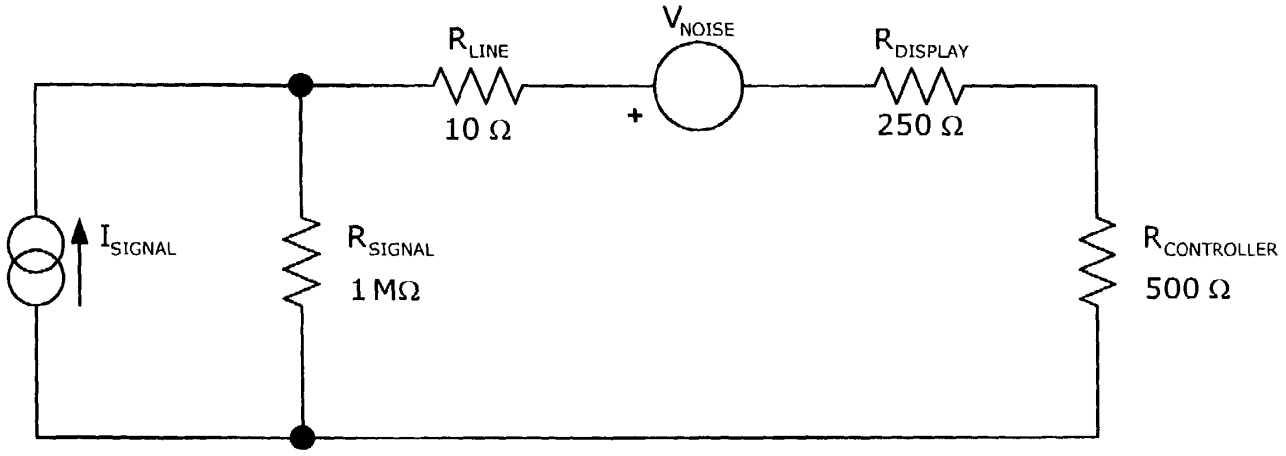


Figure 1.5 : Schematic of a current loop

A simplified current loop is shown schematically in Figure 1.5. The 4-20 mA transmitter is modelled by an ideal Norton current source composed of I_{SIGNAL} and R_{SIGNAL}. Line resistance is represented by R_{LINE} and random induced loop noise by V_{NOISE}. In this example a 500 Ω controller and a 250 Ω digital display are connected in series with the signal current. The loop is powered by a 24 V power supply.

Several advantages of this type of current loop are as follows:

- Signal voltage at any load is given by

$$V_{SIGNAL} = I_{SIGNAL} \times R_{LOAD} \tag{1.1}$$

  which is independent of supply voltage variations and line resistance.

- Random induced loop noise voltage at any load is given by

$$V_{LOOP\ NOISE} = V_{NOISE} \times \left(\frac{R_{LOAD}}{\sum R_{LOADS} + R_{LINE} + R_{SIGNAL}} \right) \tag{1.2}$$

  The loop noise at a load is reduced by the factor in brackets.

- At any load the supply variations are also reduced by the bracketed factor.
- Another advantage of the current loop transmitter is that multiple loads can be connected in series. This provides considerable control and display opportunities.

Sensors provide an output voltage whose value represents the physical parameter being measured. The transmitter amplifies and conditions the sensor's output, and then converts this voltage to a proportional 4-20 mA direct current signal that circulates within the closed series loop. The receiver, which is normally a subsection of a data acquisition system, converts the 4-20 mA current back into a voltage which can be processed further.

The full scale range of the current signal is normally either 0-20 mA or 4-20 mA. A 4-20 mA signal has the advantage that even at minimum signal value there should be a detectable current flowing. The absence of this current indicates a wiring problem.

Before analogue-to-digital conversion, the current signals are usually converted to voltage signals by a current-sensing resistor. The resistor should be of high precision and should match the signal to an input range of the analogue input hardware. For 4-20 mA signals a 50 ohm resistor will give a voltage of 200 mV to 1 V.

Equation 1.3 shows the relationship between thermal noise and resistance of a conductor. Thermal noise (also called Johnson noise or resistor noise) is inherently present in all systems operating at temperatures above absolute zero (0K or -273°C). In order to minimize thermal noise, the resistance should be kept as low as possible.

$$V_{noise}(rms) = \sqrt{4kTRB} \tag{1.3}$$

Where

V_{noise} is the generated noise voltage in Volts

k is Boltzmann's constant

T is the absolute temperature in Kelvin

R is the resistance in ohms

B is the bandwidth in Hertz.

An instrumentation amplifier is used to convert the differential voltage from the current-sensing resistor to a single-ended voltage to be converted to digital format by an ADC. Amplifiers boost the level of the input signal to match the range of the ADC, thus increasing the resolution and sensitivity of the measurement.

1.3.3 Single-ended and differential inputs

Two types of inputs are encountered in practice, the single-ended input and the differential input. With single-ended inputs, one conductor from each signal source is connected to the data acquisition interface. The measurement is the difference between the signal and the ground. This method relies on the signal source being grounded, and the signal source and data acquisition interface sharing the same ground. The problem with single-ended inputs is that they are sensitive to noise errors and that ground loops can occur since the ground level varies. When two grounds at different potentials are connected, large currents can flow, known as ground loops [17].

The ground loop problem is shown in Figure 1.6. Both the transmitter and receiver need to be earthed at the installed location for personnel safety purposes. Usually the transmitter and receiver are a few meters apart or even in different buildings. This difference in location causes a difference in ground potential. Because of the potential difference, a current will flow between these two points. The earth represents itself as a resistor between these two points, thus the ground current would be proportional to the potential difference and inversely proportional to the earth resistance.

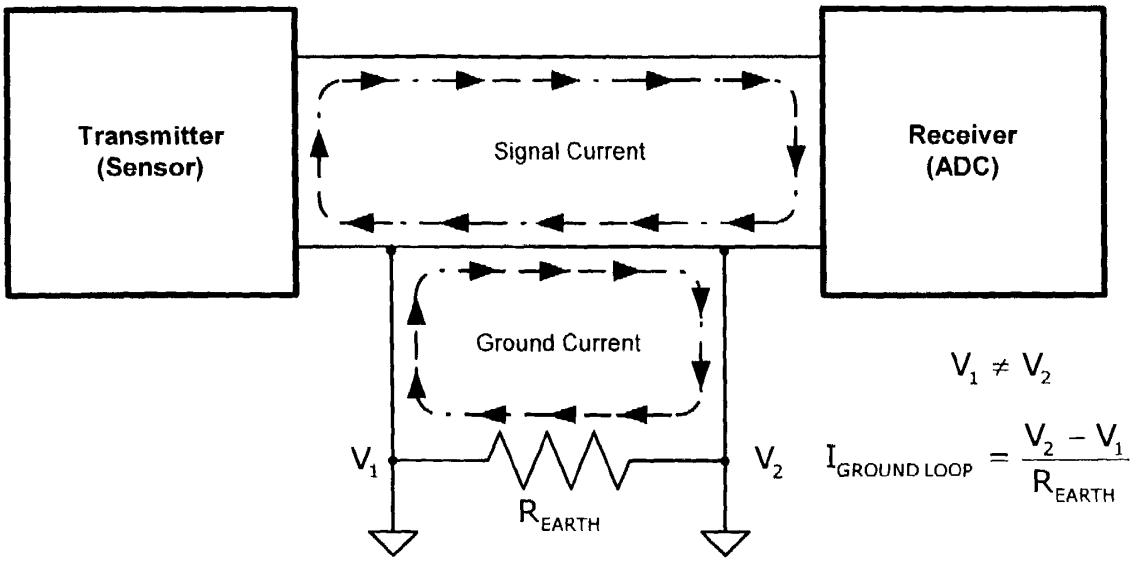


Figure 1.6 : Ground loop

A differential input measures the voltage between two input lines. Two input channels per device are required but this setup has two advantages compared to single-ended inputs. Firstly, differential inputs can measure signals from floating signal sources. Differential inputs will also cancel common mode noise or interference. Interference and noise caused by electric motors, power supply lines or other electrical sources can be rejected by measuring the differential

voltage. By measuring the difference between the two inputs, the external noise that is common to both inputs can be eliminated.

In general, a differential measurement system is preferable because it rejects the ground loop induced errors and the noise picked up in the environment. Common mode noise is rejected optimally by twisting the two conductors together, thereby ensuring that the noise picked up will be the same for each conductor. The effect of the difference in ground potential is reduced by direct current isolation between the transmitter and receiver. Single-ended configurations, on the other hand, provide twice as many measurement channels, but are only appropriate if the magnitude of the induced errors is smaller than the required accuracy of the data.

The differential input single-ended output instrumentation amplifier is used when differential inputs are required. This amplifier is used for precision amplification of differential dc or ac signals while rejecting large values of common mode noise. The next section gives a brief overview of the instrumentation amplifier.

1.3.4 Instrumentation amplifier

A circuit diagram of the instrumentation amplifier [18] is shown in Figure 1.7. This amplifier consists of three operational amplifiers: two voltage followers driving a balanced differential amplifier. Voltage followers provide high input impedance so it can be used with high output impedance sources such as sensors. Gain and common mode voltage rejection is provided by the balanced differential amplifier stage.

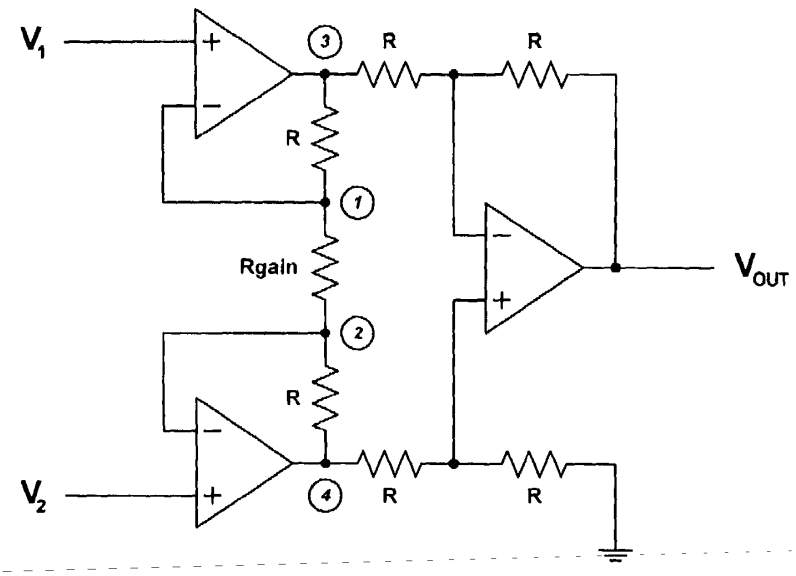


Figure 1.7 : Internal circuit of instrumentation amplifier

Ideally any voltage common to both inputs is cancelled. In practice the external resistors of the two input amplifiers are not perfectly matched so a fraction of the common mode voltage may appear. The common mode rejection ratio (CMRR) improves if the R resistors are matched closely. The CMRR is defined as the ratio of the common-mode interference voltage at the input of a circuit, to the corresponding interference voltage at the output and is usually given in decibels.

Another important specification is the input range. This is the absolute voltage level allowed before saturation occurs. The hardware operating range may be wider than the input range, but the operating range just guarantees that the hardware will not be damaged; it does not guarantee proper operation. Essentially, the instrumentation amplifier converts a differential-signal to an amplified single-ended signal. In addition, the instrumentation amplifier provides common-mode rejection.

1.3.5 Compensating for measurement errors

The result of any measurement is only an approximate estimate of the "real" value being measured. In truth, the real value can never be measured perfectly because there is always some physical limit to how well the measurement can be represented. The accuracy of a measurement refers to this limit.

Over a given range, a 16-bit ADC has 65 536 choices for a measurement, while a 12-bit ADC has 4096 choices. Ideally these choices distribute evenly across the entire measurement range, and the measurement hardware rounds the actual measurement value to the nearest choice. This rounding error, commonly called the quantization error, is often considered the only factor in accuracy. Actually, quantization error accounts for just about 35% of the total measurement error in a 12-bit ADC and only a negligible percentage in a similar 16-bit ADC. Whether a 12-bit or 16-bit ADC is used, more than just the quantization error must be considered.

Imperfections in the amplifier, such as resistor tolerances and the ADC characteristics, cause gain errors. These errors are usually specified as a percentage of the reading. To compensate for these errors, an internal calibration should be performed to compensate for gain errors as well as for changes in temperature. This calibration procedure requires an onboard reference source which is insensitive to temperature drift.

Imperfections in the amplifier or the ADC cause nonlinearity errors. A small variation in gain across the input range causes nonlinearity. This type of error is usually specified as a

percentage of full-scale range. Currently, there is no easy calibration method to compensate for nonlinearity error. The relative accuracy of the data acquisition system will indicate the amount of nonlinear error. Relative accuracy is defined as a measure in least significant bits (LSB) of the accuracy of the data acquisition system. It includes all nonlinearity and quantization errors. It does not include offset and gain errors but by knowing the relative accuracy, a tolerance can be established in each reading.

To improve the accuracy of measurements further, offset errors must also be compensated. Offset errors are constant across the input range and are therefore relatively easy to correct. A short-circuited channel can be read to measure the offset error. This value should then be subtracted from all subsequent readings.

Averaging is a good software technique used to improve the accuracy of readings. The premise of averaging is that noise and measurement errors are random in nature. Therefore, by the Central Limit Theorem, the error will have a normal (Gaussian) distribution. By collecting multiple points, the resulting distribution is Gaussian. The mean value, which is statistically close to the actual value, can now be calculated. The standard deviation from the average will be smaller if more points are taken in the average. Averaging should be avoided when working with high frequency signals or when the source of error is not random in nature.

1.4 Sources of noise

There are four principal sources of noise [19] coupling mechanisms as shown in Figure 1.8. These sources are conductive, capacitive, inductive and radiative. When currents from different circuits are shared by a common impedance, conductive coupling occurs. Time-varying electric fields in the vicinity of the signal path cause capacitive coupling. Inductive coupled noise results from time-varying magnetic fields in the area enclosed by the signal circuit. When the source of the electromagnetic field is far from the signal circuit, the electric and magnetic field couplings are considered combined electromagnetic or radiative coupling.

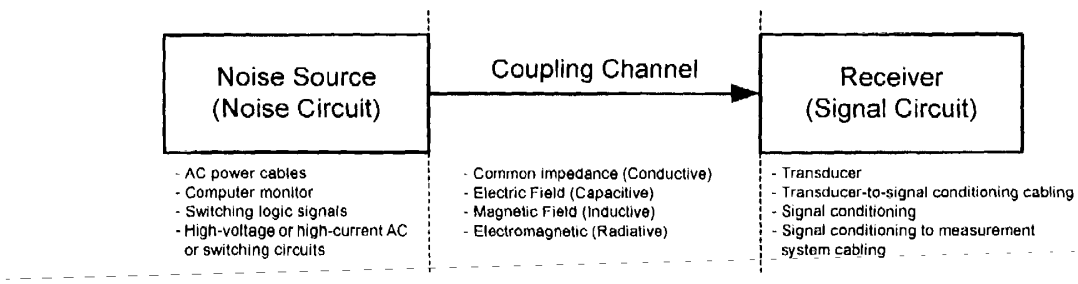


Figure 1.8 : Noise coupling

Conductively coupled noise exists because wiring conductors have finite impedance. Conductive coupling can be minimized by breaking ground loops and providing separate ground returns for both low-level and high-level, high-power signals.

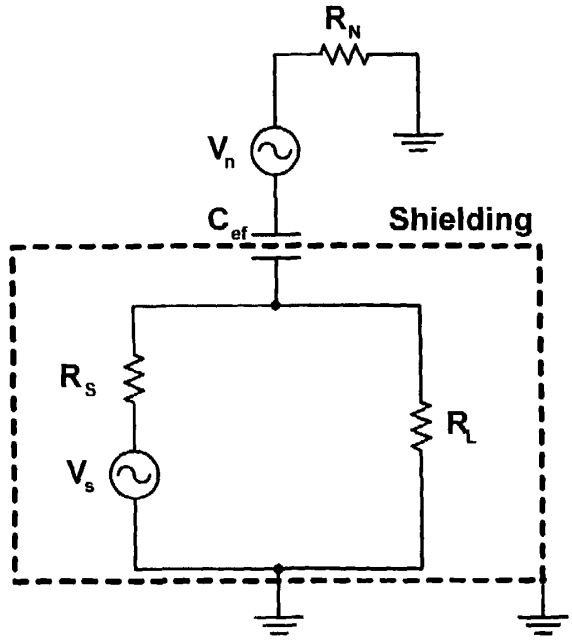


Figure 1.9 : Capacitive Coupling between Noise Source and Signal Circuit

Figure 1.9 shows the equivalent circuit for capacitive coupling. The dotted rectangle depicts shielding. This circuit consists of two parts; the noise circuit and the signal circuit. The electric field coupling is modelled as a capacitance between the two circuits. The equivalent capacitance C_{ef} is directly proportional to the overlapping area and inversely proportional to the distance between the noise circuit and signal circuit. Thus, the noise caused by capacitive coupling can be reduced by minimizing the overlap or by increasing the separation distance. The capacitance can also be reduced by using capacitive shielding [20]. When the circuit is shielded, the noise voltage is induced into the shield surrounding the signal circuit, instead of onto the conductors.

Inductive coupling is illustrated in Figure 1.10. Inductive coupling results from time-varying magnetic fields in the area enclosed by the signal circuit loop. Currents in nearby noise circuits cause this magnetic fields which induces a voltage in the signal circuit.

According to Faraday's law [21], the voltage induced is given by:

$$V_n = -M\frac{dI_N}{dt} \qquad (1.4)$$

where I_N is the RMS value of the sinusoidal current in the noise circuit and M is directly proportional to the area of the receiver circuit loop and inversely proportional to the distance between the noise source circuit and the signal circuit.

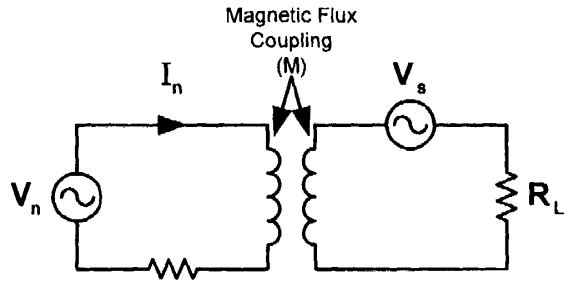


Figure 1.10 : Inductive Coupling between Noise Source and Signal Circuit

Inductive coupling can be reduced by minimizing the signal loop area or by increasing the separation distance. Another solution is to apply magnetic shielding either to the noise circuit or the signal circuit. At frequencies below 100 kHz, a soft iron shield is more effective than copper or aluminium.

1.5 System configurations

This section discusses a few typical system configurations used to stimulate a system under test and measuring the response. Signal injection is done by using actuating devices and sensors are used to measure the generated responses.

1.5.1 Personal computer with multi-function I/O board

If the stimulus and response nodes are in close proximity, a single personal computer with a multi-function I/O board can be used. The configuration is shown in Figure 1.1. A multi-function I/O board is normally PCI compatible and has analogue I/O and digital I/O capabilities, hence the name multi-function. The stimulus can be applied by using the analogue output channel and the various responses can be captured by the analogue input channels. The personal computer is used to control the data acquisition process and to display the stimulus and responses.

An example of a multi-function I/O board is the PCI-730 from Eagle Technology [22]. The PCI-730 is a low-cost PCI-based board with digital and analogue I/O capabilities. It has 24 digital I/O channels, 16 single-ended or eight differential 14-bit 100 kHz analogue input channels and four DAC channels with 14-bit resolution. The cost of this multi-function I/O card is R4 428-00.

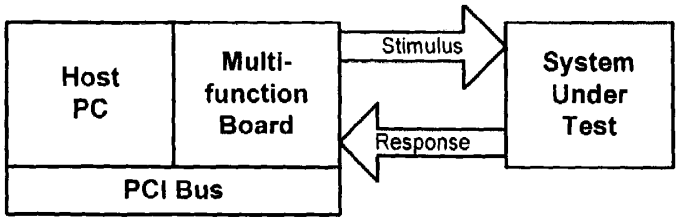


Figure 1.11 : PC with I/O card

The limitation of this setup is the distance between nodes. In a typical industrial process, the stimulus and responses can be tens of meters apart. In this situation the personal computer with multi-function I/O card system is not adequate since the length of the conductors from the sensor to the multi-function board should not exceed a few meters.

1.5.2 Networked Nodes

In an industrial environment the stimulus and response points can be tens or even hundreds of meters apart. Capturing data from such a process requires a networked measurement system consisting of several nodes. Each node functions as an analogue output, analogue input, or both and communicates with the host controller, usually a personal computer. Communicating with the host PC and controlling the peripherals such as the DAC and ADC cards require digital controllers.

Figure 1.12 shows a typical setup. An analogue output module is used to generate the stimulus, and an analogue input module is used to measure the generated response. An industrial single board computer is necessary to perform the control functions and to communicate with the host. The cost of such a system is more than double that of a system consisting of a personal computer with a multi-function I/O board. This cost escalation is due to the fact that each node requires a single board computer (SBC) to communicate with the host controller and to control the node's analogue I/O board. An example of a typical SBC is the PSB-810EAV from Eagle Technology which sockets a Pentium 3 Celeron processor and has 256 MB SDRAM. The cost of a SBC such as this one is in the order of R2800-00.

By using the PCI-730 multi-function I/O board with 24 digital I/O channels and 14-bit analogue I/O, a 14-bit system can be realized. A PCI-730 can be purchased for R4 428-00. The multi-function I/O board and the SBC are slotted into a PCI backplane and constitute a network node capable of communicating with the host controller. A node such as this one has 16 single-ended

or eight differential 14-bit 100 kHz analogue input channels, four DAC channels with 14-bit resolution and 24 digital I/O channels.

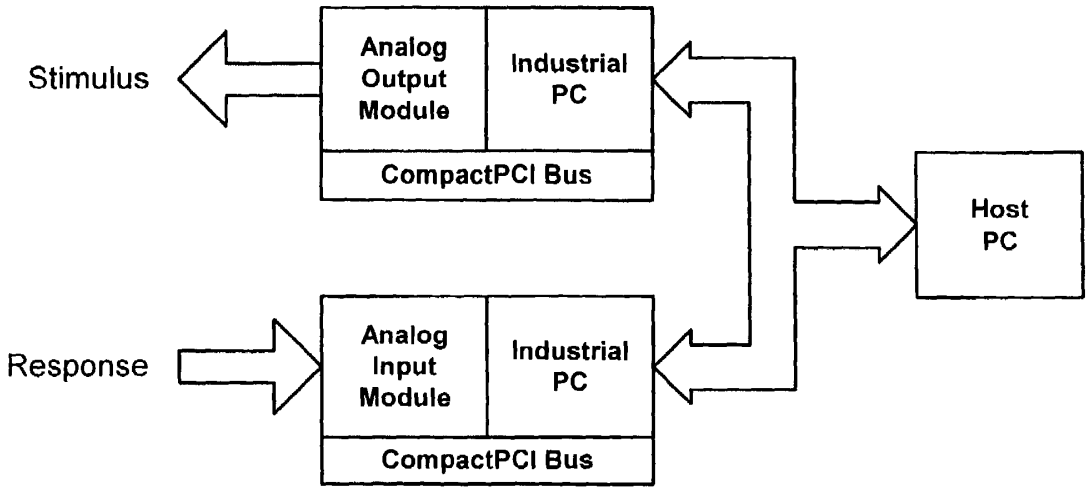


Figure 1.12 : Network setup

A typical application would use only the analogue I/O to generate a stimulus or measure a response. The total cost of one of these nodes is R7 228-00. A networked measurement system capable of generating a stimulus and measuring three responses would cost R28 912-00. A higher specification on the resolution of the measurement system would cause a further increase in cost.

If the application requires a system with 16-bit accuracy, a 16-bit multi-function I/O board should be used instead of the 14-bit board. The PCI-730E [23] from Eagle is an example of a 16-bit multi-function I/O board. This board has 16 single-ended or eight differential analogue input channels with 16-bit resolution and a maximum sampling rate of 100 kHz. In addition, this board has four analogue output channels with 16-bit resolution. The board also has a 4KB onboard memory buffer to store data. Since this board has a better resolution than the PCI-730, it is also more costly. The price of the PCI-730 is R5 628-00. The SBC and this 16-bit multi-function board implemented as a node in the network would cost R8 428-00. A 16-bit system consisting of one stimulus node and three nodes to measure the responses would cost R33 712-00.

The products of Eagle Technology were considered since previous work was done with these boards due to their low cost, compared to more complex measurement systems such as the systems offered by National Instruments. The data acquisition hardware from National Instruments exceeds the specifications for the intended purposes and is too complex and costly to be of any practical use for the intended purposes.

Figure 1.13 shows a graphical representation of the cost versus performance criteria for the measurement systems considered. The measurement system required for most engineering applications should be less complex than the products from National Instruments but should still be able to perform the popular functions. At the same time this system should perform better than the systems of Eagle Technology and should be less costly.

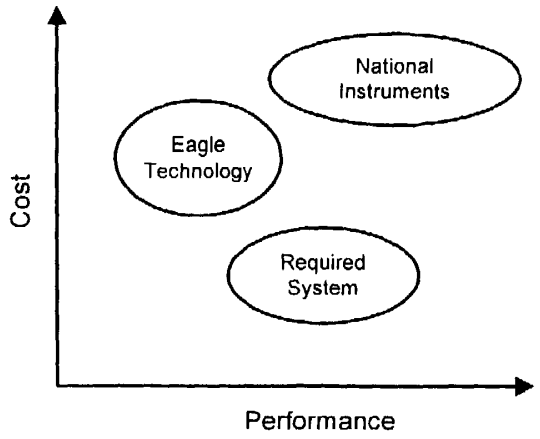


Figure 1.13 : Cost versus performance graph

To summarize, a measurement system must be developed that performs equally well or better than the low-end measurement systems while being less costly than high-end systems.

1.6 Limitations with existing systems

Some limitations of commercially available systems are that the systems are overly complex and very expensive. Another problem is that these systems do not provide sufficient galvanic isolation. Galvanic isolation is necessary in order to protect components in the system. For instance, if a transient or high voltage occurs at an input, it may damage not only the input circuit, but the rest of the data acquisition hardware. By propagating through the signal conditioning and ADC circuits, this transient can eventually damage the computer system as well. The solution to the problem is to develop a customized measurement system with the required specifications.

1.7 Custom designed measurement systems

Most data acquisition tasks can be executed by using off-the-shelf components. Some tasks require a refined measurement system which is not commercially available or too expensive. This section briefly mentions various measurement systems developed for a specific

application. Although the applications are very specialized, the technology used in the measurement systems is of importance and is discussed.

In the nuclear physics field it is often necessary to design a measurement system to be used in a new experiment. A data acquisition system has been designed for a muon catalyzed fusion experiment at the RIKEN-RAL Muon Facility [24]. Signals from the detectors are digitized in a CAMAC-based system. A CAMAC auxiliary crate controller concentrates on data capturing and the accumulated data are transferred to a workstation via a SCSI crate controller. The auxiliary crate controller is based on the MC68030 controller running at 40 MHz and has 1 MB of onboard memory.

The ALICE [25] data acquisition system has been designed to support a bandwidth of up to 2.5 GBytes/s and a storage capability of up to 1.23 GBytes/s to mass storage. The data acquisition system behind the Beam Loss Monitoring (BLM) [26] is an example of a distributed measurement system interconnected via CANbus. Data and commands are exchanged between the front-ends and the host controller by means of CANbus. The different front-ends are synchronized by broadcasting a CAN package.

The design of the CLEO III data acquisition system was guided by the need to reduce cost and complexity of both hardware and software, while achieving the required performance of 1000 Hz event rate [27].

OPERA is a long baseline neutrino experiment with a high modularity detector and low event count. To deal with these features, a distributed DAQ system based on Ethernet standards for the data transfer has been chosen. A distributed GPS clock signal is used for synchronizations and time stamp of the data [28].

The data acquisition system for the silicon pad detector used in experiment E-835 at Fermilab is another example of a custom made measuring system [29]. The data flow from the detector is in the range of 1 Mbyte/s. This system is interfaced with other elements of the global data acquisition system.

The Bragg-Curve Counter (BCC) system is used for the measurement of target multifragmentation in high-energy light-particle and nucleus collisions [30]. The BCC system was upgraded to a system with 37 channels. This required a new data-acquisition system capable of handling event rates and data sizes 10 times larger than the old system. This system

is also CAMAC-based and makes use of an auxiliary crate controller. This crate controller has a data acquisition speed of 200 KB/s and transfers data to the host computer at 1 MB/s.

In fusion experiments the increase of the discharge duration called for the development of an advanced measurement system [31]. A real-time data acquisition, reduction, analysis, storing and control system associated with a fast data and event transportation and synchronization was developed. This system used digital signal processors (DSPs) and field programmable gate arrays (FPGAs) for processing and the InfiniBand open standard for data transport. A specialized low latency synchronous network was used for synchronization and data stamping.

The DAQ system for the Compton Camera [32] was implemented by using Xilinx Spartan II devices and 12-bit 65 MHz ADCs. The system consists of a channel processor, a backplane and an event builder. Peak detection, 24-bit time stamps and integration operations are performed on each channel.

The HERA-B Data Acquisition System [33] implements a 50 kHz dead-timeless readout of 500 KB events requiring unprecedented speed of storing and data processing. The system is based on Digital Signal Processors (DSPs) minimizing the number of components. A high bandwidth, low-latency DSP switching network provides full connectivity between the readout buffers and a PC.

A transient recorder module was developed for data acquisition on fusion experiments [34]. The recorder is based on digital signal processors and programmable logic devices. These devices provide features such as multi-channel real-time data readout, real-time digital signal processing and a large quantity of onboard memory. All channels on the module are differential, galvanically isolated up to 1kV and over-voltage protected. The acquisition rate is 2M samples per second with 14-bit resolution. Local data storage capacity is 256M samples.

High-energy physics experiments require advanced data acquisition systems for capturing the data. Since 1960 the DAQ systems used in these experiments have evolved quite dramatically [35]. A hundred channels were read at a few hertz during the late sixties. This required a single minicomputer to handle the task at hand. Modern experiments have millions of channels read at megahertz rates. The DAQ systems used today feature distributed processing, complex trigger systems for event filtering, switch networks, and PC-based computer farms.

The PULSAR [36] is an example of a versatile, flexible, cheap, high-speed data acquisition and generation system used for testing complex digital components. The system backplane is

connected to the ISA bus of a personal computer by means of a standard internal I/O card. Up to eight acquisition and generator boards can be slotted into the backplane. These acquisition boards have up to one megabyte of onboard RAM which is mapped as virtual PC memory. Fast data transfer between the memory and mass storage is accomplished by this mapping. An SRAM-based FPGA is used as the main controller on the data acquisition and generator board. Program data for the FPGA are stored inside a small onboard PROM. This program controls all data transfers to and from the data acquisition board.

1.8 Summary

The various measurement systems discussed were all developed because no suitable commercial system existed for the particular application. Motivations for the design included factors such as cost, performance and availability. Some of these systems required significant resources and large development teams to complete. These systems were implemented in the physics field where huge amounts of data were captured fast.

The designs used the latest computing technology like FPGAs, DSPs and CPLDs to control the system and process the data. Some of these systems performed real-time signal processing. The communication task was accomplished by using Ethernet, TCP/IP, CANbus, Fieldbus, or direct connection to the ISA bus of the PC. Some of these systems were interfaced to existing measurement systems which required additional development. To display the captured data efficiently, graphical user interfaces were developed for some of these systems.

The cost of a system is usually related to the complexity. Thus the development of the aforementioned systems cost hundreds of thousand and even millions of rands. The measurement system discussed in this document is not as complex as these systems but some of the concepts used in these systems proved to be useful.

1.9 Problem statement

A custom designed measurement system capable of handling waveform acquisition and generation tasks is required. This system should be less costly than commercially available systems, flexible and user-friendly. In addition, the system should be able to make high speed high resolution synchronous measurements at multiple points and should have superior galvanic isolation.

Chapter 2

Design

Perhaps the most useful area of electronic engineering involves gathering and manipulating data from an industrial process or a scientific experiment. The industrial process can be electrical, mechanical, thermo dynamical, or combinations thereof. Once data are collected from the process, modelling, parameter estimation, condition monitoring and fault detection can be done on the system. An inexpensive yet efficient measurement system is needed to acquire the necessary data for subsequent analysis. This chapter describes the design of a measurement system capable of exciting a system under test and measuring multiple responses by using a systems engineering approach [37].

PART I

CONCEPTUAL DESIGN PHASE

2.1 Customer Requirements

Many instances for the requirement of an inexpensive general purpose measurement system exist. Such a system must be capable of performing the most popular functions of commercially available systems, but must be less expensive than commercial counterparts. In addition, the system should be easy to install and operate. This will accelerate the data capturing process and allow more time for further data processing. The key requirements of the measuring system are summarized below:

- Perform most popular functions such as signal injection and signal acquisition
- Should measure a variety of voltage levels, up to a few kilovolts
- Distance between measurement points in the order of 20 m
- Must be galvanically isolated from the rest of the system
- Easy installation and operation
- General purpose system
- Low cost system.

2.1.1 General purpose system

The system should be able to measure a wide range of variables given the correct sensors. These variables include temperature, pressure, mass flow, voltage, current, power etc. General purpose mainly refers to the input and output stages of the system. The system requires an input voltage from a transducer and supplies an output voltage to an actuating device.

2.1.2 Inexpensive

When specifying cost as a requirement, product quality must be kept in mind. When a new system is designed, the most important demand is correct functionality. It is of no use to have an inexpensive partly-functioning measuring system. The customer will rather pay more for a commercial product that is guaranteed to function effectively. Cost should be considered only when functionally equivalent components are considered.

2.1.3 Perform most popular functions

The system must be able to perform only the essential functions and not any specialized functions. This reduces the complexity of the system and development cost. Reduction in complexity also speeds up the troubleshooting process and decreases downtime. The two most crucial functions necessary is waveform generation and waveform digitization.

2.1.4 Easy installation and operation

When working on a project, the engineer often needs to gather data from an industrial process. Installation of the measuring system should be straightforward and simple. Additionally, the system should be easy to transport. The system must be robust to ensure functionality even when subjected to frequent transportation. Commercially available systems often call for elaborate training sessions in order to fully understand the measuring system. The setup procedure for the measuring system should be easy and the data capturing process should be simple, yet effective.

2.2 Design Requirements

Determining the design requirements is one of the most important aspects of the engineering process. Engineering experience is of utmost importance when transforming customer requirements to design requirements. Design requirements must be measurable and should be verified when the design is completed.

Decisions pertaining to design requirements are also very important with regard to the systems engineering approach to design. A decision made at this stage is fixed at the latest stages of development. It is not desirable to change design requirements since the whole design will change and time and capital investment will be wasted or lost. Well-informed decisions in the early design stages prevent redesigning at later stages in the systems engineering approach.

The design requirements for the measuring system may be stated as:

- High resolution, high speed waveform generation
- High resolution, high speed digitization
- Galvanic isolation
- Host controlled
- Modular.

2.3 Functional Analysis

This section discusses the measurement system in terms of its functionality. The system functionality can be divided into three distinct functions:

- Communicate with host controller.
- Generate waveform (stimulus).
- Measure waveform (response).

2.3.1 Initial System Level Functional Analysis

The functions that any system must perform should be established before technologies are allocated to perform the functions. A design should only be limited by certain technologies when trade-offs are performed and not during an abstract functional analysis. Engineering teams may make some technology choices from experience.

Figure 2.1 summarizes the system level functions of the system. At this stage, no choice of technology has been made with regard to the system. Technological choices will be made during resource allocation.

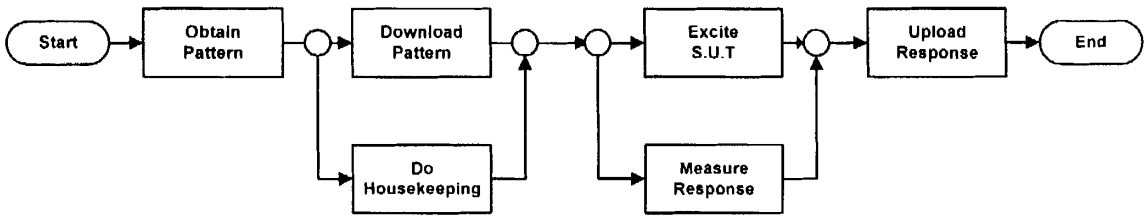


Figure 2.1 : System level functional analysis

At the system level the measurement system is not complex. It is connected to the system under test (S.U.T) and is controlled by means of a personal computer. Different commands are sent from the computer to start and stop processes of the measurement system. A suitable graphical user interface is necessary to display the acquired data on the computer.

2.3.1.1 Obtain pattern

The waveform used as stimulus when performing signal injection is stored in a data file on the personal computer. Software facilitates the retrieval process whereby this file is opened and the waveform displayed.

This data file containing the waveform data can be created in different ways:

- Capturing a physical signal by means of a digitizer
- Defining the waveform by using mathematical functions from a software package such as Matlab, Visual C++ or Visual Basic
- Drawing the waveform on screen using dedicated waveform editing software.

Mathematically generated waveforms can be frequently used waveforms such as sine, square, and triangle. More complex waveforms can be created by defining waveforms in multiple buffers and performing waveform staging (or sequencing). This method links and loops these buffers in any order and can generate true arbitrary waveforms.

2.3.1.2 Download pattern

Once the pattern is loaded from file, it is transferred to the measuring system hardware via the interface. The waveform is stored in medium depth, fast access memory on the measurement system. After a successful waveform download, the measurement system is in idle mode and waits for further commands from the host controller.

2.3.1.3 Do housekeeping

As the waveform is downloaded, the firmware should prepare the hardware for the injection and measurement phase. This preparation includes initialization of timers, variables and buffers.

2.3.1.4 Excite system under test

The excitation of the system under test consists of two steps. At first the frequency of the clock signal must be set. The next step is to start the clock signal which serves as the time base for waveform generation. The whole waveform is generated before the clock signal is stopped under control of the firmware.

2.3.1.5 Measure response

The clock signal is shared by the waveform generator and waveform digitizer. This common clock signal synchronizes the waveform generation and waveform digitization processes. By synchronizing these events, a precise input-output relationship of the system under test can be obtained. A value is measured by the waveform digitizer for every value generated by the waveform generator.

2.3.1.6 Upload response

The final step is to upload the measured data to the host controller for further analysis. Captured data are sent to the host controller and stored in a data file. This completes the data acquisition cycle.

2.3.2 Functional allocation

Related functions are grouped together into subsystem blocks that will perform these functions. High level trade-offs should be carried out and the best alternative should be selected.

2.3.3 Functional packaging

The measuring system can be subdivided into three components as shown in Figure 2.2:

- Hardware
- Software
- Firmware.

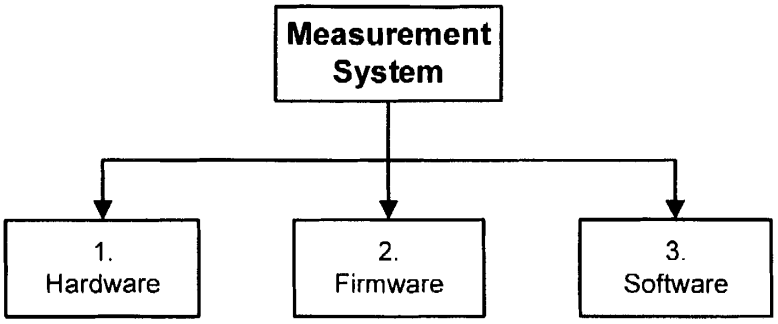


Figure 2.2 : Functional allocation top level

2.3.3.1 Hardware

A block diagram of the measuring system hardware is shown in Figure 2.3. The most important functions of the system are signal injection and signal measurement. Signal injection is done by the waveform generator which converts digital codes to analogue output voltages. Analogue input voltages are sampled by the digitizer. When the system is capturing data, these data should be stored in memory. The signal injection and signal acquisition processes are under control of the processor. At some stage the measuring system should transfer data to and from the host computer, under control of the processor. The transceiver converts the voltage levels for communication with the host computer. Communication also requires some form of

intelligence to interpret packets and to perform error checking. None of these components will function without a power supply for the correct voltages as required by the measuring system.

The measuring system consists of a power supply, transceiver, processor, waveform generator and digitizer. A processor used in this sense is also known as an embedded processor. These five components will be discussed in more detail during the design phase.

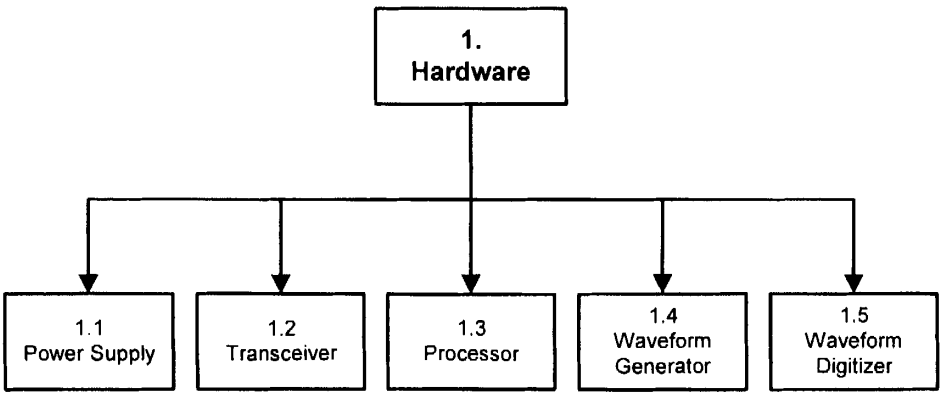


Figure 2.3 : Functional Allocation (Hardware)

2.3.3.2 Firmware

The processor performs communication tasks and orchestrates all actions performed by the measuring system. Code on the processor, called firmware, is written to perform all the mentioned functions. All communication, peripheral control and housekeeping are under control of the processor and its firmware. Figure 2.4 shows the main functions to be performed by the firmware running on the embedded processor.

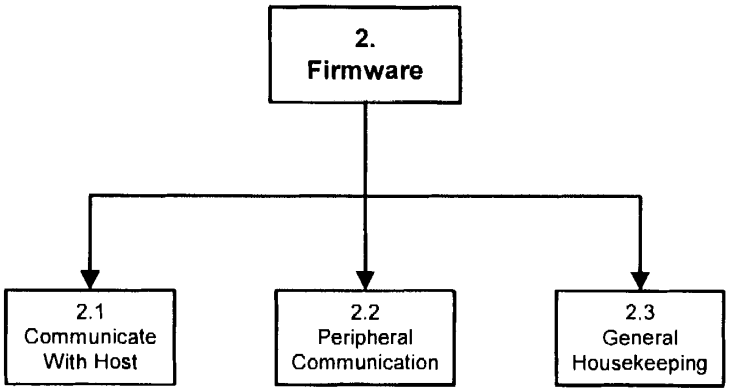


Figure 2.4 : Functional allocation (Firmware)

2.3.3.3 Software

One side of the communication link is under control of the embedded processor and its firmware. The other side is controlled by the host computer and its associated software. The software on the host computer should perform the following functions as shown in Figure 2.5:

- Generate the data file for excitation
- Communicate with the hardware
- Display the captured data.

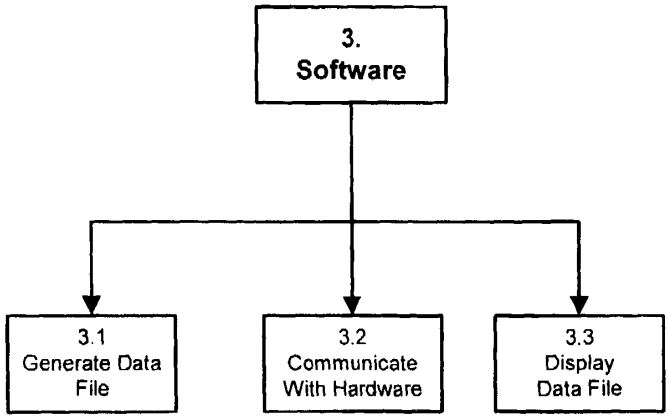


Figure 2.5 : Functional allocation (Software)

2.4 Design Alternatives and Trade Offs

Two possible design alternatives were considered. The first was to design an all in one device that contains the power supply, analogue interface, communications hardware and microprocessor. As a second alternative, a modular approach was considered. The modular approach, consisting of individual modules each with a specific purpose, was followed. This approach simplifies troubleshooting and makes it easy to upgrade one module without changing the rest of the system.

2.5 Design Concept

Figure 2.6 shows a simple block diagram of the proposed measurement system. A personal computer is used to transfer data to and from the measurement system. The waveform to be injected into the system under test is downloaded to the waveform generator which performs the excitation.

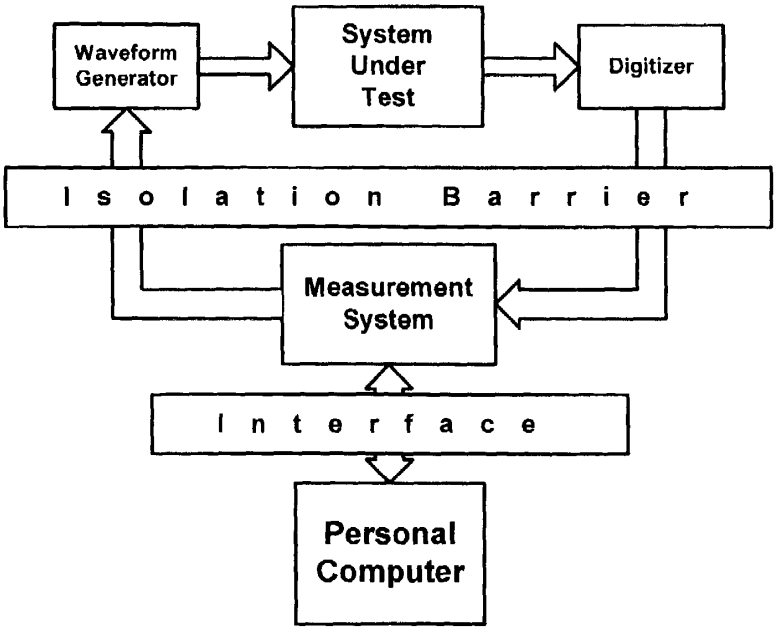


Figure 2.6 : Functional architecture

The response of the system under test is measured at multiple points (only a single point is illustrated in Figure 2.6) by the digitizers. After one complete cycle, the data are retrieved from the digitizers and displayed on the personal computer. Part 2 of this chapter discusses the design of each component in more detail.

PART 2

PRELIMINARY AND DETAIL DESIGN PHASE

In the preliminary design phase, the same process that has been followed in the conceptual design phase is carried out at a sub-system level. If a Quality Function Deployment (QFD) House of Quality (HOQ) [38] analysis should be implemented at sub-system level, the inputs are the prioritized design requirements that have been determined in the previous section.

In the case of the measurement system, a QFD HOQ analysis at the preliminary and detail design stages was not carried out explicitly. Since the technical risk was low, and the cost associated with following a detailed HOQ analysis at lower levels was high, a straightforward systematic design approach was followed.

The detail design of the measuring system is discussed in this section. This design is subdivided into the main functions to be performed by the measuring system:

- Communication
- Waveform generation
- Waveform digitization.

2.6 Communication

2.6.1 OSI Model

The open systems interconnection (OSI) model [39], [40], developed by the International Organization for Standardization (ISO), is a model for computer communications architecture. Figure 2.7 illustrates the OSI model.

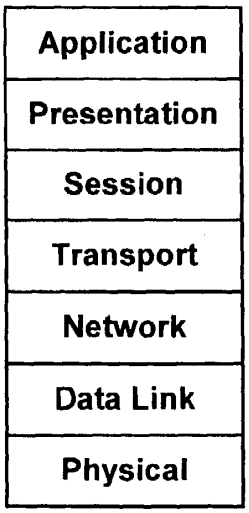


Figure 2.7 : OSI Model

2.6.2 Medium

The physical transmission medium is part of the physical layer in the OSI model. In a data transmission system, the transmission medium is the physical path between transmitter and receiver. Transmission media can be classified as guided or unguided. With guided media, the waves are guided along a solid medium, such as copper twisted pair, copper coaxial cable, or optical fibre. The atmosphere and outer space are examples of unguided media, which provide a means of transmitting electromagnetic signals but not guide them; this form of transmission is usually referred to as wireless transmission. Radio, satellite, microwave and infrared are examples of wireless transmission.

The measurement system will be used in industrial environments, and reliability and data integrity are of utmost importance. Considering the effects of interference and cost, guided transmission is the better option for this application. From the available mediums, optical fibre

was selected. The advantages of optical fibre as compared to twisted pair and coaxial cable are:

- Smaller size and lighter weight
- Provides galvanic isolation.
- Electromagnetic immunity
- Greater repeater spacing
- Resistant to corrosion
- Lower attenuation
- Greater capacity

Optical fibre can be made from glass or plastic. To minimize cost, plastic optic fibre is used in this project. The plastic fibre proved to be sufficient for the distance and bit rate as required for this project.

2.6.3 Physical layer

Functions within this layer are responsible for activating, maintaining, and deactivating a physical circuit between communicating devices and for transmitting raw bits over the data link. Specifications for physical signals (electrical, optical), cabling, and the characteristics of the connectors are included in this layer. This layer accepts frames from the data link layer and translates the bit stream into signals on the physical medium, which lies below the physical layer.

2.6.4 Network topology

Possible network topologies available include bus, tree, star and ring. The bus topology was eliminated since it is physically not possible to connect the optical fibre in a bus topology. The structure of a tree topology is very complex in terms of the topology and routing firmware required. The star topology is a suitable choice but would require more optical fibre to be used and the number of communication ports should be equal to the number of nodes in the network. This makes it very difficult to expand the system and impairs the flexibility of the system.

Since this system would be used in an industrial environment, there would typically be a distance in the order of tens of meters between the nodes in the network. In order to maximize distance between nodes and to simplify network expansion, a ring topology was chosen for this project.

2.6.5 Interface

In order to interface to the optic fibre, electrical signals need to be converted to optical signals. This is accomplished by using an optical transmitter and an optical receiver. Three different types of optical sources are used in fibre optic systems: the light-emitting diode (LED), edge-emitting semiconductor laser diode, or vertical cavity surface-emitting lasers (VCSELs) [41]. The LED was chosen because it is less costly, operates over a greater temperature range, and has a longer operational life.

Data from the measurement system need to be transferred to the personal computer. To simplify matters, a serial communications port on the personal computer was used. An RS-232 to optical transceiver was designed to accomplish the conversion.

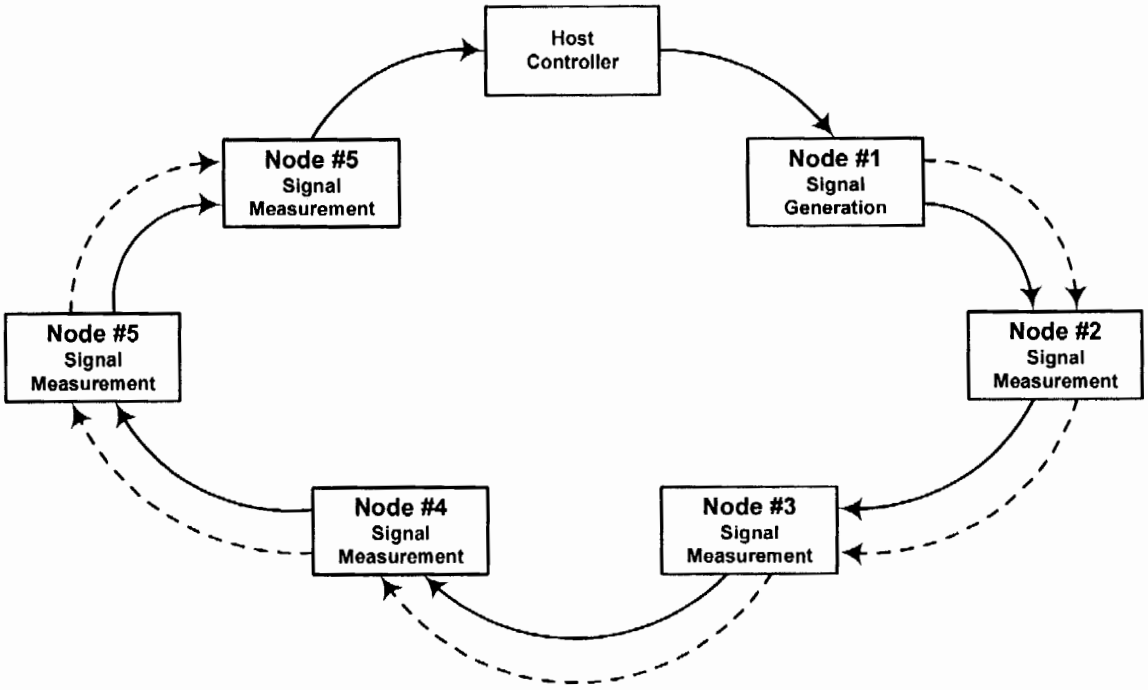


Figure 2.8 : Network Topology

2.6.6 Data representation

Transmission modes can be subdivided into two broad categories: synchronous transmission and asynchronous transmission. The main difference between these two modes is that in the synchronous case, the receiver uses a clock which is synchronized to the transmitter clock. This clock can be transferred in two ways:

- A separate interface circuit (as in X.21 and RS-449)
- Encoded in the data (i.e. Manchester encoding, AMI encoding, HDB3 encoding).

In an encoded system, the receiver generates a copy of the original clock signal from the transmitter by using a phase locked loop (PLL). Although higher data rates can be achieved by using synchronous transmission, the penalty is a more complex interface design. This system uses asynchronous transmission (RS-232) between nodes.

RS-232 was used between the personal computer and the RS-232 to optical converter. In the optical fibre network, a light pulse represents a binary value of one and no light represents a zero. Significant power savings are accomplished by using this active-high transmission scheme. The transmission rate is determined by the communications port of the host and must be the same as that of the nodes in the network.

2.6.7 Data link layer

The principal service provided by the data link layer to higher layers is that of error detection and control. Thus, with a fully functional data link layer protocol, the next higher layer may assume error-free transmission over the link. To simplify the design, the data link layer was not implemented. The data transfer process proved to be reliable enough without the data link layer. Since this layer is implemented in software on the personal computer and firmware on the measurement system hardware, this functionality can be incorporated if required.

2.6.8 Network layer

The network layer is responsible for the end-to-end routing or switching of data to establish a connection for the transparent delivery of data. This layer addresses and resolves all inherent problems related to the transmission of data between networks. The first byte in the data packet contains the destination address and the third byte contains the source address. Any number between 1 and 255 is valid, but 0 is reserved for the host controller.

2.6.9 Transport layer

The transport layer provides a mechanism for the exchange of data between end systems. The service ensures that data are delivered error-free, in sequence, with no losses or duplications. This layer gives the user several options in obtaining certain levels of quality from the network. It is designed to keep the user isolated from some of the physical and functional aspects of the network. No transport protocol was implemented in this design.

2.6.10 Session layer

The session layer serves as a user interface with the transport service layer. The layer provides for an organized means to exchange data between users. Users can select the type of synchronization and control needed from the layer. In this particular application a simple query and response scheme is used and there is no need for session layer services.

2.6.11 Presentation layer

The presentation layer provides for the syntax of data in the model; that is, the representation of data. It is not concerned with the meaning or semantics of the data. Its principal role, for example, is to accept data types (character, integer) from the application layer and then negotiate with its peer layer as to the syntax representation (such as ASCII). Thereafter, its functions are limited. The layer consists of many tables of syntax. The layer is not implemented in this system since all the applications on all the nodes make use of a common convention.

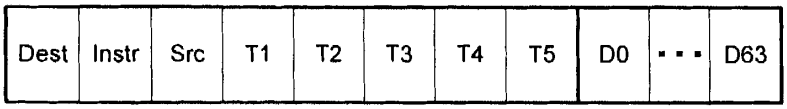
2.6.12 Application layer

The application layer is concerned with the support of an end-user application process. Unlike the presentation layer, this layer is concerned with the semantics of data. The layer contains service elements to support application processes such as job management and financial data exchange. The layer also supports the virtual terminal and virtual file concept. This layer is implemented in the measuring system via the user interface software used to transfer data to and from the nodes in the network.

2.6.13 Packet structure

Data must be transmitted from a source to a destination in the network. A header containing the source and destination addresses needs to be attached to the data. This process is called encapsulation. A complete packet of data consists of the actual data encapsulated by the header. The structure of a data packet is shown in Figure 2.9.

The header consists of the destination address, instruction code, source address, tag field, and data field. The destination address and source address is an 8-bit address from 1 to 255; address 0 is reserved. An instruction field is included to give commands to the destination address. The instruction codes in use are 0x01 (Load file), 0x02 (Save file), 0x03 (Set digital clock frequency), 0x04 (Enable digital clock), 0x05 (Disable digital clock), and 0x06 (Request data). More instruction codes can be implemented easily if required.



Dest : Destination Address (1 byte)
Instr : Instruction Code (1 byte)
Src : Source Address (1 byte)
Tx : Tag Field #x (5 bytes)
Dx : Data Byte #x (64 bytes)

Figure 2.9 : Packet structure

The five tag fields are auxiliary fields and can be used to pass additional information or parameters if necessary. Data are send in the data field which consists of 64 bytes. To transfer a complete waveform file consisting of 4096 integers, 128 packets (of 64 bytes each) of data must be transferred as shown in Figure 2.10.

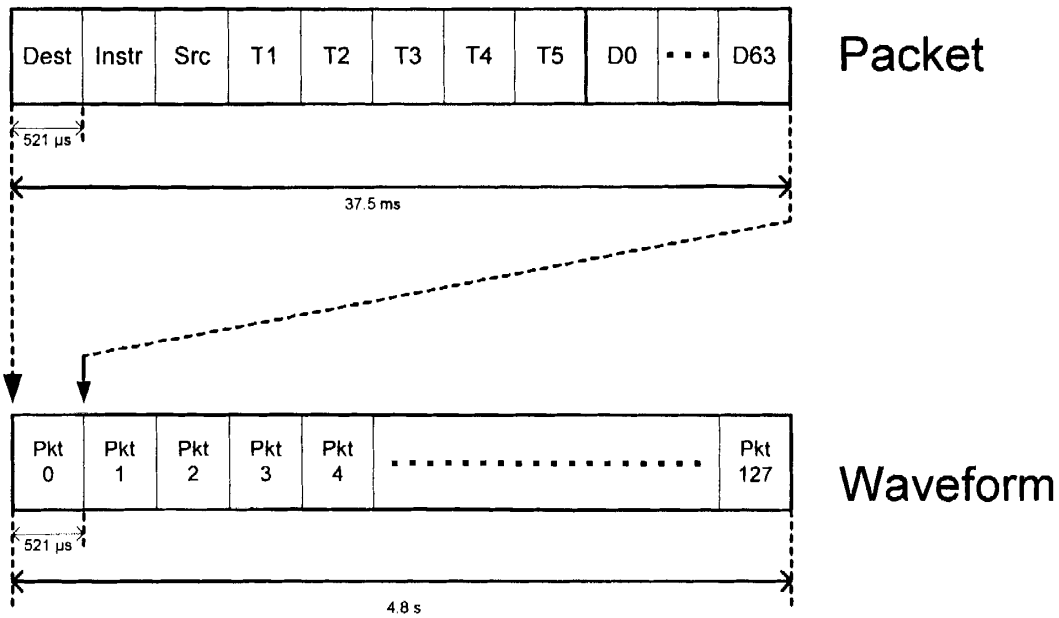


Figure 2.10 : Waveform transfer

At a baud rate of 19200 bps a single byte is transferred in 52.1 µs, a packet is transferred in 37.5 ms and a complete waveform consisting of 128 packets takes 4.8 s to be transferred. These transfer times are suitable for the intended application.

2.7 Waveform Generation

The response of a system can only be measured after the appropriate stimulus has been applied at the input. This stimulus is a waveform and can be any variable such as voltage, current, pressure, or mass flow. The conversion from voltage to any of the other quantities is accomplished by an actuator. The voltage waveform is generated by a digital-to-analogue converter (DAC). Design of the waveform generator involves choosing the correct DAC and surrounding circuitry. This part of the design is discussed in the following sections.

2.7.1 Digital-to-analogue conversion process

The digital-to-analogue conversion process is employed to convert the digital signal into an analogue form after it has been stored in digital format. The most commonly used arrangement is shown in Figure 2.11, and consists of two main components: the DAC and a low-pass filter which is also called a reconstruction, smoothing, or anti-image filter.

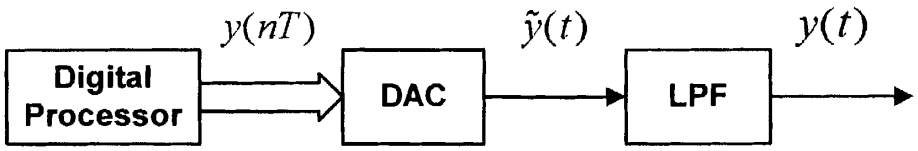


Figure 2.11 : Digital-to-analogue conversion process

2.7.2 The DAC

The DAC is the most important component in the waveform generator. The basic DAC accepts digital data and produces an analogue output signal which is proportional to the digital code at its input. Several parameters need to be evaluated when comparing different DACs.

2.7.2.1 DAC specifications

DAC specifications can be subdivided into two categories, general specifications and performance specifications [42]. General specifications include architecture, interface type, output type, and number of outputs. Performance specifications include resolution, settling time, differential nonlinearity (DNL), integral nonlinearity (INL), power dissipation, and packaging options. Design requirements determine which DAC should be used in this project. The following subsections discuss the most important specifications.

- ***Resolution***

Since the waveform generator should be capable of generating high resolution waveforms, the resolution of the DAC should be high. A DAC with 16-bit resolution would be sufficient for the application. For an input voltage range of ±10 V, the resolution is 305 µV, which translates to an error of 0.0015 %.

- ***Settling time***

Settling time is the time from a change in input code until a DAC's output signal remains within ±½ LSB (or some other specified tolerance) of the final value. This value limits the maximum frequency at which data can be sent to the DAC. The maximum clock frequency of the system is 50 kHz which translates to a period of 20 µs. Thus, the settling time of the DAC should be less than 20 µs.

- ***Interface type***

Possible interfaces to be used are serial, parallel, SPI, I^2C, or Microwire. A parallel interface was chosen because of the fast transfer rate that can be attained. Another motivation was that simpler and faster code is required to interface to a parallel DAC.

- ***Packaging options***

One of the customer requirements is to keep the system simple. This means that construction and troubleshooting should be kept fairly straightforward. For this purpose a dual-in-line (DIP) package was chosen since it is readily available and allows mounting in a socket.

2.7.3 Available DACs

The different digital-to-analogue converters of some market-leading manufacturers were considered and a choice was made based upon the criteria defined in section 2.7.2.1. Products of Maxim, Texas Instruments, Linear Technology and Analog Devices were considered (see Appendix A).

2.7.3.1 Maxim

The digital-to-analogue converter series of Maxim includes a wide range of possible solutions. They have 25 different 16-bit DACs available. Fifteen of these devices satisfy the package

requirements. Seven of these devices have settling times of less than 10 µs, but all of these devices have only serial interfaces available. Thus, Maxim has no suitable device.

2.7.3.2 Texas Instruments

Texas Instruments have twenty-eight 16-bit devices available. Although these devices have settling times less than 20 µs, the packaging options are limited to surface mount. Another restriction is that most of the devices only have a serial or 16-bit interface.

2.7.3.3 Linear Technology

Linear Technology offers eight products with the required resolution and settling time. Four of these devices have a parallel interface bus, but they are not suitable since their data bus is16 bits wide. The rest of the converters are all serial interface devices, which is not appropriate either.

2.7.3.4 Analog Devices

Analog Devices has four devices which met the search criteria. These devices are AD7846, AD7849, AD660, and AD669. Of these, the AD660 was chosen because it met all the specifications and it is readily available. The AD660 is a 16-bit DAC with an on-board voltage reference, double buffered latches and output amplifier. Integral and differential nonlinearity is maintained at ± 1 LSB and the settling time is 10 µs to within ½ LSB for a full-scale step. Data can be loaded into the AD660 in serial mode or as two 8-bit bytes. The byte mode input format is also flexible in that either the high byte or low byte data can be loaded first. The double buffered latch structure eliminates data skew errors and provides for simultaneous updating of DACs in a multi-DAC system. Different packages are available, including a plastic DIP package.

2.8 Waveform Digitization

Once a stimulus is applied to a system by using a waveform generator, the response of the system must be measured at various points. The digitizer is used to capture the waveform and consists of an anti-aliasing filter followed by an analogue-to-digital converter (ADC). This section describes the design of the digitizer section of the measurement system.

2.8.1 Analogue-to-digital conversion process

Figure 2.12 shows the analogue-to-digital conversion process. The first stage in the conversion process is to band-limit the analogue input signal. If required, this is done by a low-pass filter

also known as an anti-aliasing filter. Next the filtered analogue signal is converted to digital form by an analogue-to-digital converter. The digital value produced by the ADC is read by the digital processor, which stores or processes the captured data.

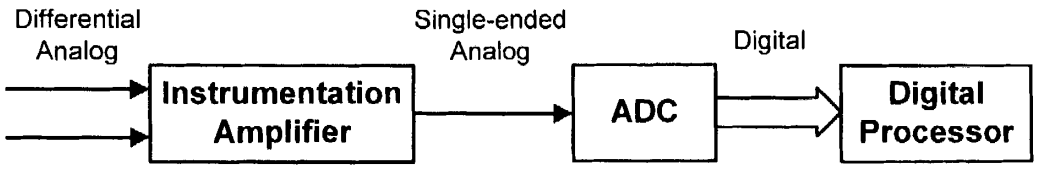


Figure 2.12 : Analogue-to-digital conversion process

2.8.2 Instrumentation Amplifier

An instrumentation amplifier has a high input impedance and offers noise rejection. For this reason, the AD624 instrumentation amplifier from Analog Devices was used in this design. It is a high precision, low noise instrumentation amplifier designed for use with low level transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity makes the AD624 ideal for use in high resolution data acquisition systems.

2.8.3 Analogue-to-digital converter

The analogue-to-digital converter is the most important component in a waveform digitizer. The ADC converts an analogue input signal to a digital code for further processing by a digital processor. When choosing a suitable ADC, the following specifications need to be considered.

2.8.3.1 ADC specifications

As with the DAC, ADC specifications can be subdivided into two categories, general specifications and performance specifications [43]. General specifications include architecture, interface type, input type, and number of inputs. Performance specifications include resolution, sampling rate, signal-to-noise ratio (SNR), differential non-linearity (DNL), integral non-linearity (INL), signal-to-noise and distortion ratio (SINAD), spurious free dynamic range (SFDR), power dissipation, and packaging options. To find a suitable ADC for use in this project, the customer requirements guide the way. The following subsections discuss the most important specifications.

- **Resolution**

When an analogue signal is digitized, it is represented by a finite number of discrete voltage levels. The number of discrete levels used to represent the signal is known as the resolution. An increase in resolution will capture the analogue signal more accurately. This measurement

system must be capable of making high accuracy measurements. A converter with a higher resolution will also reduce quantization error. Thus, an analogue-to-digital converter with a 16-bit resolution is used in this system.

- ***Sampling rate***

The sampling rate is the rate at which the converter acquires the input signal, digitizes it, and outputs data to the digital processor. For this measurement system an ADC with a sampling rate of 100 kHz is required. The Nyquist criterion states that, in order to prevent undesired aliasing, a signal must be sampled at a rate equal to at least twice its bandwidth. Thus, frequencies of up to 50 kHz can be measured by a 100 kHz ADC.

- ***Interface type***

As with the DAC, possible interfaces to be used are serial, parallel, SPI, I^2C, or Microwire. A parallel interface was chosen because of the fast transfer rate that can be attained. Another motivation is simpler and faster code needed to interface to a parallel ADC.

- ***Packaging options***

One of the customer requirements is to keep the system simple. This means that construction and troubleshooting should be kept fairly straightforward. For this purpose a dual-in-line (DIP) package was chosen since it is readily available and allows mounting in a socket.

2.8.4 Available ADCs

The same process is followed as with the choice of an appropriate DAC. The ADCs of some leading manufacturers were considered and a choice made based upon the criteria defined in the previous section. Products of Maxim, Texas Instruments, Linear Technology and Analog devices were considered (see Appendix B).

2.8.4.1 Maxim

Packaging is the only requirement not fulfilled by Maxim. All the ADCs have the required resolution, sampling rate and interface options but are only available in surface mount packaging. This shortcoming does not satisfy the easy assembly requirement.

2.8.4.2 Texas Instruments

The ADS7805 from Texas Instruments is a suitable ADC with the required resolution, sampling rate and package, but the interface is 16-bit parallel.

2.8.4.3 Linear Technology

Linear Technology has a suitable device satisfying all the requirements. The LTC1605 is a 16-bit 100 ksps ADC in a plastic dual-in-line package. Interfacing to the device can be accomplished via an 8-bit or 16-bit parallel bus.

2.8.4.4 Analog Devices

The AD676 and AD976 are both suitable candidates for use in the digitizer. These two devices are 16-bit 100 ksps ADCs with an 8-bit or 16-bit parallel interface and is available in plastic dual-in-line packages. Based on the survey done, the AD976 was chosen based on availability and previous experience with the device.

2.9 Digital Clock Generator

All digital-to-analogue and analogue-to-digital conversions must be synchronized in order to obtain an input-output mapping of a system. A common clock signal must be fed to all DACs and ADCs to synchronize the system. The digital clock generator (DCG) was developed to generate a clock signal with a variable frequency to facilitate different sampling frequencies.

2.9.1 Block diagram

The clock generator is capable of generating clock signals of variable frequency and duty cycle. Figure 2.13 shows a block diagram of the digital clock generator. Three cascaded 8-bit dividers make it possible to divide by any factor from 1 to 16 581 375. The 40 MHz clock source crystal can be replaced by any other frequency, to accommodate even higher or lower clock frequencies. For example, a 100 MHz crystal can produce sampling rates of 6.03 Hz to 100 MHz, and a 10 MHz crystal can generate frequencies from 0.603 Hz to 10 MHz.

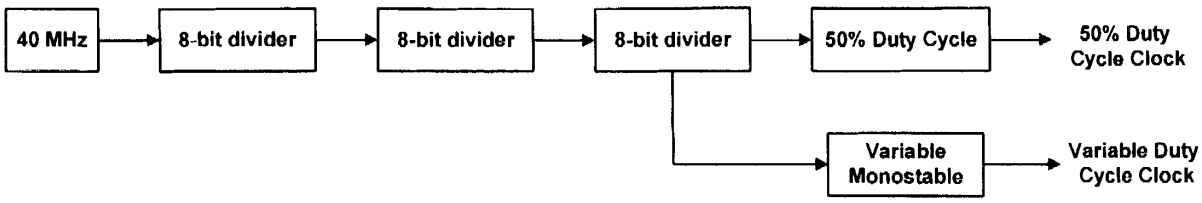


Figure 2.13 : Digital clock generator block diagram

The DCG uses programmable 8-bit dividers which can be programmed by writing a byte to each divider. The digital controller is used to set the sampling frequency by writing the appropriate presets to the different dividers. Two options for the duty cycle of the output clock are available; a fixed 50% duty cycle and a variable duty cycle clock. Troubleshooting and measurement of the output clock signal are made more simple by enabling the 50% output while the variable duty cycle can be used under normal operating conditions.

A variable duty cycle makes it possible to replace the current DAC and ADC without changing the clock generator. If a different type of optical fibre is used, the duty cycle can also be adjusted for optimal transmission via the fibre.

2.10 Digital Controller

The digital controller is necessary to control the waveform generator and waveform digitizer, to program the digital clock generator, and to communicate with the host. Since a modular approach is followed, the digital controller is a standalone module consisting of all the necessary supporting peripherals as discussed next.

2.10.1 Block diagram

A block diagram of the digital controller and surrounding circuitry is shown in Figure 2.14. The main component in the controller module is the DS89C310 microcontroller from Dallas Semiconductor. This microcontroller is a high speed 8051 based 8-bit microcontroller and was chosen since it executes instructions between 1.5 and 3 times faster than the original architecture with the same frequency crystal. Read only memory (ROM) is needed to store the program code for the microcontroller. In this project a standard 27C256 32 Kbyte UV EPROM was used. The code along with the EPROM is collectively known as firmware. Flowcharts of the firmware operation can be seen in Appendix D.

The digital controller module also needs storage to store the sampled data or waveform to be generated. Two static RAMs on the board give 64 Kbytes of RAM to store the needed data. Static RAM was chosen since it is the fastest, and it can be easily interfaced to the microcontroller.

The Peripheral Port Interface (PPI) was included on the board to provide digital I/O for use on control panels. When the system is used in an industrial environment, switches can be read and LEDs driven by the digital I/O port. In addition, the digital I/O was used for debugging purposes.

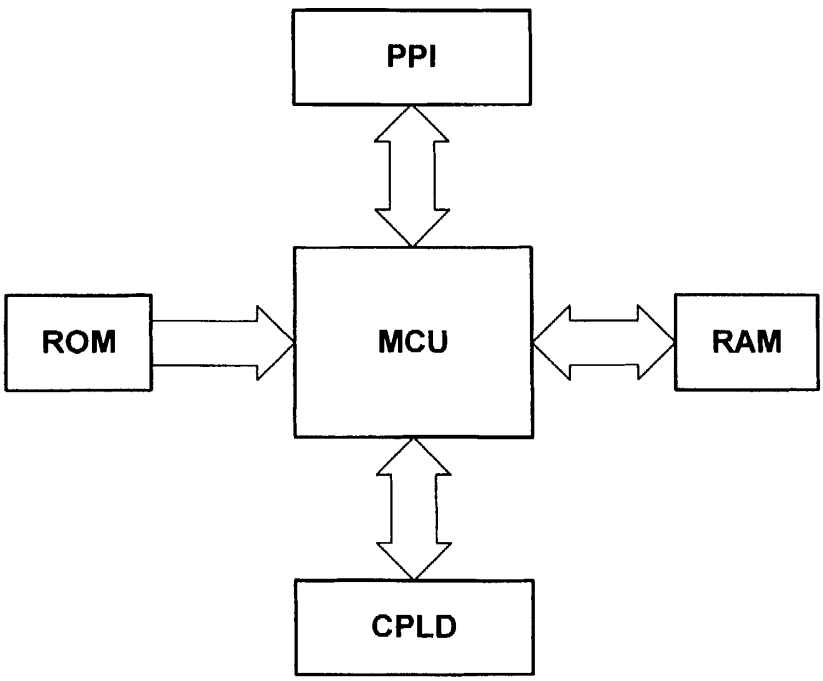


Figure 2.14 : Digital controller module

Signals from the microcontroller need to be decoded for writing to and reading from the RAM or to address a peripheral such as the PPI. These signals can be generated by using discrete logic, but it was decided to use a Complex Programmable Logic Device (CPLD) instead since this improved the system's flexibility and saved a lot of board space.

2.11 Power Supply

The physical distance between the different nodes in the network requires that every node must have its own power source. A 12 volt gel-sealed lead-acid battery is the ideal solution since it has a capacity of 7 ampere hour and it is rechargeable. A switch-mode power supply should be used to maximize efficiency and reduce power losses to a minimum. The power supply should output three voltage levels. For the microcontroller and associated logic, 5V is required. The

ADC and DAC modules require +15V and -15V. An analytical approach can be followed to determine the current required by the system. This method involves calculating the average current required by every component in the system. These values are then added to calculate the total current consumed. A more effective way is to determine the average current required by the system experimentally.

2.11.1 Experimental setup

In order to determine the current capacity required from the switch-mode power supply, a linear power supply was used to drive the system. The current drawn by the system was measured and the results are shown in Table 2.1.

	+5V current (mA)	+15V current (mA)	-15V current (mA)
MCU	70	0	0
DCG	23	0	0
DAC	13	5	5
ADC	9	15	4
Total	115	20	9

Table 2.1 : System current consumption

2.11.2 Design requirements

As already mentioned, the system should be modular and transportable. The physical distance between nodes requires the use of lead-acid batteries at each node. These lead-acid batteries should last as long as possible; this requires the use of a switch-mode power supply. Besides a 5V output, the power supply should generate +15V and -15V to drive the analogue circuitry.

When used in remote locations, solar cells can be used to charge the batteries. The advantage is that such a system will recharge itself and will not require frequent service to replace or recharge batteries.

The key design requirements can be summarized as follows:

- High efficiency switch-mode power supply (>80%)
- Capable of generating 5V (150 mA), +15V (50 mA), and -15V (50 mA)
- Minimum effect on surrounding circuitry (interference).

2.11.3 Design

The LM2575 simple switcher from National Semiconductor [44] was chosen as the 5V switching regulator. This series offers a high-efficiency option for popular three-terminal linear regulators. The switching regulator requires a readily available off-the-shelf inductor. To generate +15V and -15V, the MAX743 from Maxim [45] was used. The choice is based on availability, previous experience with the device and the high efficiency of the device.

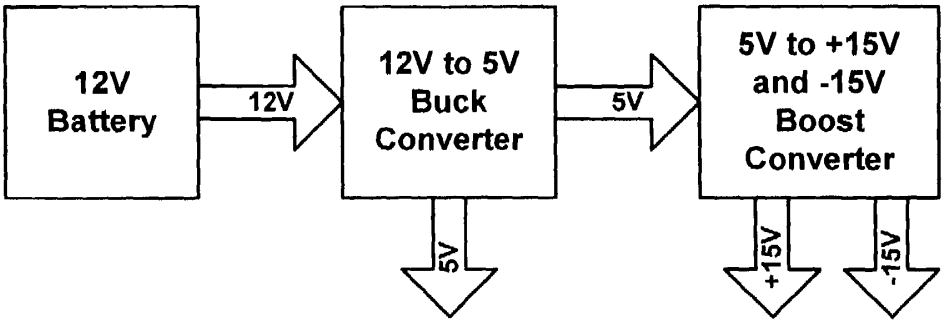


Figure 2.15 : Switch-mode power supply

A single LM2575 is capable of driving a 1A load, and has an efficiency of approximately 83% at full load. At typically expected operating conditions, the 5V supply delivers 150 mA at which the efficiency drops to 78%, still more efficient than a linear regulator.

The MAX743 generates the +15V and -15V for the analogue circuitry including the operational amplifiers. At typically expected operating conditions and a current consumption of 25 mA, the efficiency of the converter is 80%.

2.12 Backplane

The DAC-, ADC-, DCG-, MCU-, and PSU modules need to be connected to a common bus. All the modules slot into the backplane to connect the various modules to the system. This modular approach to construction simplifies troubleshooting of the system and minimizes downtime. A defective module can be replaced with a working one without disassembling the system.

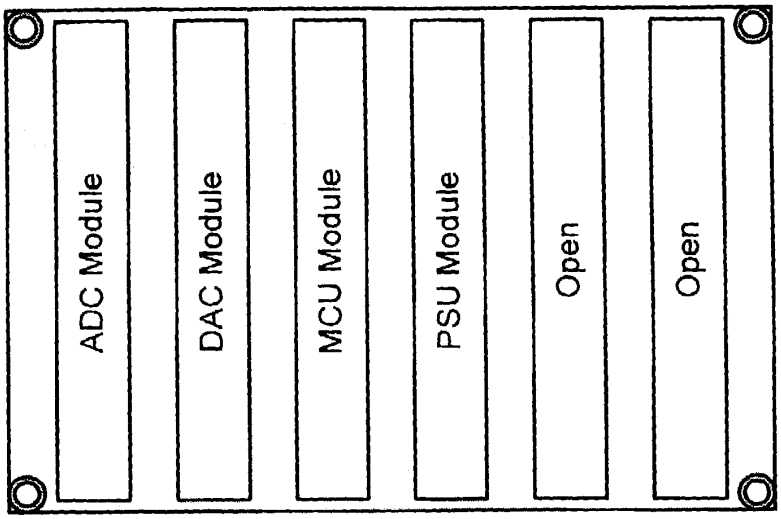


Figure 2.16 : Modules slotted into backplane

Modularity also makes it easy to expand or upgrade the system. If required, a module with digital I/O can be developed and added to the system. The digital controller module can be redesigned and replaced without affecting the rest of the system.

2.13 Enclosure

The purpose of the module enclosure is normally to protect the electronic circuitry from physical damage caused by everyday operation. In this system the metallic enclosure serves another more important purpose; it shields the system from electrostatic fields. Since this system is based on a 16-bit ADC and DAC, its resolution is 305 μV which makes it very susceptible to noise and EMI. By shielding the modules from EMI, noise can be limited to internally generated noise like the power supply and switching of digital electronics. The enclosure acts as a Faraday cage [46], shielding out stray electric fields. Noise voltages are induced in the shield and not in the electronics.

Chapter 3

Testing

One of the most important phases in the design loop is to test the completed design against the original specifications. This chapter discusses the various test experiments and methods used in practice and the custom tests developed for testing the developed measurement system. The three functions to be tested include communication, signal generation, and signal acquisition. The results of these tests are viewed in Chapter 4.

3.1 Data Communications

The communications test is a simple test to determine the efficiency of the data transfer process. The efficiency of the data transfer process is influenced by the transmission medium, the protocol used and the conversion electronics. Efficient data transfer ensures that the captured data are retrieved correctly the first time. This eliminates data retransmissions and the subsequent time delays.

3.1.1 Setup

The setup for the communication test is shown in Figure 3.1. The data signals from the personal computer are converted from electrical RS-232 to optical, compatible for use in the optic fibre. From this point onward the system is galvanically isolated from the personal computer. The nodes in the network are connected in a ring topology and the test network consists of four nodes. Any node in the network can function as a waveform generator, waveform digitizer, or both. For testing purposes the first node in the network is set up as a waveform generator while all other nodes are set up as waveform digitizers.

3.1.2 Method

The communication efficiency of the measurement system is tested by transmitting data to the hardware and then retrieving the data from the hardware. An 8K waveform with random values is generated on a personal computer and sent to the measurement hardware. These data are then retrieved from the hardware and compared with the original file to determine if any data transfer errors occurred.

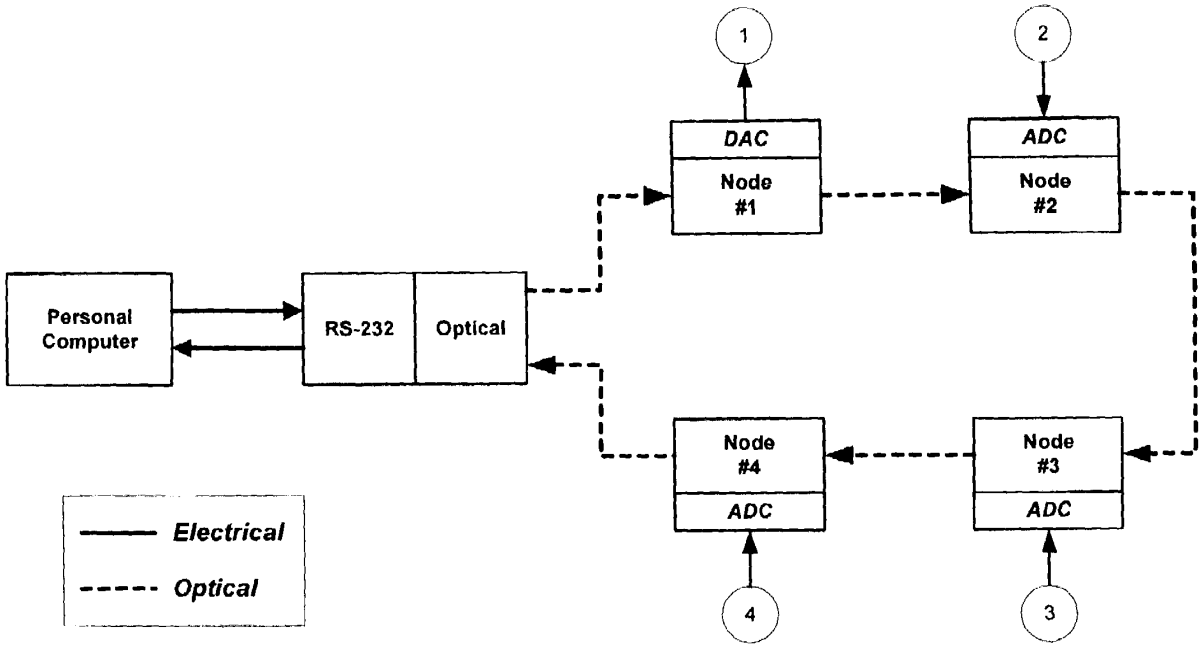


Figure 3.1 : Communication test setup

Figure 3.2 shows the format of a data packet. The data packet to be transmitted consists of the header and the data. The header section contains eight bytes; the destination, instruction, source, and five tag fields. The data section contains 64 bytes of data. To download a complete waveform to the hardware, 128 packets must be transmitted. This transfers 8192 bytes of data, or 4096 integer values (16-bit values).

Destination	Instruction	Source	Tag 1	Tag 2	Tag 3	Tag 4	Tag 5	Data 0	.....	Data 63

Figure 3.2 : Data packet format

As stated in the previous paragraph, 64 bytes of data require 8 bytes of overheads. Thus every 8K bytes of data is accompanied by 1K bytes of overheads. To test the transfer efficiency, 8K bytes of waveform data are transmitted to the hardware where it is stored. The data are now read from the hardware and compared with the original data to determine if any errors occurred. This process is repeated 16 times for a total of 128K bytes (or 1M bits) of data.

The Bit Error Ratio (BER) is the most common measure of error performance on a data circuit and is defined as the probability that a bit is received in error [47].

$$BER = \frac{Errors}{Total\ Number\ of\ Bits} \qquad (3.1)$$

It is also called the bit error rate. In these tests the number of bits received in error is divided by 1M bits to determine the BER, which is expressed as a coefficient and a power of ten, for example BER $< 1 \times 10^{-6}$. This implies that less than one out of one million bits is received in error.

3.2 Digital Clock Generator

The analogue input module is used to digitize waveforms and the analogue output module is used to generate waveforms. These two modules make use of an analogue-to-digital and a digital-to-analogue converter respectively. Both these data converters require a clock signal to operate. This clock signal also ensures that the signal generation and signal acquisition occur synchronously. The digital clock generator module is used to generate the clock signal and should be tested before testing any of the data converter modules. A thorough test of the digital clock generator (DCG) module is of utmost importance since the system timing accuracy will completely depend on the accuracy of the DCG. Once the digital clock generator is tested, the other modules can be tested.

3.2.1 Setup

The hardware setup to validate the digital clock generator module is shown in Figure 3.3.

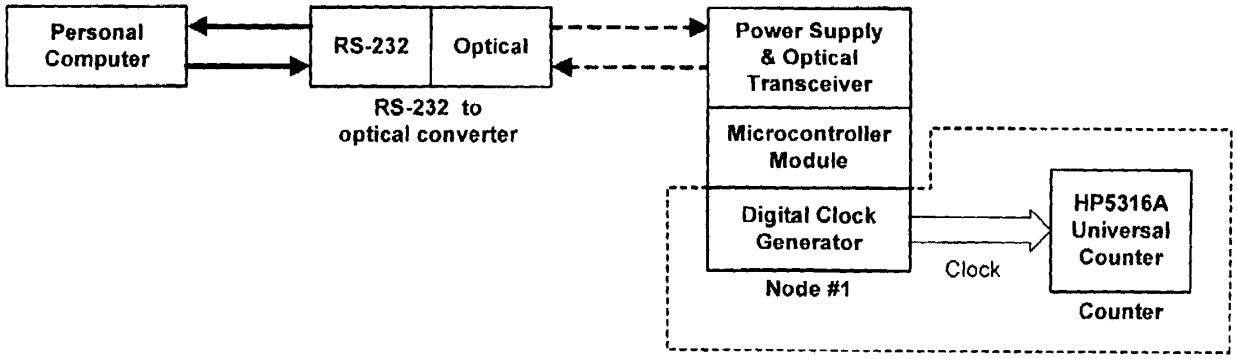


Figure 3.3 : Digital clock generator test setup

3.2.2 Method

The digital clock generator was tested by presetting it with a sampling frequency by means of a program on the personal computer. A universal counter from Hewlett Packard, the HP5316A, was used to measure the generated frequency. This counter displays the measured frequency up to eight significant figures. This process was repeated for several frequencies from 1 Hz up to 500 kHz.

3.3 Waveform Generation

The heart of the waveform generator module is the digital-to-analogue converter. The DAC generates an analogue voltage in the range -10V to +10V with 16-bit resolution. One bit change represents a change in voltage of 305 μV. In order to do a valid comparison test an oscilloscope or similar digitizing device with a resolution of at least 18 bits is required.

3.3.1 Setup

The hardware setup for the waveform generation test is shown in Figure 3.4.

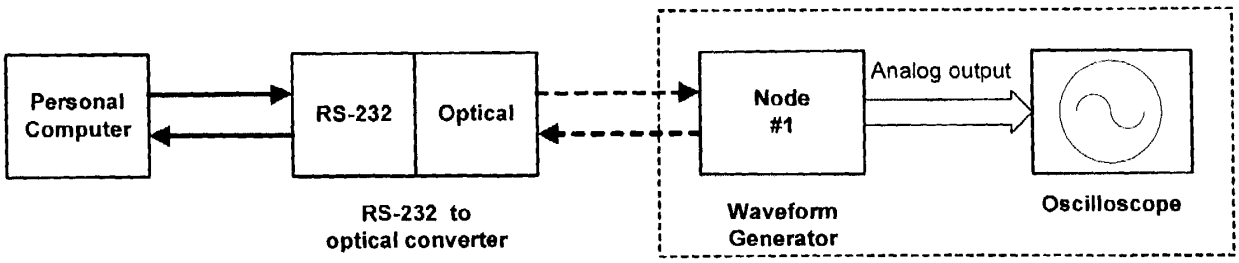


Figure 3.4 : Waveform generator test setup

3.3.2 Method

A pure sine wave with 16-bit accuracy is generated in software by using a mathematical function. This waveform is downloaded to the memory bank of the hardware. The software on the host PC triggers the start of signal generation event and the digital-to-analogue converter converts the stored waveform to analogue voltages between -10V and +10V. The oscilloscope is connected to the analogue output channel to measure the generated waveform. A high resolution digital storage oscilloscope should be used since the data must be downloaded to a personal computer for further analysis using a mathematical software package such as Matlab.

3.3.3 Results

This test could not be conducted in the laboratory since the available oscilloscopes only have 8-bit resolution which is not sufficient to test a high resolution system. The Agilent 54621 [48] and the LeCroy Wavesurfer 422 [49] both have vertical resolutions of only 8-bits. To overcome this problem an alternative test must be designed.

3.4 Waveform Digitization

The most important component in the waveform digitizer is the analogue-to-digital converter. The ADC converts the -10V to +10V analogue input voltage to a 16-bit digital value. The resolution of the digitizer is 305 µV. In order to test this device successfully, a precision signal generator and an oscilloscope with a vertical resolution of at least 16 bits is required.

3.4.1 Setup

Figure 3.5 shows the hardware setup for testing the waveform digitizer module.

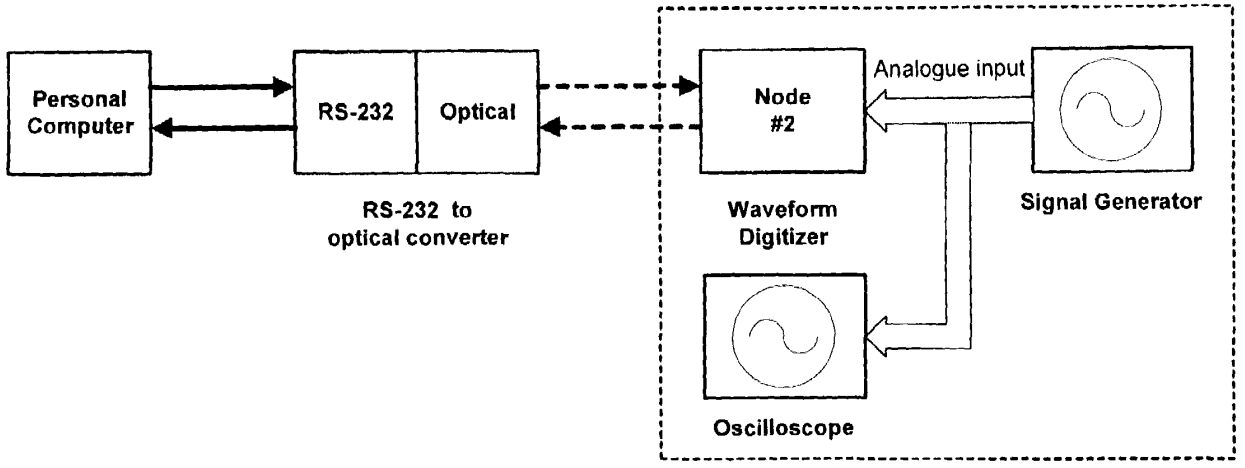


Figure 3.5 : Waveform digitizer test setup

3.4.2 Method

A signal generator with a resolution of 16 bits or better is used to generate a sine wave. This sine wave is captured by the waveform digitizer module. At the same time this waveform is also captured by a high resolution digitizer. These two waveforms are analyzed and compared to determine the relative accuracy of the digitizer module. A mathematical software package is used to analyze the data on a personal computer.

3.4.3 Results

This test could not be conducted in the laboratory since the available oscilloscopes only have 8-bit resolution which is not sufficient to test a high resolution system. The Agilent 54621 and the LeCroy Wavesurfer 422 both have vertical resolutions of only 8-bits. To overcome this problem an alternative test must be designed.

3.5 Grounded Inputs Test

In order to test the noise internal to the waveform digitizer, the differential inputs are connected to ground and samples are taken.

3.5.1 Setup

Figure 3.6 shows the test setup for the grounded inputs test. The differential inputs to the instrumentation amplifier are connected together and to ground via two 10 kΩ resistors. The bias currents of the instrumentation amplifier can move the voltage level of the floating source out of the valid range of the input stage of the analogue-to-digital converter. This voltage is anchored to a reference by means of these two resistors, called bias resistors. The function of these resistors is to provide a DC path from the instrumentation amplifier inputs to ground.

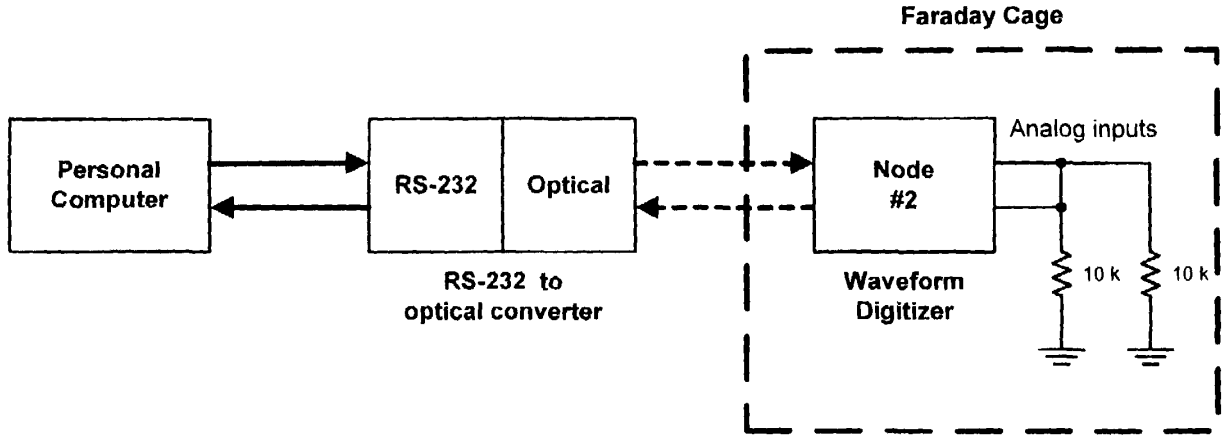


Figure 3.6 : Grounded inputs test setup

The complete node consisting of the battery, power supply, optical transceiver, digital clock generator, digital controller module and waveform digitizer are placed inside a Faraday cage to eliminate EMI noise. Each of these modules is shielded by a copper enclosure connected to ground to shield electric fields and an internal mild steel plate to shield electromagnetic fields.

3.5.2 Method

Once the setup is complete, all other sources capable of generating interference are switched off. This includes oscilloscopes, computer screens, fluorescent lights, electric fans and ceiling fans. Next the data acquisition process is started and 4096 samples are taken. Since the goal of this experiment is to determine the noise internal to the system, no input signal is applied to the differential inputs, these inputs are shorted.

3.6 Back-to-back Test

To test the functionality of this high resolution measurement system, the waveform generator and waveform digitizer need to be tested individually. For the purpose of this study it is sufficient to test the system as a whole instead of each individual component. The back-to-back test is a simple yet effective test which can be conducted to test the system. This test tests the waveform generation and the waveform digitization functions of the system and gives the total error introduced by waveform generation and waveform digitization. For more accurate testing and calibration of this system, further testing in an advanced laboratory needs to be done.

3.6.1 Setup

Figure 3.7 shows the hardware setup for the back-to-back test.

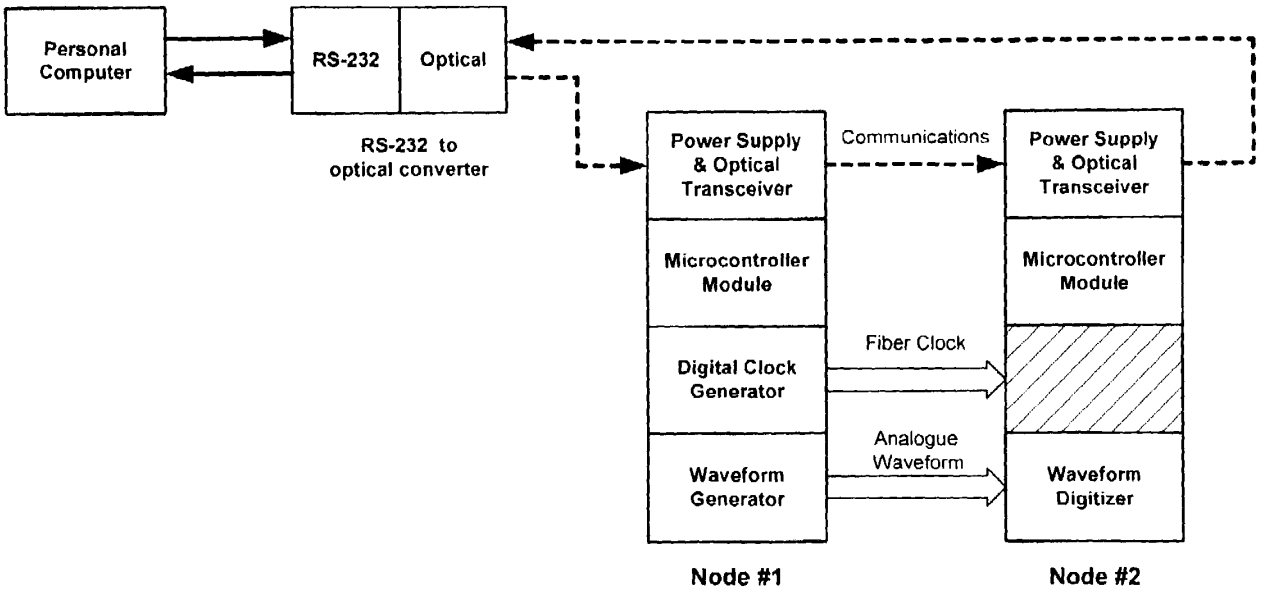


Figure 3.7 : Back-to-back test setup

3.6.2 Method

The back-to-back test was done by implementing two nodes. The first node contains a digital-to-analogue converter (DAC) and the second node contains an analogue-to-digital converter (ADC). A pure sine wave is generated on the personal computer and this waveform is sent to the DAC. Next the frequency of the digital clock generator (DCG) is set and the digital clock generator is started. Signal generation by the DAC and signal measurement by the ADC occur synchronously by means of the clock signal distributed via optical fibre.

3.6.3 Conclusion

To test a high accuracy measurement system such as this 16-bit system requires sophisticated equipment. In order to evaluate a 16-bit waveform generator, a digital storage oscilloscope or waveform digitizing device with a resolution of better than 16 bits is necessary. These instruments are not available in a standard laboratory and are costly.

One solution is to buy a moderately low cost data logger with 16-bits resolution. A company named Picotech Technology Limited offers a 16-bit PC oscilloscope with 1% accuracy, the ADC-216 [50]. This instrument offers 32KB of internal memory and can acquire samples at a tempo of 333 ksps. The cost of this hardware along with the software is R5 783-00. This is a very cost effective solution for validating a high resolution measurement system. Unfortunately this product was released recently and was not available when these tests were done.

To test the basic integrity of the system, a back-to-back test is done. A precision sine wave is generated in software and downloaded to the waveform generation hardware. As the waveform generator outputs the analogue waveform, the waveform digitizer captures it. The captured data are retrieved from the waveform digitizer hardware and saved on the personal computer. These data are then compared to the original data and the difference represents the combined errors introduced by the waveform generation module and waveform digitization hardware.

Chapter 4

Results

The previous chapter discussed the various tests conducted to test the various functions of the measurement system. Communication, waveform generation and waveform acquisition are the most important features to be tested. Results from these tests and further processing done on the data are viewed in this chapter.

4.1 Data Communications

The baud rate for data communications between network nodes and the personal computer is set at 19200 bps. This data rate is the maximum achievable rate for the 18.432 MHz crystal and plastic fibre used. Figure 4.1 shows the transfer times of data in the system. A baud rate of 19200 bps translates to one bit every 52.08 microseconds. Since every data byte is accompanied by a start bit and a stop bit, the total time to transmit one byte of data is 521 microseconds.

The packet structure used consists of an eight byte header and a 64 byte data field. Thus, a complete packet consists of 72 bytes which takes 37.5 ms to transmit. The waveform file contains 4096 integer (16-bit) values or 8192 bytes of data. To transfer a complete waveform, 128 packets of data need to be sent and the duration of this transfer is 4.8 seconds.

The transfer time of 4.8 seconds can be achieved if there are no delays between successive bytes or packets. Delays were inserted between successive packets and this increased the transfer time significantly. The delay gives the microcontroller time to inspect packet n before packet $n+1$ is received. Based on the result, the packet is either interpreted or passed on to the next node in the network. The duration of this delay was determined by experimenting with different delays and the best results were obtained with a delay of 115 milliseconds.

Figure 4.2 shows a packet being transmitted. As mentioned previously, a data packet consists of an 8-byte header and a 64-byte data field. The total 72 bytes are transmitted in 39.2 milliseconds which is consistent with the predicted time. Every data packet is followed by a processing delay of 115 milliseconds as seen on the screenshot.

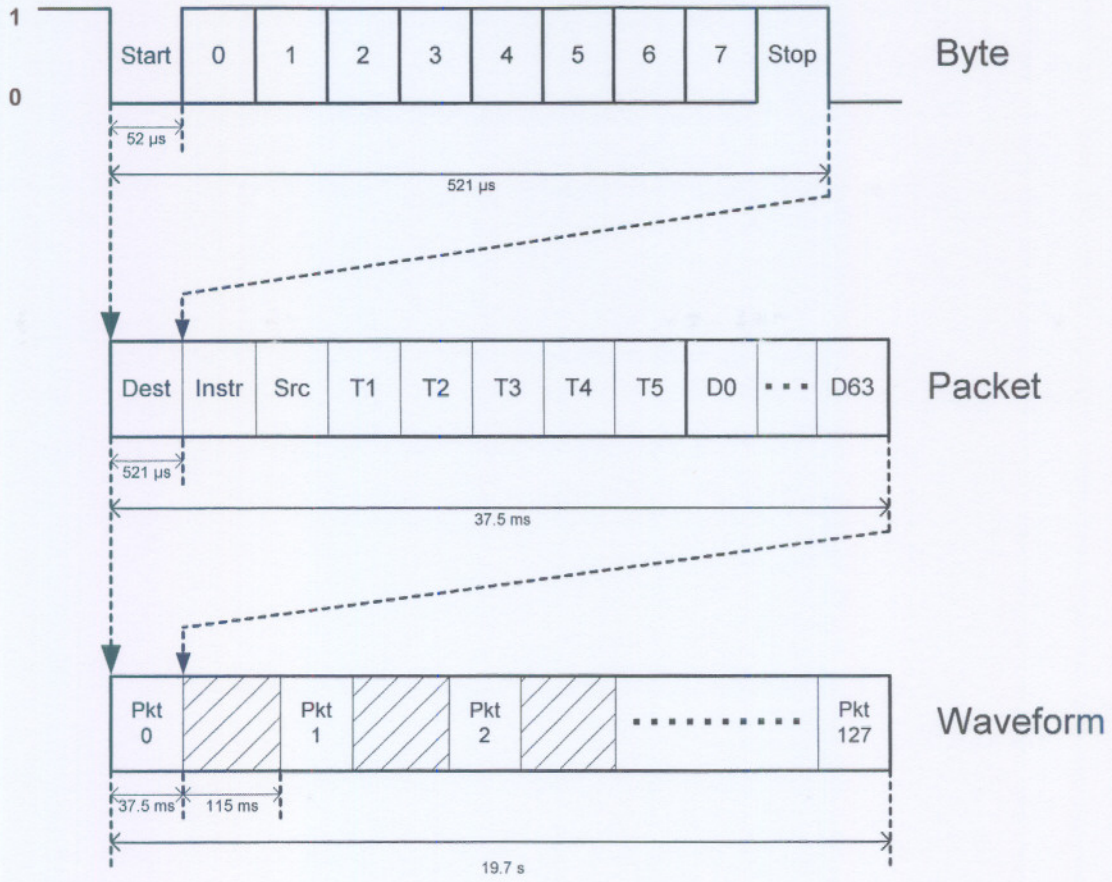


Figure 4.1 : Data communications

Figure 4.3 is a screenshot of an actual 8 Kb waveform file transfer. The duration of a waveform file transfer was measured to be 19.70 seconds. This fourfold increase in transfer time is due to the processing delay inserted between successive packets.

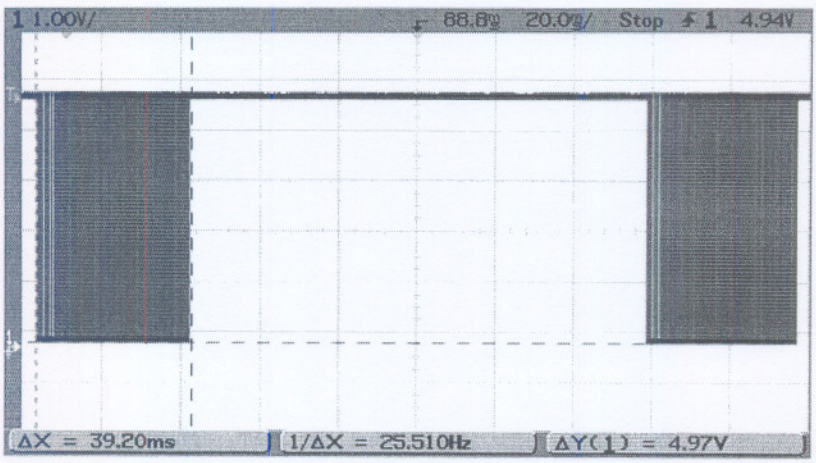


Figure 4.2 : Transmission of packet

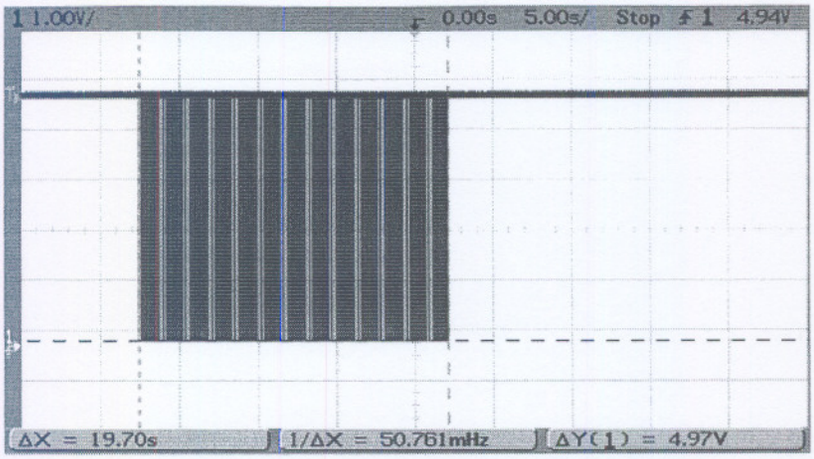


Figure 4.3 : Transmission of waveform

The results of the data transfer to the measurement hardware are shown in Table 4.1.

Unit to transfer	Time
Byte	521 µs
Packet	39 ms
Delay	115 ms
Packet + Delay	154 ms
9K bytes	19.7 s

Table 4.1 : Summary of transfer times

The waveform data were transferred in 19.7 s, each packet containing 64 bytes of waveform data and 8 bytes overheads. When a waveform is sent to the hardware, 1 KB of overheads accompanies the 8 KB of data. This translates to an overhead of 11.11 %. In order to test the effectiveness of the data communications, a test was set up. During this test a randomly generated waveform was generated on the personal computer and sent to the hardware. The next step was to retrieve the data from the hardware and to compare it with the original generated file. The results of this test are shown in Table 4.2.

Amount of data transferred	1 Megabit
Transfer time	320 seconds
Throughput	3.2 Kbit/s
Number of errors	0
BER	$< 1 \times 10^{-6}$

Table 4.2 : Communication test results

This test was repeated 100 times and no errors were encountered. This can be attributed to the high efficiency and noise immunity of the optic fibre.

4.2 Digital Clock Generator

Testing of the digital clock generator includes a test of the master clock and a test of the local clock. A node contains a master clock if the digital clock generator module is part of the node electronics. This clock is distributed to the rest of the network via optical fibre and reshaped at each node. The reshaped clock signal is known as the local clock. These two clock signals are shown in Figure 4.4.

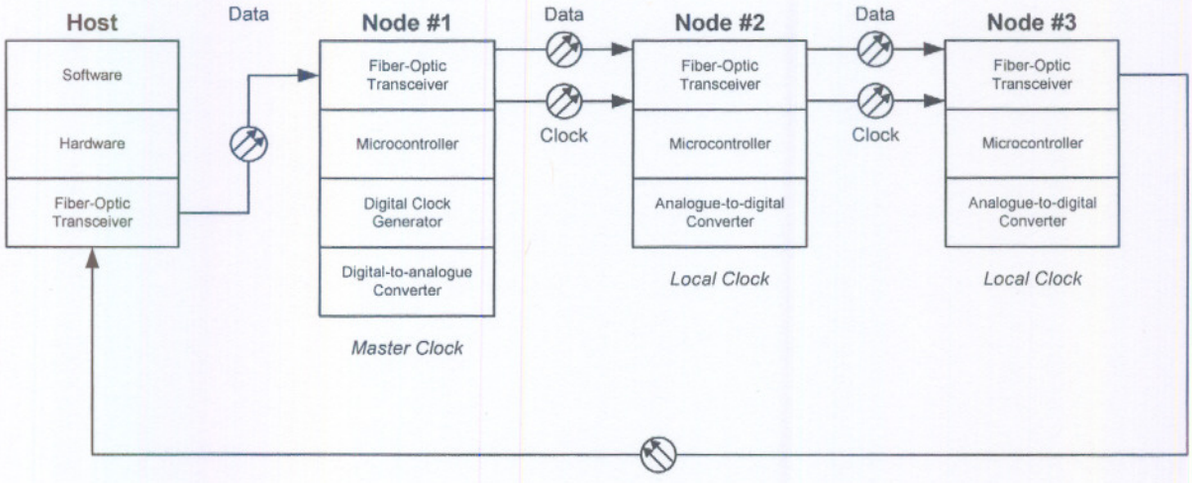


Figure 4.4 : Master clock and local clock

4.2.1 Master clock test

As stated in Chapter 3, the digital clock generator (DCG) module determines the accuracy of both waveform generation and waveform digitization. The DCG module is tested first to ensure proper operation of the DAC and ADC modules. The DCG was programmed to generate clock signals with different frequencies and the frequency was measured by a Hewlett Packard HP5316A universal counter as described in Chapter 3. Screenshots are shown for the DCG programmed for 50 kHz (Figure 4.5) and 200 kHz (Figure 4.6) operation.

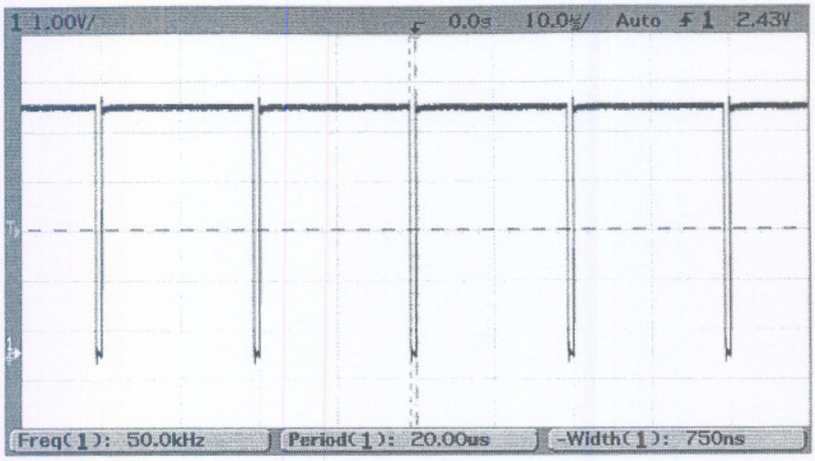


Figure 4.5 : Digital clock signal at 50 kHz

The tests for determining the accuracy of the DCG were done at 20 °C and at various clock frequencies. The range of the clock frequencies used in the test vary from 1 Hz to 500 kHz but can be set even lower or higher by replacing the crystal oscillator on the DCG module. The results of the test are shown in Table 4.3.

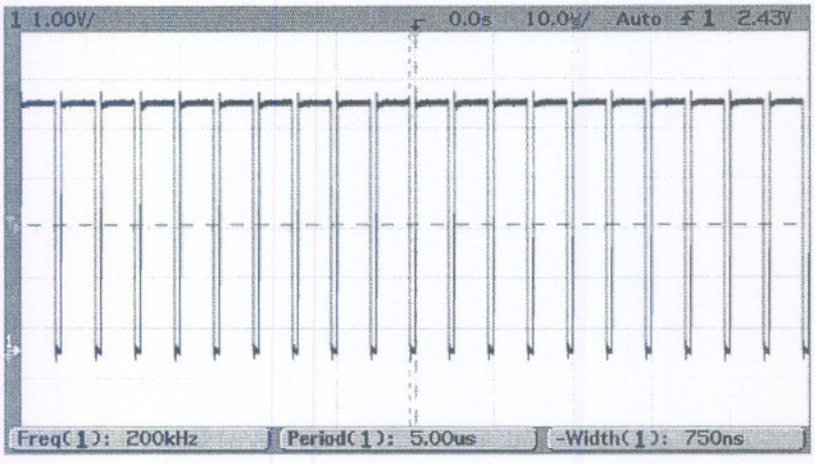


Figure 4.6 : Digital clock signal at 200 kHz

The error was calculated by rounding the result to four significant figures. The average clock frequency error was calculated to be 0.00040% which is a 4 parts per million (ppm) error.

A CFPT-6106 [51] temperature compensated crystal oscillator (TCXO) manufactured by CMAC was used. This oscillator is highly stable and has a frequency stability of ±1.5 ppm. Since this crystal is temperature compensated, a variation in temperature would have an insignificant effect on the output frequency. Ageing of the oscillator causes an additional frequency drift of ±1 ppm per year. The manufacturing date of this specific crystal is February 2002 and thus the

drift due to ageing should be ±2.5 ppm. Summing the absolute values gives a total drift of 4 ppm which corresponds with the values obtained experimentally.

Preset frequency (Hz)	Measured frequency (Hz)	Error (%)	Temperature (ºC)
1	0.999996	0.0004	20
5	4.99998	0.0004	20
10	9.99996	0.0004	20
50	49.999801	0.0004	20
100	99.9996	0.0004	20
500	499.99801	0.0004	20
1000	999.996	0.0004	20
5000	4999.9801	0.0004	20
10000	9999.96	0.0004	20
50000	49999.802	0.0004	20
100000	99999.6	0.0004	20
200000	199999.21	0.0004	20
500000	499998.02	0.0004	20

Table 4.3 : Clock generator test results

The previous test measured the accuracy of the clock signal generated by the master DCG module. This clock signal must be distributed to the rest of the network in order to synchronize all nodes with a common clock signal. Galvanic isolation is obtained by using optic fibre between network nodes. The clock signal is distorted when it propagates through the optic fibre and must be reshaped at every network node to eliminate any glitches.

4.2.2 Local clock test

The effectiveness of the reshaping circuit is tested by comparing the clock signals at both ends of the optic fibre. Figure 4.7 shows the clock signal transmitted via optic fibre and Figure 4.8 shows the same signal after being reshaped by the reshaping circuit.

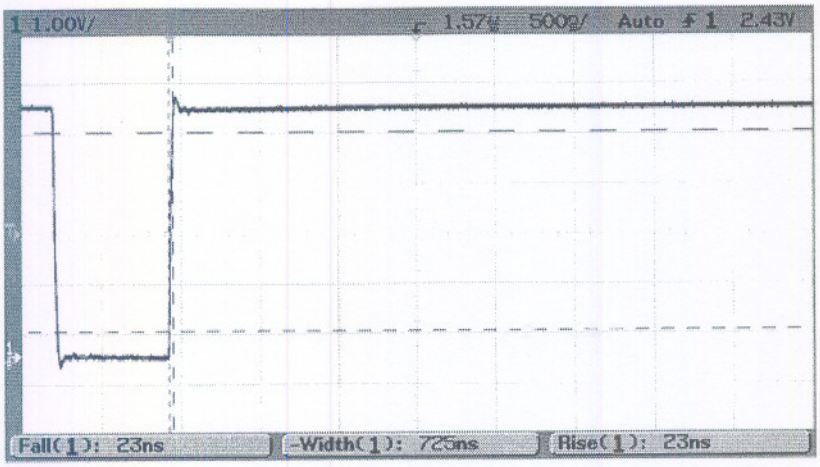


Figure 4.7 : Clock signal input to optic fibre

The width of the generated active low clock pulse is approximately 720 nanoseconds. This width is increased to approximately 4.4 microseconds by the reshape circuit. The main reason for increasing the width by this amount is to eliminate glitches. One consequence of the increase in width, is a decrease in maximum clock frequency.

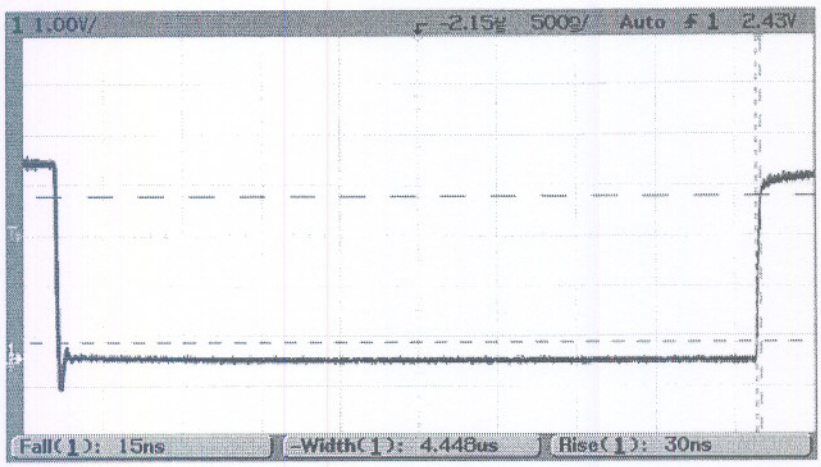


Figure 4.8 : Reshape circuit output

4.2.3 Conclusion

The DCG module was tested over the range 1 Hz to 500 kHz and proved to be accurate to 4 parts per million (ppm). Propagation of the clock signal via optic fibre and the subsequent reshaping limit the maximum clocking frequency to 200 kHz. This is not a drawback for the current system since the maximum sampling frequency for both the DAC and ADC is 100 kHz. This is still more than sufficient for the purposes as described in Chapter 1.

4.3 Waveform Generation

Although this test could not be done to the required accuracy, the Agilent 54621 oscilloscope was used to capture the generated waveform to 8-bit accuracy. A screenshot of the oscilloscope is shown in Figure 4.9.

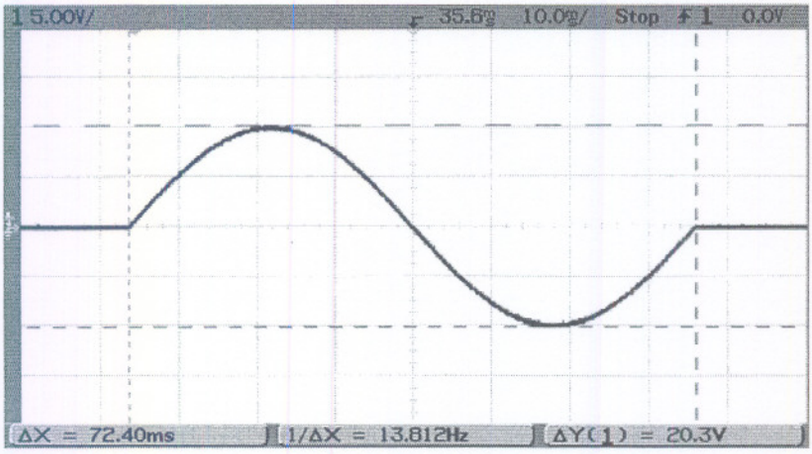


Figure 4.9 : Output of waveform generator module

4.4 Waveform Digitization

This test could not be conducted in the laboratory since the resolution offered by the available signal generator and oscilloscopes is not sufficient to test a high resolution system. The Agilent 54621 and the LeCroy Wavesurfer 422 both have vertical resolutions of only eight bits.

4.5 Grounded inputs Test

As stated before, the purpose of this test is to determine the noise internal to the waveform digitizer. The results of this test show the noise present when no external signal is applied and no EMI noise is present.

4.5.1 Captured signal

Figure 4.10 shows the signal captured by the waveform digitizer when the differential inputs are grounded. The maximum value of the signal is 41.3 mV and the minimum value is -31 mV. An offset voltage of 5.2 mV is present in this signal. This signal consists of noise generated by the circuit and noise picked up from the environment. The latter being the most significant.

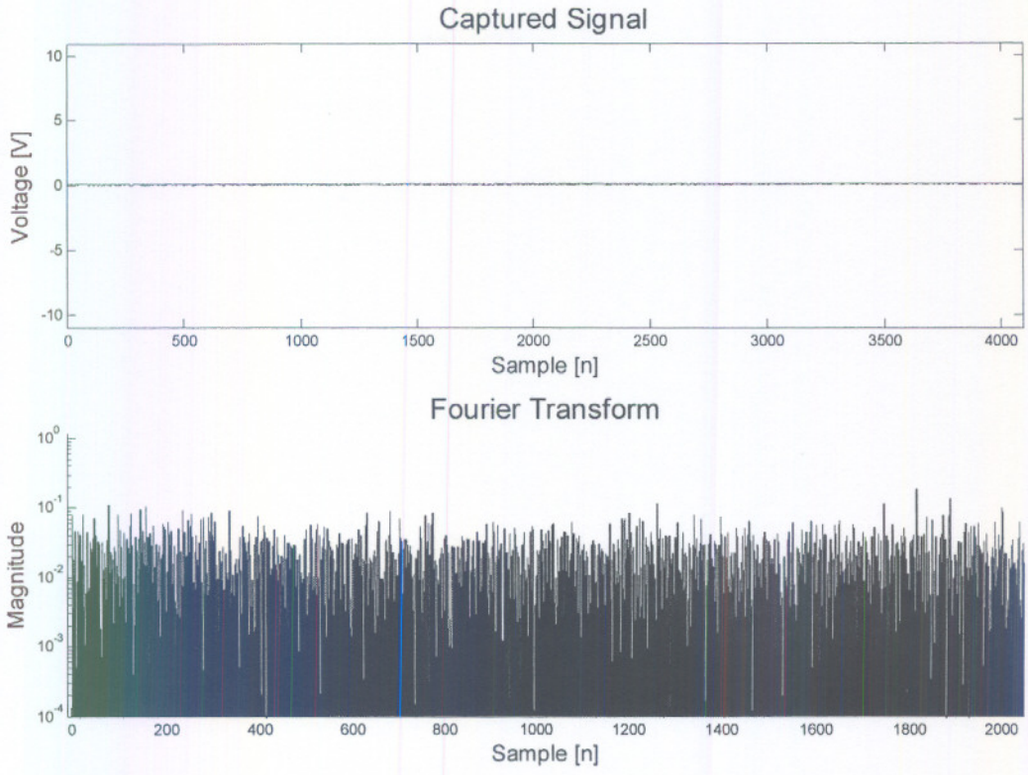


Figure 4.10 : Grounded Inputs Test

4.6 Back-to-back Test

Any particular node can function either as a signal generator or signal digitizer. For the purpose of the back-to-back test, two network nodes are used. Node number one is configured to generate a waveform and node number two is configured as a waveform digitizer. The output of the waveform generator is connected to the input of the waveform digitizer, hence the name back-to-back. This test illustrates the various errors introduced in the measurement system.

4.6.1 Original sine wave

First a high precision sine wave is generated on the computer by means of software. The precision of this sine wave is 64-bits and the IEEE double floating point data type is used, as shown in Figure 4.11. The frequency spectrum shows a large fundamental component and wideband noise of insignificant magnitude.

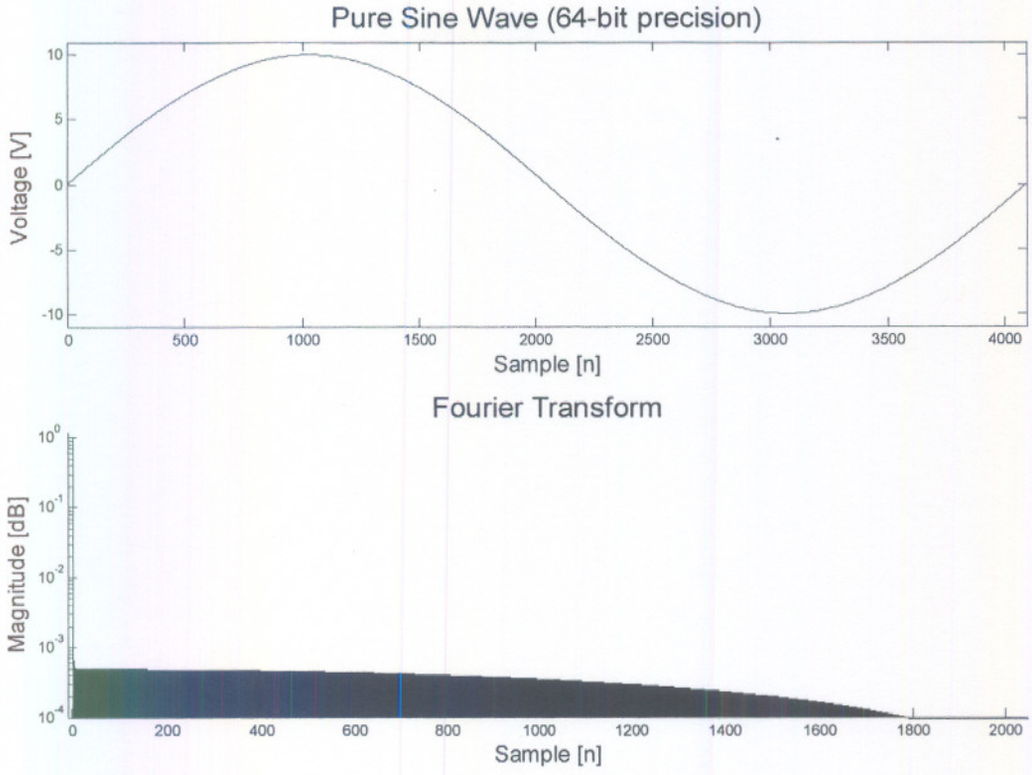


Figure 4.11 : Software-generated pure sine wave (Time and Frequency domain)

4.6.2 Rounded sine wave

The DAC on the waveform generator module requires its input data to be in 16-bit unsigned character format. This waveform is sent to the waveform generator node via optical fibre and stored in onboard memory. A single value of the waveform is transferred as two bytes, a low byte and a high byte. The DAC on the waveform generator node converts the stored waveform to an analogue signal. Figure 4.12 shows the 16-bit precision sine wave used as input to the DAC.

Although the fundamental component is evident in the frequency spectrum of the 16-bit sine wave, the rest of the spectrum deviates from the frequency spectrum of the 64-bit sine wave. Rounding errors introduced during the 64-bit to 16-bit conversion are responsible for this distortion.

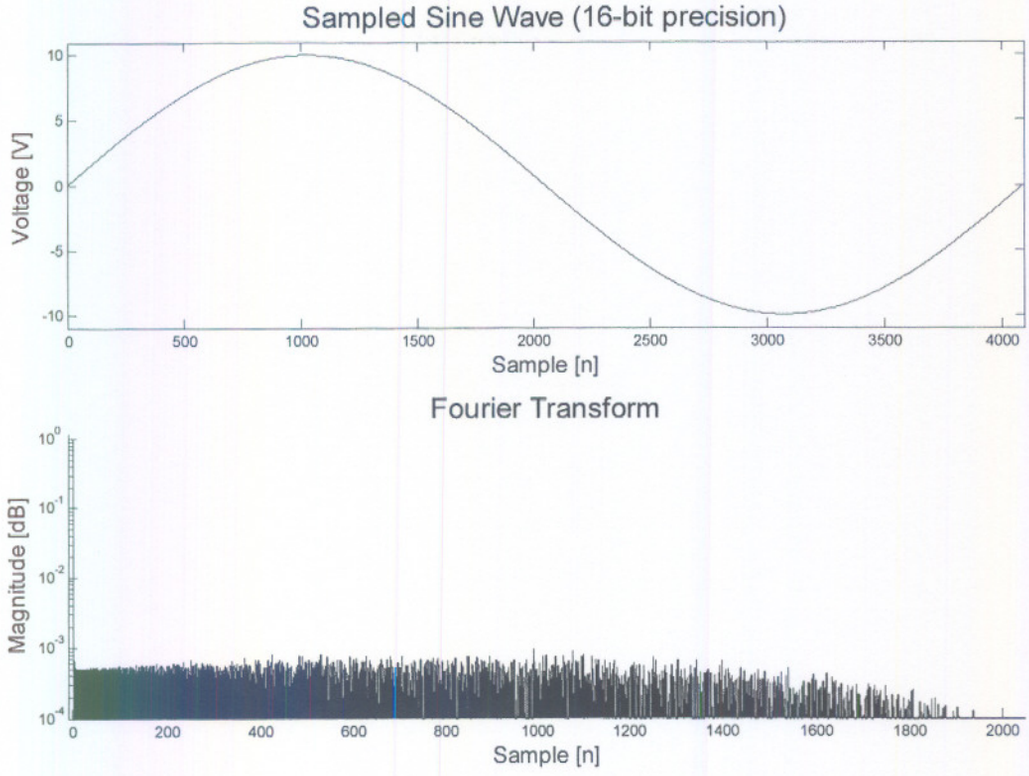


Figure 4.12 : Signal generated by DAC module (Time and Frequency domain)

4.6.3 Digitized sine wave

When the master clock is started, the 16-bit values stored in onboard memory are converted to analogue voltages from -10 V to 10 V. Since the output of the waveform generator module is connected to the input of the waveform digitizer, this waveform is digitized by the ADC on the waveform digitizer module. For every clock pulse, a digital value is converted to analogue and this analogue value is converted back to digital. This process is repeated for the whole waveform (4096 points) and the captured waveform is stored in the onboard memory of the waveform digitizer module.

A graphical user interface program is used to retrieve the captured data from the networked nodes. After downloading the data to the personal computer, the data are displayed graphically for easy interpretation. Data can now be saved as an 8K byte data file for later use. The structure of the data file is very simple and can be read by a mathematical package like Matlab for further processing. Figure 4.13 shows the digitized sine wave and its frequency spectrum.

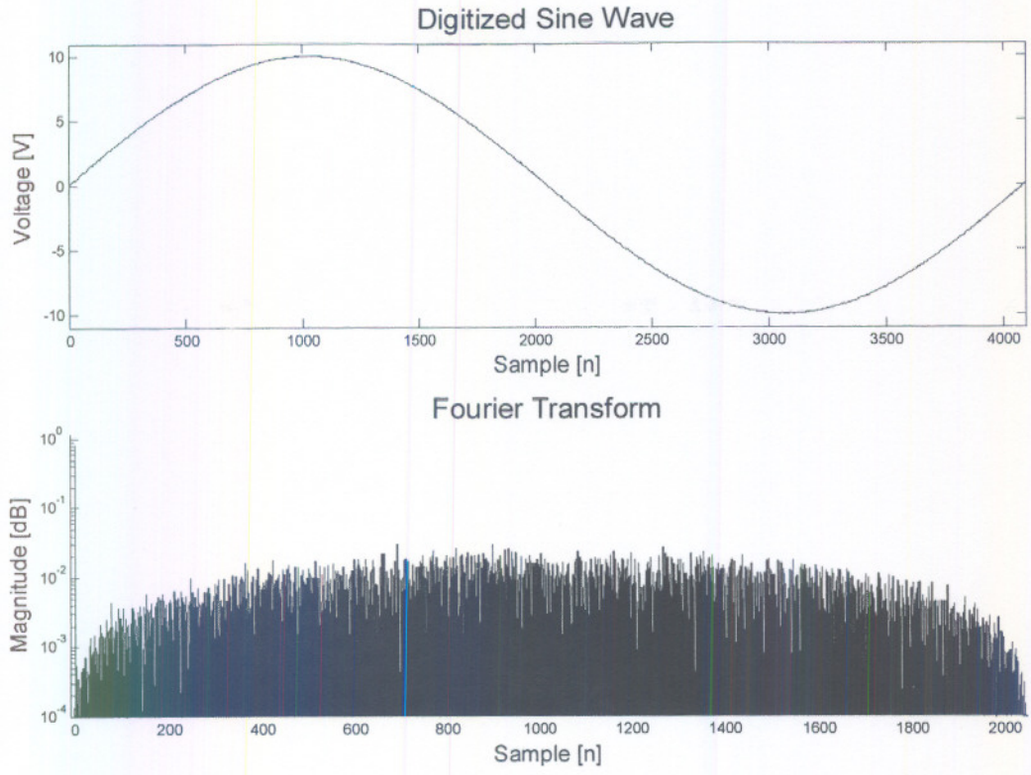


Figure 4.13 : Signal captured by ADC module

4.6.4 Errors

Errors introduced by rounding and noise are shown in Figure 4.14. Rounding errors are made when converting from a high precision variable (64-bit) to a lower precision variable (16-bit). The high precision sine wave was generated in Matlab to serve as a reference for subsequent comparisons with sine waves captured by the measurement system. The 16-bit precision sine wave was generated by the graphical user interface for the measurement system.

The noise in the DAC to ADC path is evident on the frequency spectrum in Figure 4.13. Because of the Gaussian distribution of noise, the noise is spread across the whole frequency spectrum.

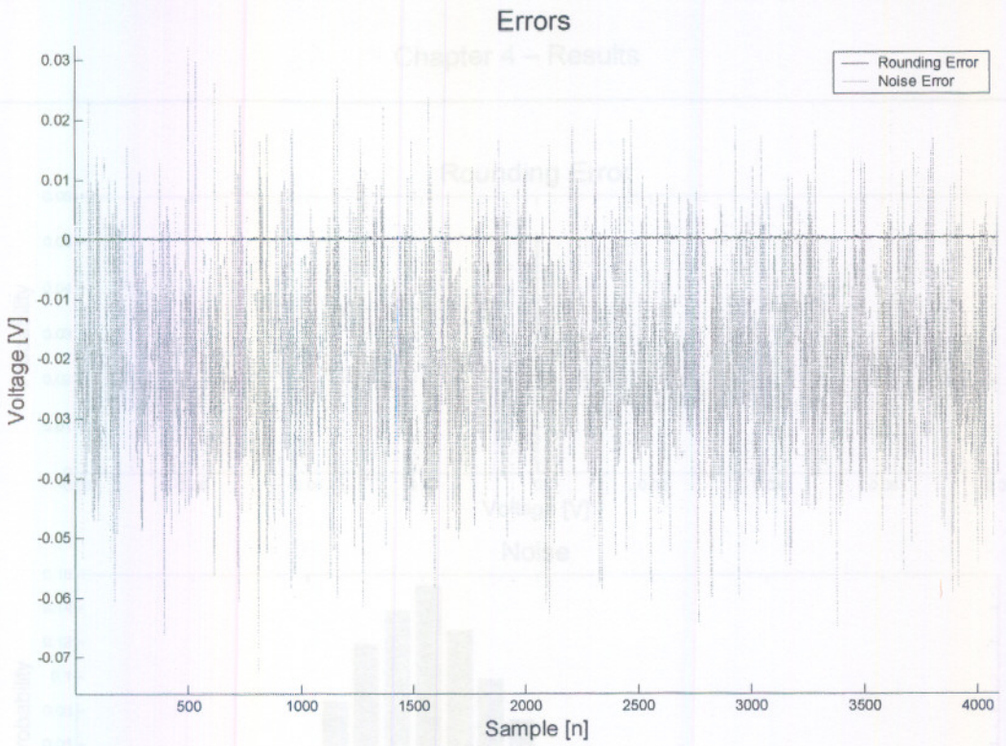


Figure 4.14 : Errors introduced by rounding and noise

Figure 4.14 shows plots of the rounding error and the error caused by noise in the system. The rounding error is very small compared to the noise. However, it is large enough to be analyzed further. The largest rounding error made is 305 μV and the average rounding error is 153 μV.

The noise in the system has a maximum value of 32 mV, a minimum of 79.8 mV and an average value of -19.7 mV. Total system noise is the sum of the rounding error and the noise introduced into the circuitry.

Figure 4.15 contains two histogram plots. From the top histogram it is clear that the distribution of the rounding error is uniform. The probability of the occurrence of a specific error amplitude is more or less the same for all the voltages centred around 150 μV. Probability distribution of the noise in the system is illustrated in the bottom figure. From this figure the normal distribution is evident. The median is determined to be -20 mV and values around this point are the most likely to occur. Probability of occurrence decreases exponentially away from this median.

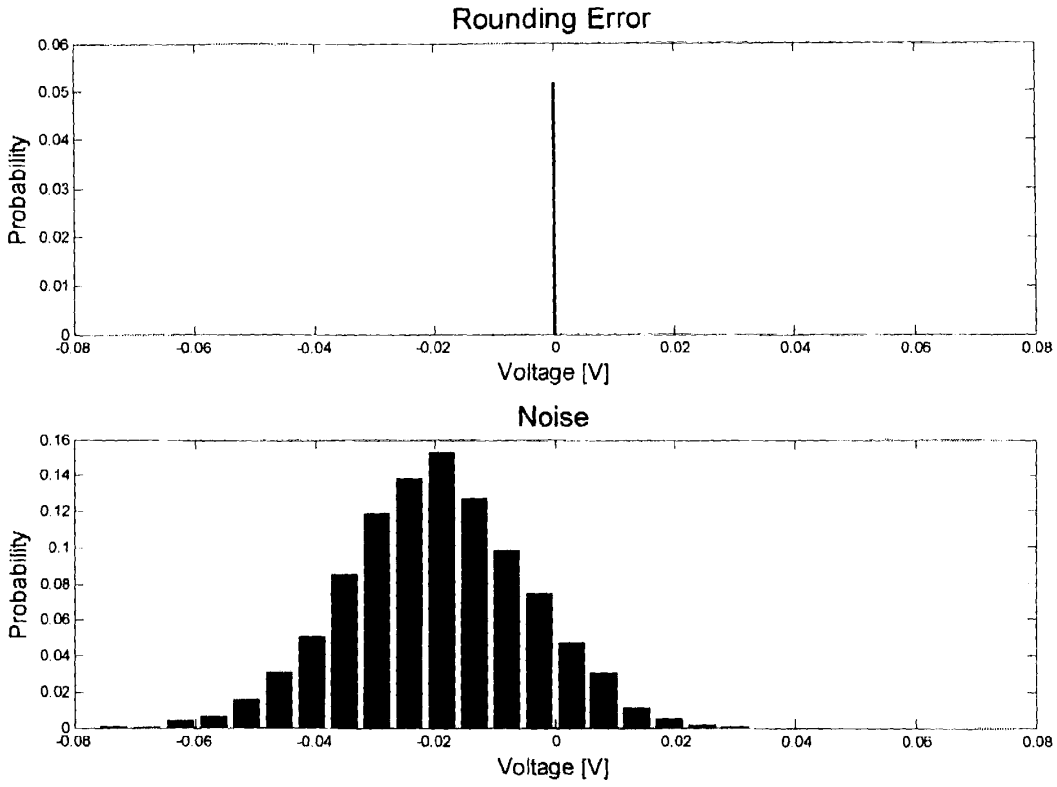


Figure 4.15 : Histogram plots of errors

Chapter 5

Conclusion

This chapter outlines what was accomplished in this project. A measurement system was developed and tested and the concept of a multi-node galvanic isolated measurement system was demonstrated successfully, but additional work needs to be done to improve the system.

5.1 Conclusion

This project was done based on a foreseen requirement in the industry. The requirement was to have a low cost high accuracy, high speed, galvanic isolated, synchronous measurement system to inject signals into a system and to measure signals in a system. Many off-the-shelf systems exist, but are either too complex for the intended purpose or too costly. The solution to this problem was to develop a low cost measurement system.

The user specifications served as the basis for developing technical specifications. Eventually the technical specifications and a literature study on possible solutions led to the design of the system. Design of this system was done by the functional description and functional allocation of the various functions to be performed.

A developed system should be tested to close the engineering design loop. Although a 16-bit data acquisition system requires high precision instruments for testing, simpler test were designed to test certain aspects of the system. These tests proved to be more than sufficient to illustrate the concept of a synchronous, multi-node, galvanic isolated measurement system.

5.2 Improvements

Although this system proved to be working well, several improvements can be made. The electronic industry is one of the fastest growing industries in the world. New products are developed and released every day. This makes it a challenge to choose optimal components for an electronic design. By the time the design is completed, several newer and better components are available. For instance, the sampling speed of the developed system is limited by the analogue-to-digital converter used on the waveform digitization module. By replacing this

older ADC with a newer version would solve this problem and increase the maximum sampling speed.

In order to keep the development cost of the system as low as possible, an 8-bit microcontroller was used in every network node to coordinate the various functions like data communications and data handling. The latest microcontrollers on the market offer superior performance over the DS89C310 used in this project and their price is only a fraction of the older chip. New architectures like the DSPIC from Microchip offer a DSP/PIC hybrid with enhanced features and increased clock speed, also at lower cost.

Through-hole components and double-sided printed circuit boards were used for all the modules since it is less costly and since this is an experimental design model. This design resulted in higher than expected noise in the system. In order to minimize the noise some improvements need to be made. Firstly, the circuit board of the ADC module must be redesigned by implementing high-speed digital design techniques to minimize noise. This board should be a multi-layered board with separate power, ground and signal layers [52]. Additionally, surface mount components should be used. This will also reduce the physical size of the modules.

The graphical user interface written to interface with the measurement hardware is capable of executing only a few basic functions. This software can be enhanced to generate and edit waveforms for injection and for further analysis of captured data.

The power supply can also be redesigned to obtain a more effective switch mode power supply [53]. Since this system makes use of rechargeable batteries, a more effective power supply would mean less frequent recharging of batteries.

5.3 Summary

Although some improvements can be made to the measurement system, the concept of the proposed measurement system was developed and demonstrated successfully. Now that the concept is illustrated, additional features can be added and existing features improved. Because of the modular design, the different modules can be redesigned individually without affecting the rest of the system. This makes it possible to retain the original working concept while improving the system systematically.

Appendix A

Manufacturer	Device	Resolution	Settling Time (us)	Interface	Package
Texas Instruments	DAC712	16	10	16 bit parallel	28 SOIC / PDIP
Texas Instruments	DAC714	16	10	Serial	16 SOIC / PDIP
Texas Instruments	DAC715	16	10	16 bit parallel	28 SOIC / PDIP
Texas Instruments	DAC716	16	10	Serial	16 SOIC / PDIP
Texas Instruments	DAC7631	16	10	Serial	20 SSOP
Texas Instruments	DAC7731	16	5	Serial	24 SSOP
Texas Instruments	DAC8501	16	10	Serial	8VSSOP
Maxim	MAX5200	16	1	Serial	10 uMAX
Maxim	MAX5204	16	25	Serial	10 uMAX
Maxim	MAX541	16	1	Serial	8 SOIC / PDIP
Maxim	MAX5441	16	1	Serial	8 uMAX
Maxim	MAX5541	16	1	Serial	8 SOIC / PDIP
Linear Tech	LTC1821	16	2	16 bit parallel	36 SSOP
Linear Tech	LTC1668	16	20n	16 bit parallel	28 SSOP
Linear Tech	LTC1650	16	4	serial	16 SOIC, PDIP
Linear Tech	LTC1599	16	2	16 bit parallel	24 SSOP
Linear Tech	LTC1597	16	2	16 bit parallel	28 SSOP
Linear Tech	LTC1596	16	2	serial	16 SOIC, PDIP
Linear Tech	LTC1595	16	2	serial	8 SOIC, PDIP
Linear Tech	LTC1592	16	2	serial	16 SSOP
Analog Devices	AD5660	16	8	serial	SOT-23
Analog Devices	AD7846	16	7	8/16 bit parallel	28 PDIP / PLCC
Analog Devices	AD7849	16	7	8/16 bit parallel	20 PDIP / SOIC
Analog Devices	AD660	16	6	8/16 bit parallel	24 PDIP / SOIC
Analog Devices	AD669	16	6	8/16 bit parallel	28 PDIP / SOIC
Analog Devices	AD5544	16	2	serial	28 SSOP
Analog Devices	AD766	16	1.5	serial	16 PDIP
Analog Devices	AD5541	16	1	serial	8 SOIC
Analog Devices	AD5542	16	1	serial	14 SOIC

Table A.1 : Digital-to-analogue converters

Appendix B

Manufacturer	Device	Resolution	Sampling Frequency	Interface	Package	INL	DNL
Texas Instruments	ADS7805	16	100 ksps	16 bit parallel	28 PDIP	3	1
Texas Instruments	ADS7809	16	100 ksps	serial	20 SOIC	0.003	1
Maxim	MAX1188	16	135 ksps	8 bit parallel	20 TSSOP	2	1
Maxim	MAX1189	16	135 ksps	16 bit parallel	28 TSSOP	2	1
Maxim	MAX1166	16	165 ksps	8 bit parallel	20 TSSOP	2	1
Maxim	MAX1162	16	200 ksps	serial	10 uMAX	2	1
Maxim	MAX1132	16	200 ksps	serial	20 SSOP	1.5	1
Linear Tech	LTC1605	16	100 ksps	16 bit / 8 bit parallel	28 PDIP	2	1
Linear Tech	LTC1864	16	150 ksps	serial	8 SOIC	2	1
Analog Devices	AD7684	16	100 KSPS	serial	8 SOIC	3	1
Analog Devices	AD977	16	100 KSPS	serial	20 PDIP	1	1
Analog Devices	AD677	16	100 KSPS	serial	28 PDIP	1	1
Analog Devices	AD676	16	100 KSPS	parallel	28 PDIP	1	1
Analog Devices	AD976	16	100 KSPS	parallel	28 PDIP	1	1

Table B.1 : Analogue-to-digital converters

Appendix C

Hardware

C.1 Hardware design

This section includes schematics of the measuring system design. These schematics are fully documented and the following figure shows where each schematic fits in.

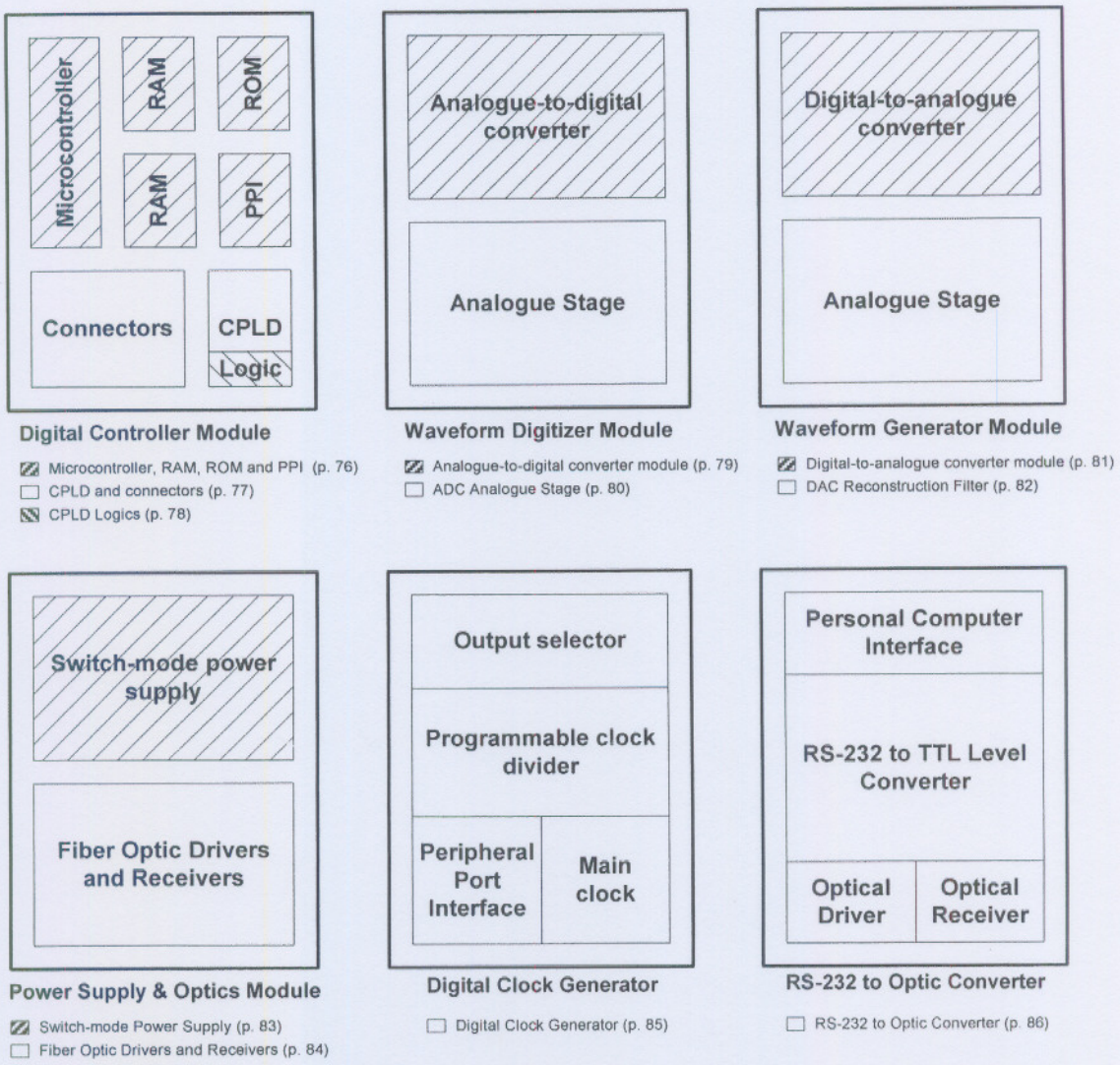
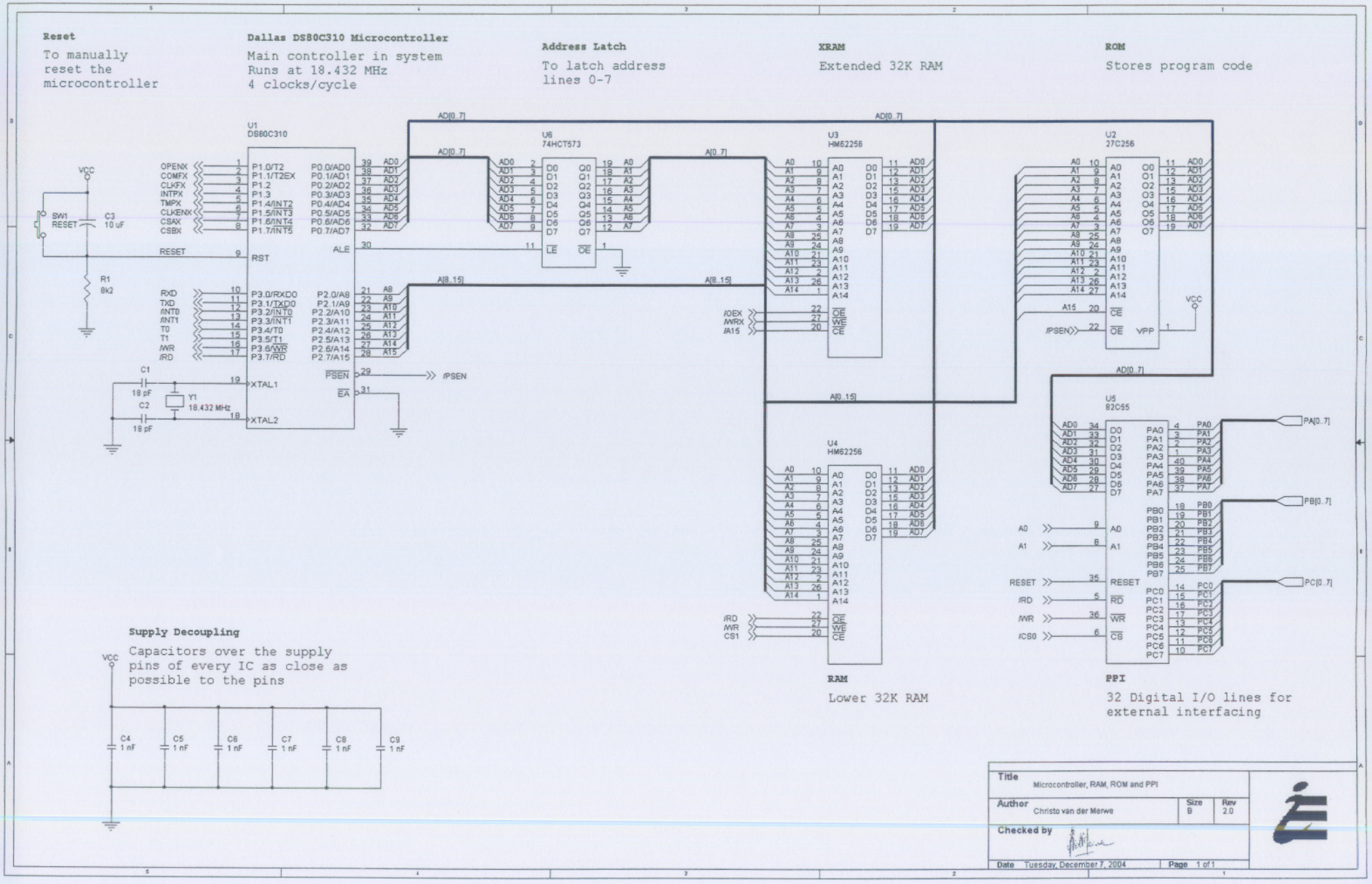
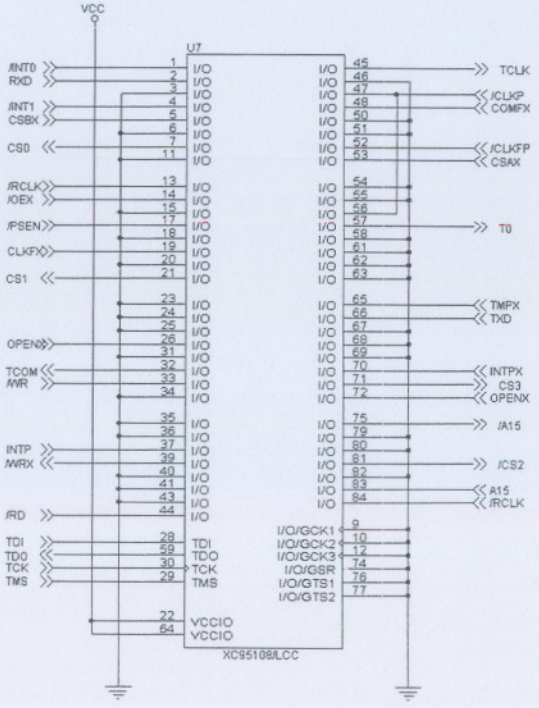


Figure C.1 : Overview of schematic diagrams


Reset
To manually reset the microcontroller
Dallas DS80C310 Microcontroller
Main controller in system
Runs at 18.432 MHz
4 clocks/cycle
Address Latch
To latch address lines 0-7
XRAM
Extended 32K RAM
ROM
Stores program code
U1
DS80C310
U6
74HCT573
U3
HM62256
U2
27C256
U4
HM62256
U5
82C55
SW1
RESET
C3
10 uF
R1
8k2
C1
18 pF
C2
18 pF
Y1
18.432 MHz
AD[0..7]
A[8..15]
A[0..15]
/PSEN
/IOEX
/MWRX
/IA15
/RD
/WR
CS1
RESET
/RD
/WR
/CS0
A0
A1
PA[0..7]
PB[0..7]
PC[0..7]
RAM
Lower 32K RAM
PPI
32 Digital I/O lines for external interfacing
Supply Decoupling
Capacitors over the supply pins of every IC as close as possible to the pins
C4 1 nF
C5 1 nF
C6 1 nF
C7 1 nF
C8 1 nF
C9 1 nF
Title
Microcontroller, RAM, ROM and PPI
Author
Christo van der Merwe
Size
B
Rev
2.0
Checked by
Date
Tuesday, December 7, 2004
Page
1 of 1

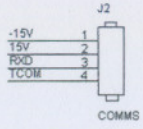
Complex Programmable Logic Device (CPLD)

The XC95108 CPLD contains all the glue logic used on the digital controller module. The device is in-circuit reprogrammable and can be programmed and debugged via the JTAG port

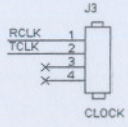


Auxiliary Connectors

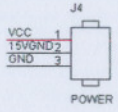
Connects module to system bus



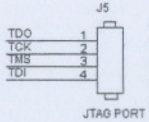
Communications
Analogue supply



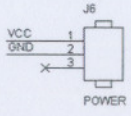
Sampling Clock



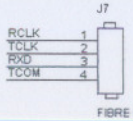
Digital supply (5V)
Analogue ground
Digital ground



JTAG Port for programming CPLD
Test Data Out
Test Clock
Test Mode Select
Test Data Input



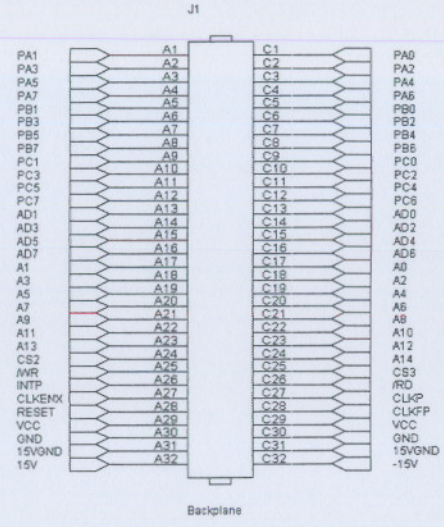
Digital supply (5V)
Digital ground



Connects to
Fiber Optic Drivers
and Receivers via RJ-11

Backplane Connector

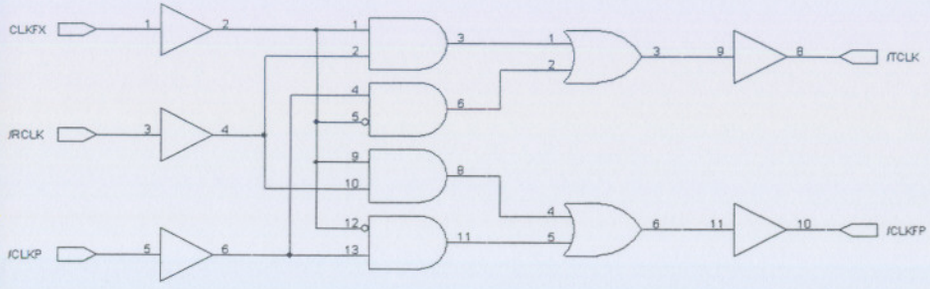
Connects module to system bus
All address, control and data signals of different modules are connected via the backplane



Title	CPLD and connectors		
Author	Christo van der Merwe	Size B	Rev 2.0
Checked by			
Date	Tuesday, December 7, 2004	Page	1 of 1

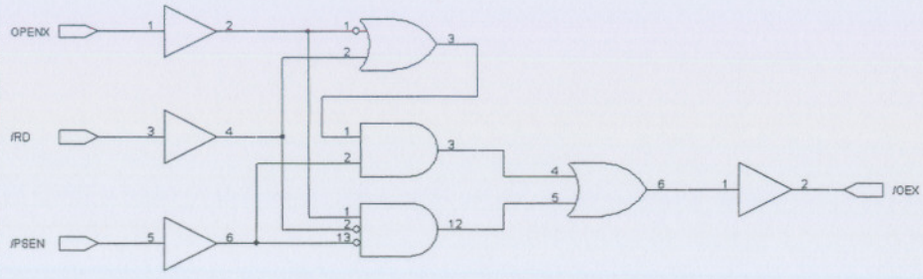
Clock

Selects /CLKFP (Local Clock) or /RCLK (Fiber Clock) via CLKFX



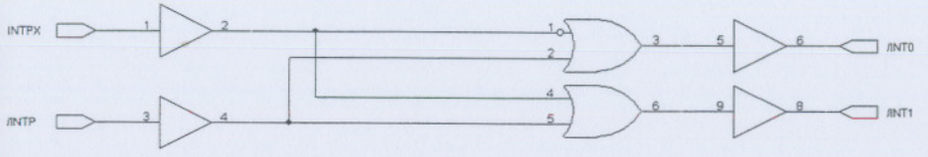
External Output Enable

Moves RAM into upper 32K via /OPENX



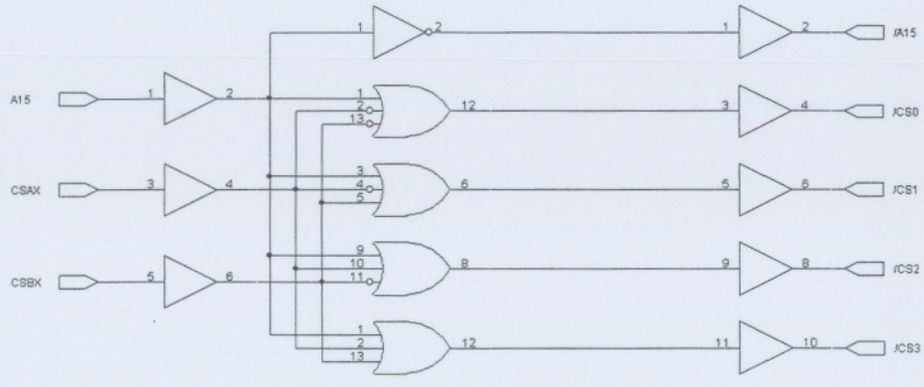
Interrupts

Routes /INTP to microcontroller /INT0 or /INT1 via INTPX



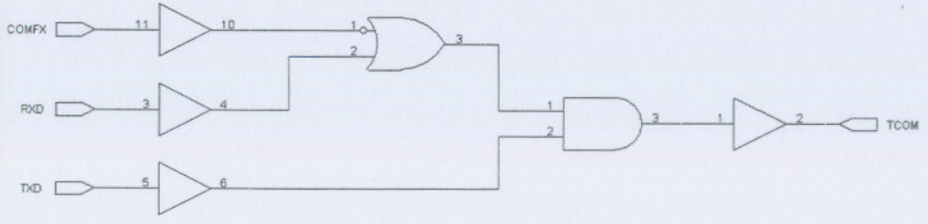
Chip Selects

Four chip selects for peripherals



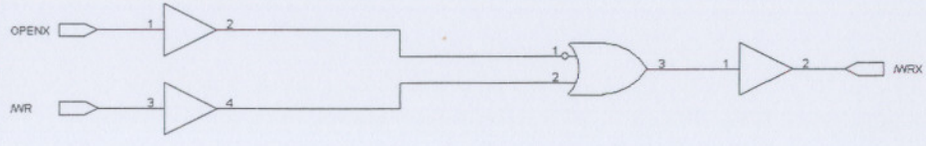
Communications

Routes RXD to TCOM via COMFX (if node is repeater)



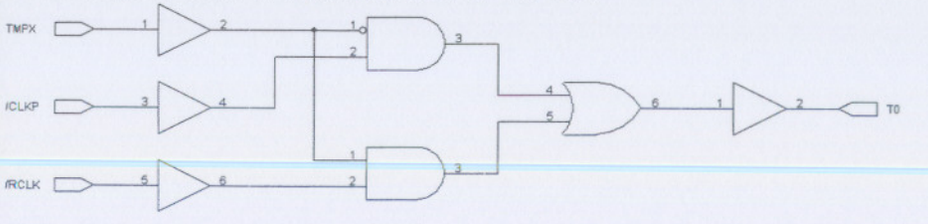
External Write

Write signal to external memory

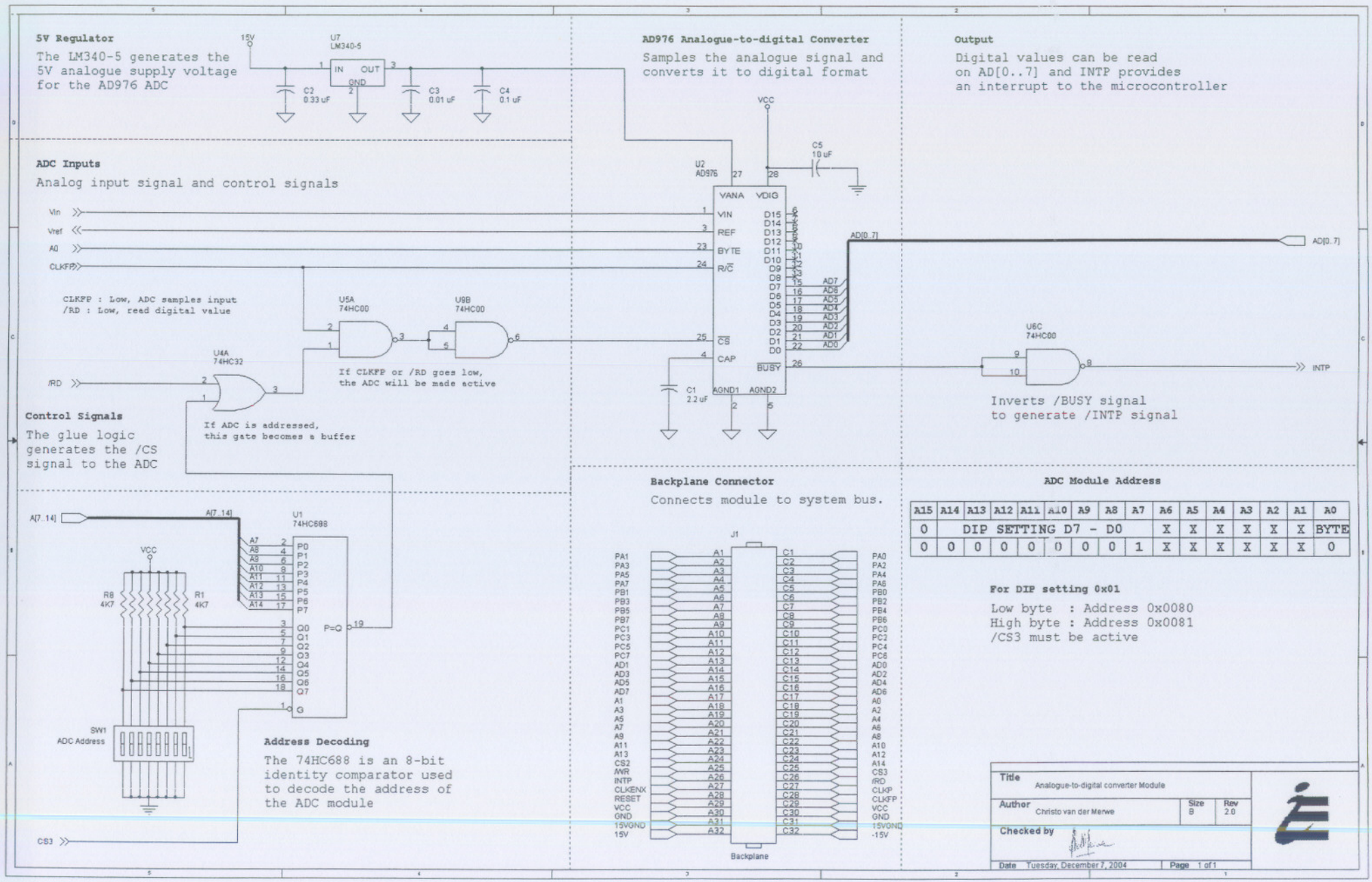


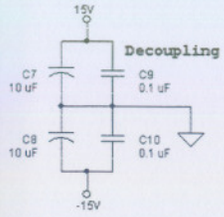
Timer

Routes /CLKP or /RCLK to microcontroller T0 via TMPX



Title	CPLD Logics		
Author	Christo van der Merwe	Size B	Rev 2.0
Checked by			
Date	Tuesday, December 7, 2004	Page	1 of 1


5V Regulator
The LM340-5 generates the 5V analogue supply voltage for the AD976 ADC
15V
U7
LM340-5
IN
OUT
GND
C2
0.33 uF
C3
0.01 uF
C4
0.1 uF
AD976 Analogue-to-digital Converter
Samples the analogue signal and converts it to digital format
Output
Digital values can be read on AD[0..7] and INTP provides an interrupt to the microcontroller
ADC Inputs
Analog input signal and control signals
Vin
Vref
A0
CLKFP
CLKFP : Low, ADC samples input
/RD : Low, read digital value
U5A
74HC00
U5B
74HC00
U4A
74HC32
/RD
If CLKFP or /RD goes low, the ADC will be made active
If ADC is addressed, this gate becomes a buffer
Control Signals
The glue logic generates the /CS signal to the ADC
U2
AD976
VCC
C5
10 uF
VANA
VDIG
VIN
REF
BYTE
R/C
CS
CAP
BUSY
AGND1
AGND2
C1
2.2 uF
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
AD[0..7]
U6C
74HC00
INTP
Inverts /BUSY signal to generate /INTP signal
A[7..14]
U1
74HC688
P0
P1
P2
P3
P4
P5
P6
P7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
G
P=Q
R8
4K7
R1
4K7
SW1
ADC Address
CS3
Address Decoding
The 74HC688 is an 8-bit identity comparator used to decode the address of the ADC module
Backplane Connector
Connects module to system bus.
J1
Backplane
ADC Module Address
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
0 DIP SETTING D7 - D0 X X X X X X BYTE
0 0 0 0 0 0 0 0 1 X X X X X X 0
For DIP setting 0x01
Low byte : Address 0x0080
High byte : Address 0x0081
/CS3 must be active
Title
Analogue-to-digital converter Module
Author
Christo van der Merwe
Size
B
Rev
2.0
Checked by
Date Tuesday, December 7, 2004
Page 1 of 1



AD624 Instrumentation Amplifier

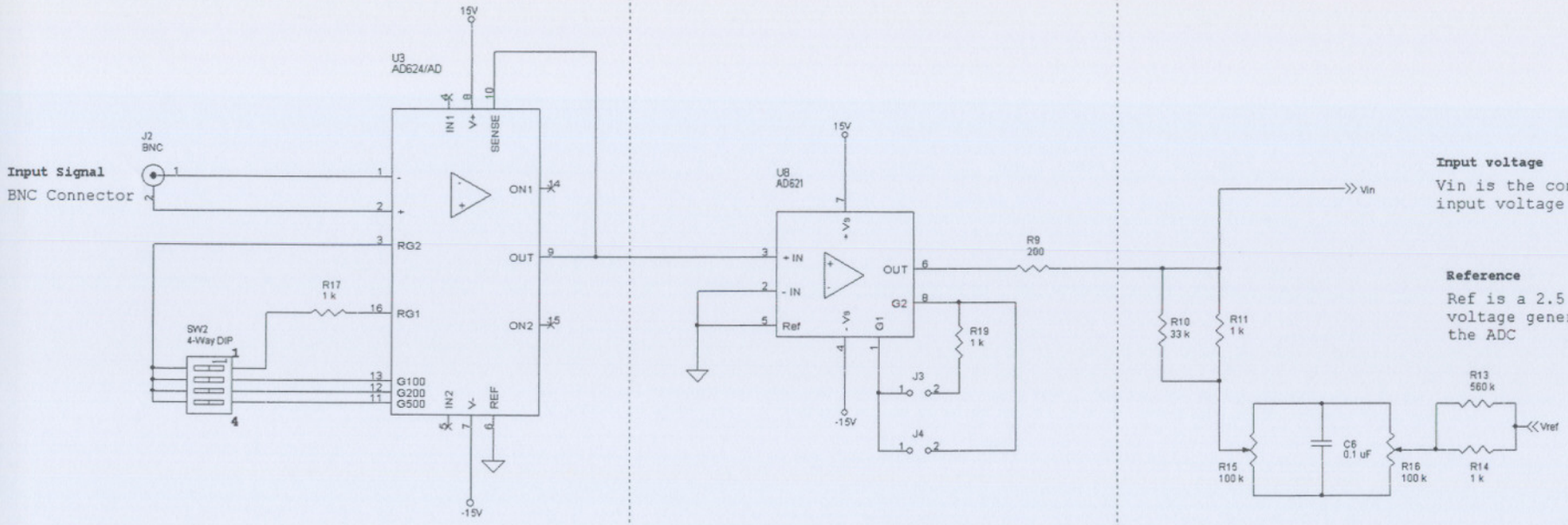
Converts the input current to an output voltage. Signal gain can be set by the DIP switch

AD621 Instrumentation Amplifier

Provides an additional gain stage. Gain can be set any value between 10 and 100

Offset and Gain adjustment stage

This stage precedes the ADC and adjusts the gain and offset of the signal to be sampled



Input voltage

Vin is the conditioned input voltage to the ADC

Reference

Ref is a 2.5 V reference voltage generated by the ADC

Gain Adjust	
DIP	GAIN
None	1
1	Formula
2	100
3	200
4	500

Input Gain Adjustment

The input gain is determined by the DIP setting. DIP setting 1 sets the gain as follows

$$G = \frac{40000}{R_{17}} + 1$$

The 1k resistor sets the gain at 41.

Gain Adjust	
JUMPER	GAIN
None	10
3	Formula
4	100

Gain Adjustment

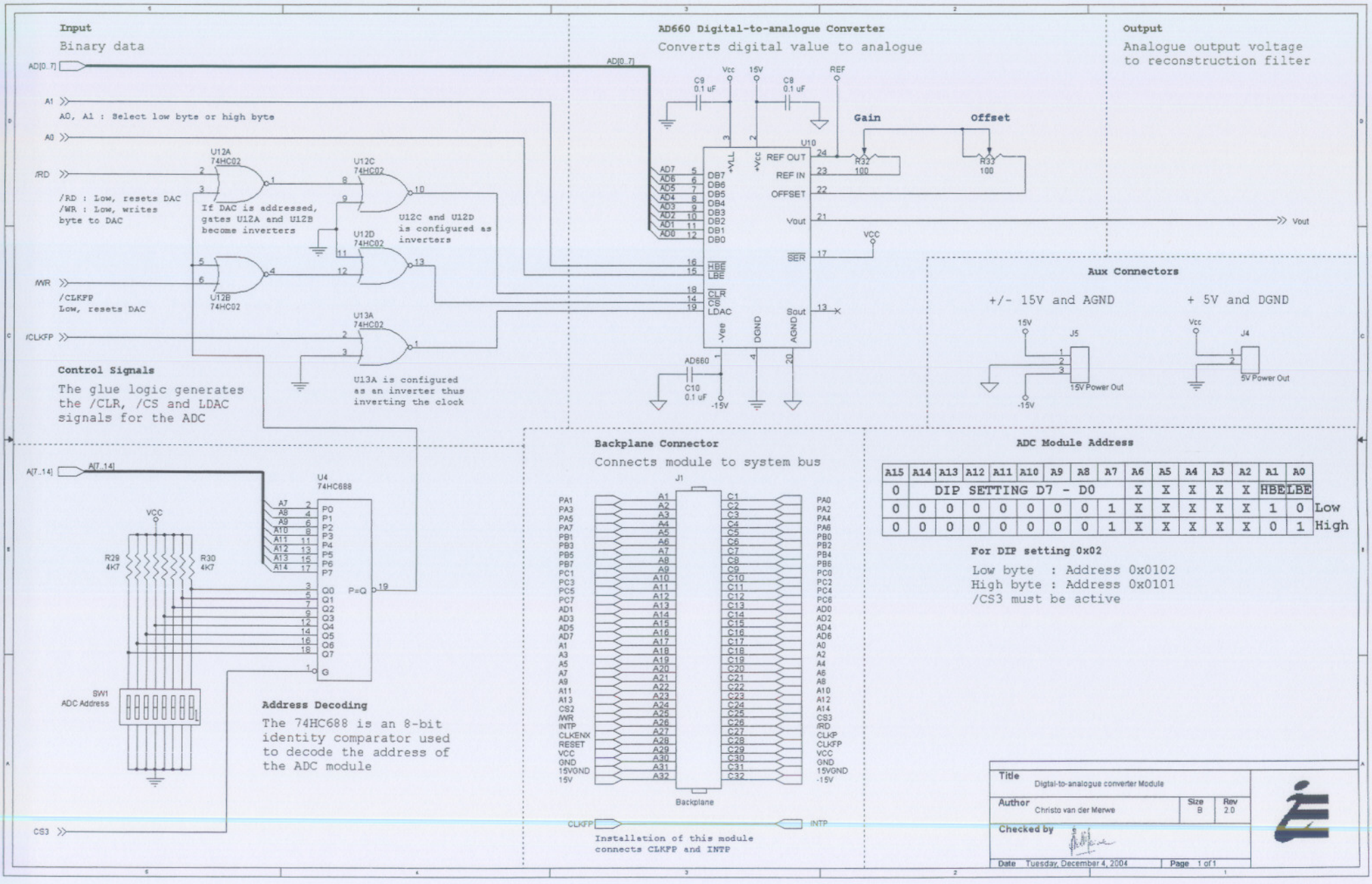
The input gain is determined by the jumper setting. J3 sets the gain as follows

$$G = 1 + \frac{9(R_{19} + 6111.111)}{(R_{19} + 555.555)}$$

ADC Offset and Gain adjustment

Offset is adjusted by R15
Gain is adjusted by R16

Title	ADC Analogue Stage		
Author	Christo van der Merwe	Size B	Rev 2.0
Checked by			
Date	Tuesday, December 7, 2004	Page	1 of 1



A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	DIP SETTING D7 - D0								X	X	X	X	X	HBE	LBE	
0	0	0	0	0	0	0	0	1	X	X	X	X	X	1	0	Low
0	0	0	0	0	0	0	0	1	X	X	X	X	X	0	1	High

Reconstruction Filter

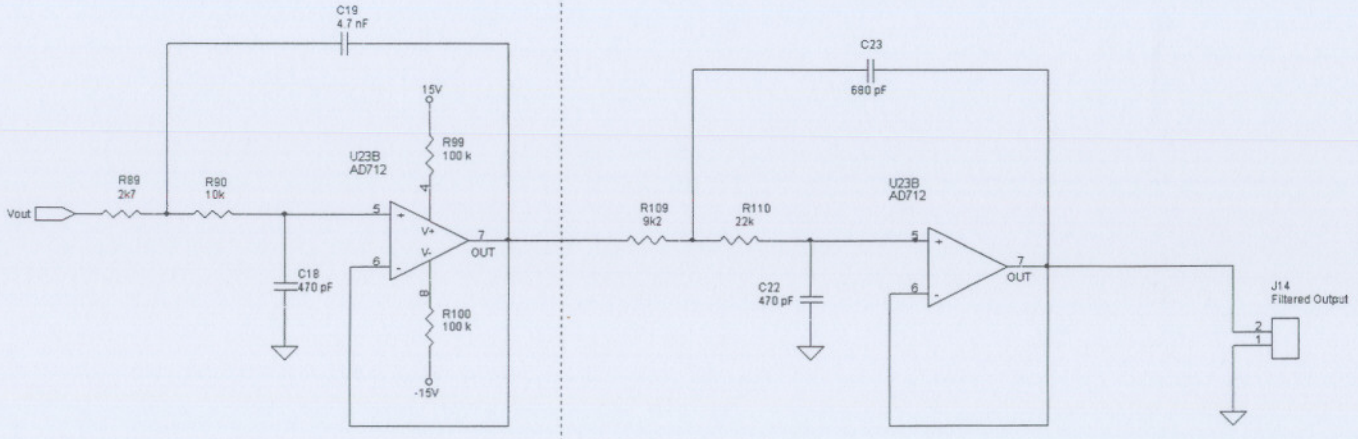
Two 20 kHz second-order Butterworth low-pass filters in cascaed is used for the reconstruction stage

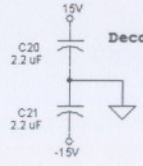
Stage 1

20 kHz second-order Butterworth low-pass filter

Stage 2

20 kHz second-order Butterworth low-pass filter





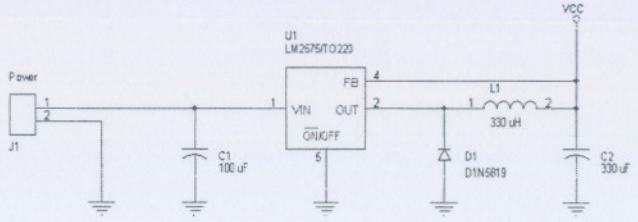
Decoupling capacitors

Title	DAC Reconstruction Filter		
Author	Christo van der Merwe	Size B	Rev 2.0
Checked by			
Date	Tuesday, December 4, 2004	Page	1 of 1

12V to 5V Step-Down Converter

Input Voltage

7 - 40V Unregulated DC



Output Rating

5V @ 1 A maximum
Typical Efficiency : 80%

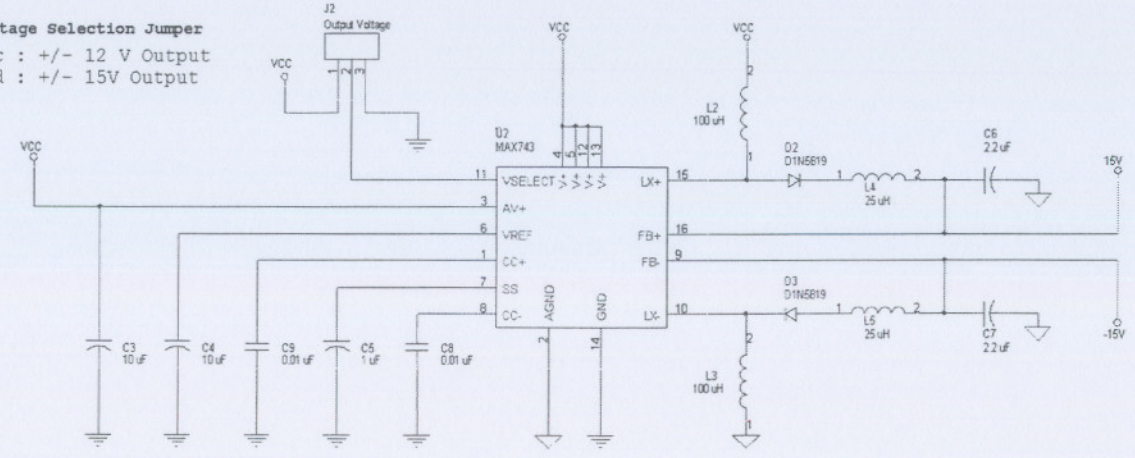
Inductor L1

330 uH Toroid

+5V to ±12V / ±15V Converter

Voltage Selection Jumper

Vcc : +/- 12 V Output
Gnd : +/- 15V Output



Output Rating

+/- 15V @ 100 mA maximum
Typical Efficiency : 82%

Inductors L2, L3

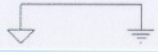
100 uH Toroid

Inductors L4, L5

25 uH Axial

Digital and Analogue Ground

These two grounds should be connected at only ONE point



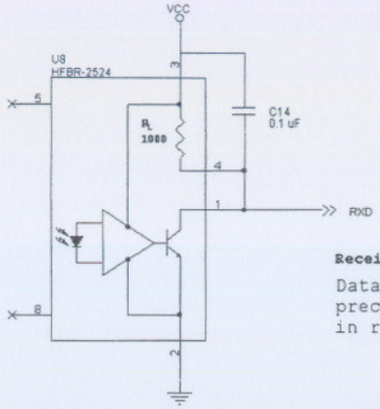
Title: Switch-mode Power Supply		
Author: Christo van der Merwe	Size: B	Rev: 2.0
Checked by:		
Date: Tuesday, December 7, 2004	Page: 1 of 1	

Communications

Receiver

Fiber Optic Receiver

HFBR-2524
Open collector Schottky output transistor
Internal 1 k ohm pullup resistor is used



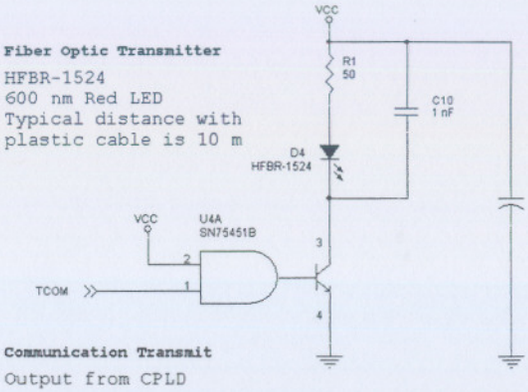
Received Data

Data received from preceding node in ring network

Transmitter

Fiber Optic Transmitter

HFBR-1524
600 nm Red LED
Typical distance with plastic cable is 10 m



Communication Transmit

Output from CPLD

SN75451 Peripheral Driver

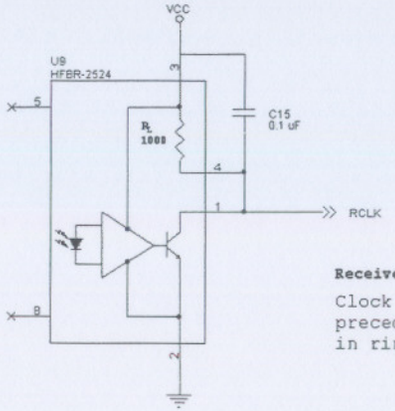
Supplies up to 300 mA to drive fiber optic transmitter LED

Clocking

Receiver

Fiber Optic Receiver

HFBR-2524
Open collector Schottky output transistor
Internal 1 k ohm pullup resistor is used



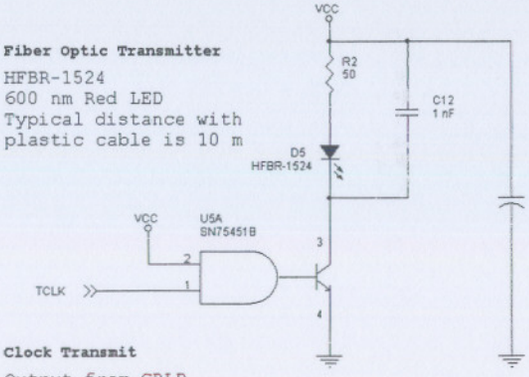
Received Clock

Clock signal from preceding node in ring network

Transmitter

Fiber Optic Transmitter

HFBR-1524
600 nm Red LED
Typical distance with plastic cable is 10 m



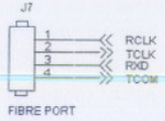
Clock Transmit

Output from CPLD

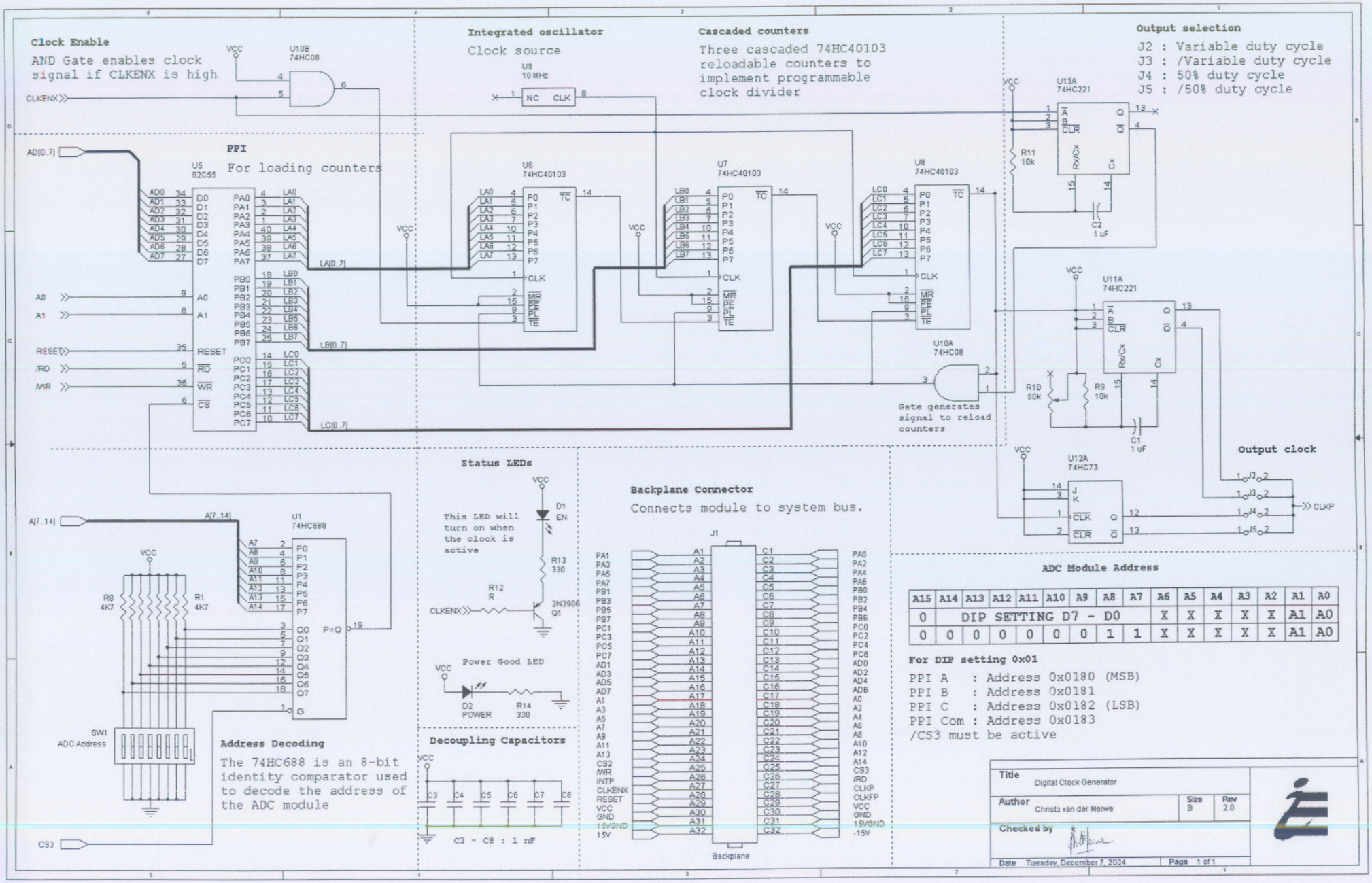
SN75451 Peripheral Driver

Supplies up to 300 mA to drive fiber optic transmitter LED

Connector



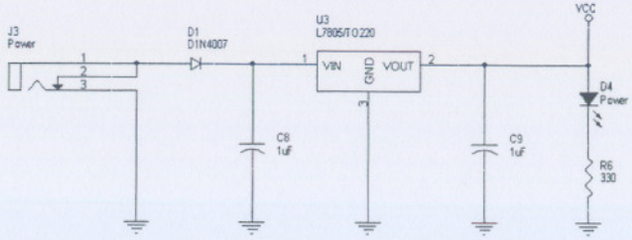
Title: Fiber Optic Drivers and Receivers		
Author: Christo van der Merwe	Size: B	Rev: 2.0
Checked by:		
Date: Tuesday, December 7, 2004	Page: 1 of 1	



A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	DIP SETTING D7 - D0								X	X	X	X	X	A1	A0
0	0	0	0	0	0	0	1	1	X	X	X	X	X	A1	A0

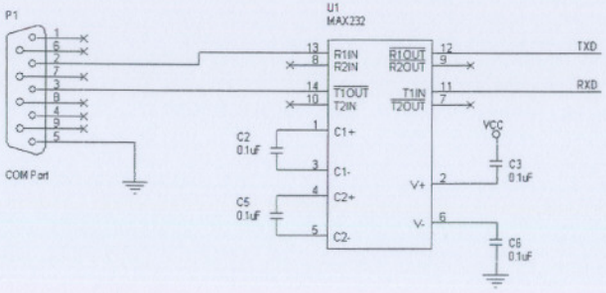
Power Supply

Supplies 5V DC to converter unit



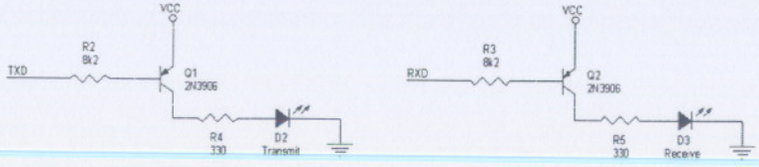
MAX232

Converts RS-232 signals from PC to TTL signals



Status LEDs

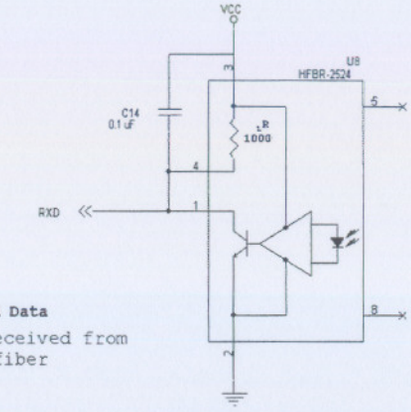
Indicates when data is transmitted and received



Transmission Reception

Fiber Optic Receiver

HFBR-2524
Open collector Schottky output transistor
Internal 1 k ohm pullup resistor is used

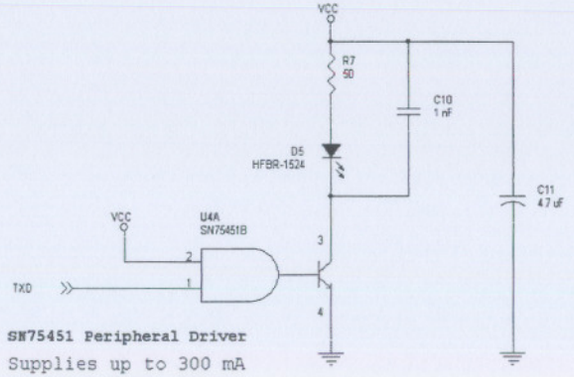


Received Data

Data received from optic fiber

Fiber Optic Transmitter

HFBR-1524
600 nm Red LED
Typical distance with plastic cable is 10 m

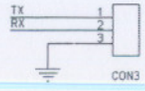


SN75451 Peripheral Driver

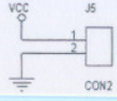
Supplies up to 300 mA to drive fiber optic transmitter LED

Connectors

Communications (TTL) Connector



5V Output Connector



Title	RS-232 to Optic Converter		
Author	Christo van der Merwe	Size B	Rev 2.0
Checked by			
Date	Tuesday, December 7, 2004	Page	1 of 1

Appendix D

Firmware

D.1 Firmware design

Firmware can be described as software (programs or data) that has been written onto read-only memory (ROM). Firmware is a combination of software and hardware. ROMs, PROMs and EPROMs that have data or programs recorded on them are firmware. In this project an EPROM is used to store the firmware that controls the modules by means of the DS80C310 microcontroller. This section contains flowcharts to explain the decisions made and actions performed by the microcontroller.

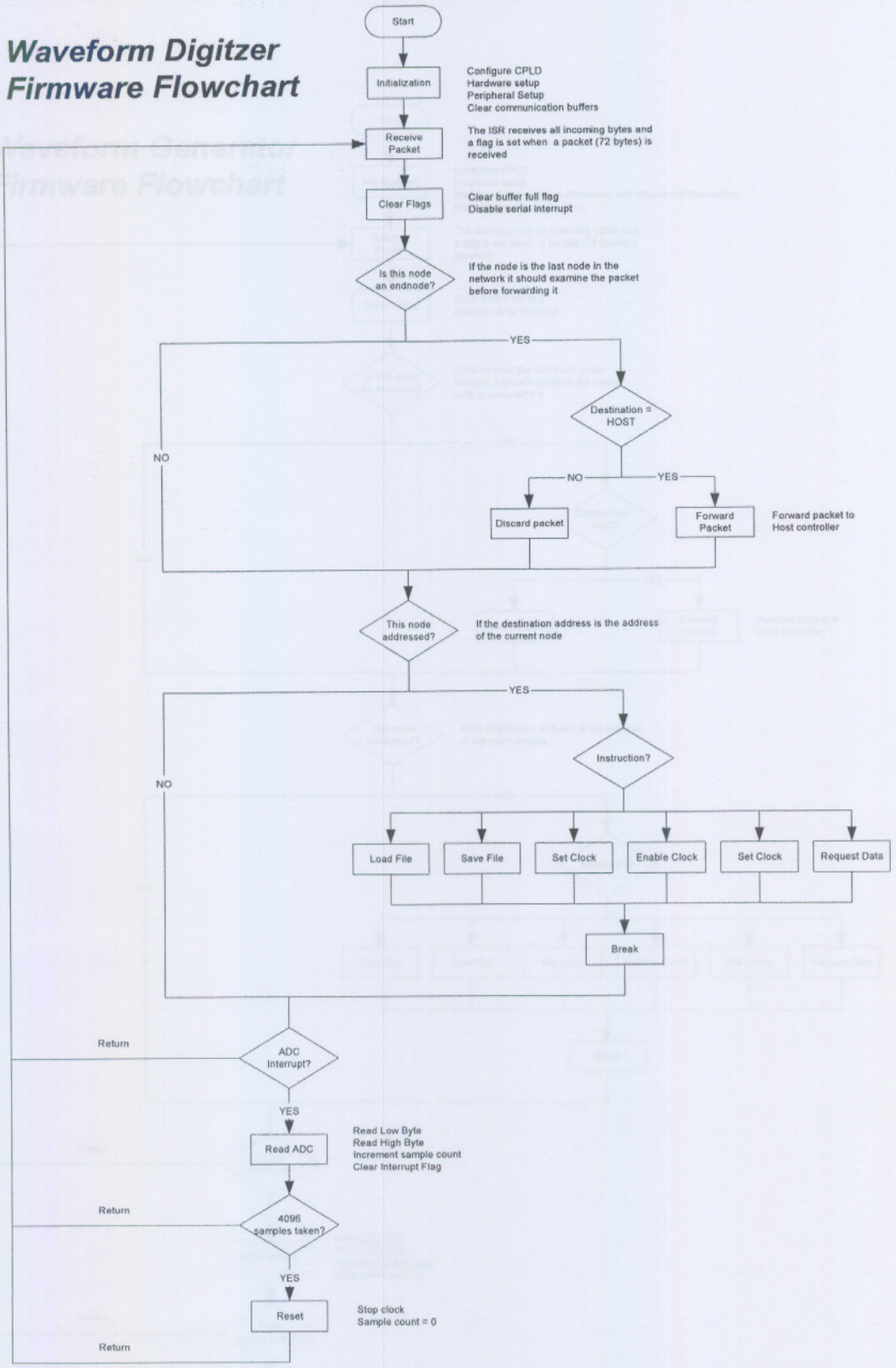
The function of the waveform digitizer is to capture an analogue signal by means of the analogue-to-digital converter. These digital values are stored in static memory and are transferred to the host controller for further analysis. When generating a waveform with the waveform generator, the waveform must first be downloaded to the hardware and stored in the static memory. Stored digital values are converted to analogue voltages by the digital to analogue converter. Firmware is written to control all these processes as is shown in the flowcharts.

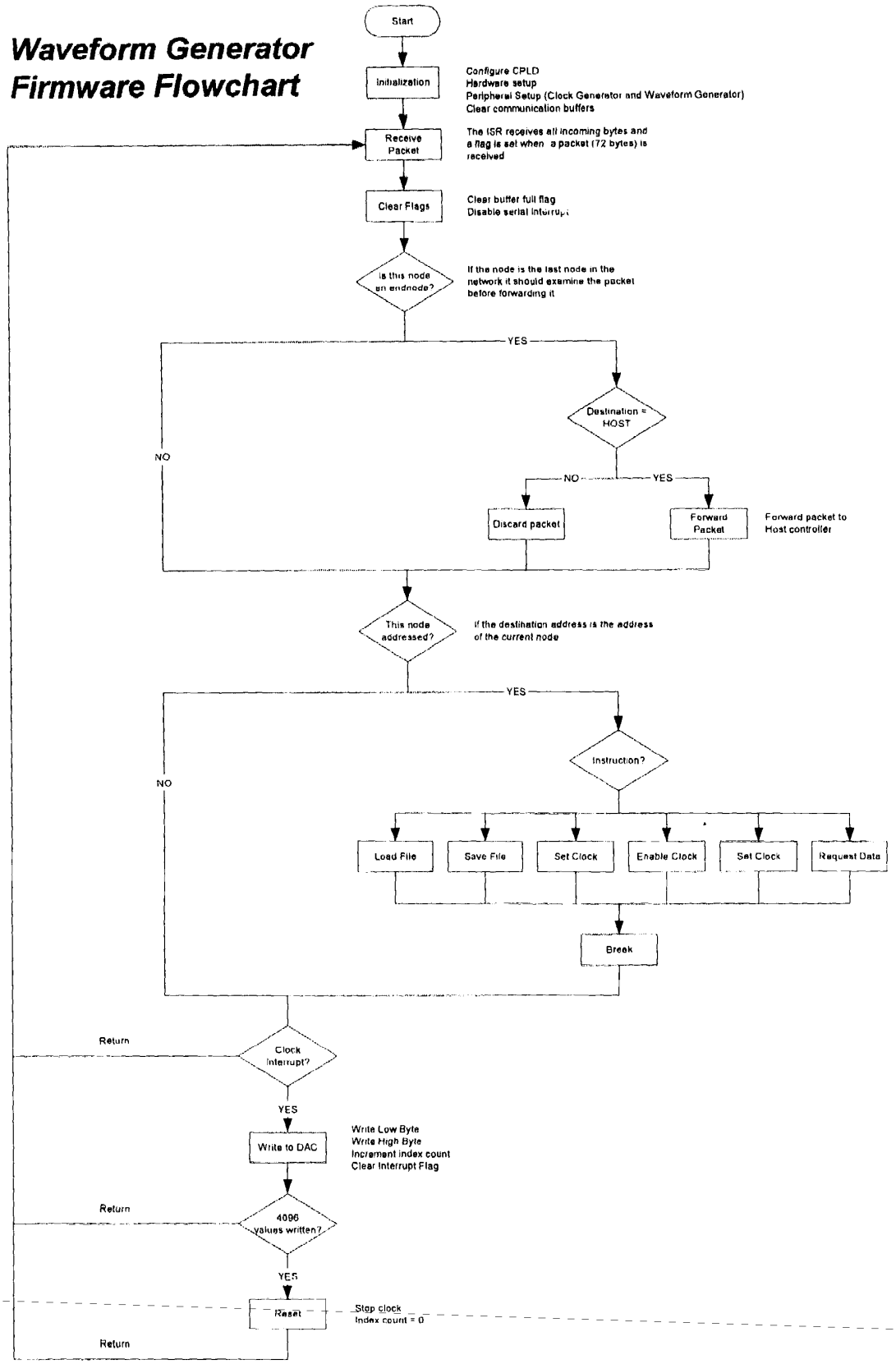
General housekeeping such as resetting variables and clearing flags must first be done. The serial port, internal timers, CPLD and peripherals are configured next. Initialization for the waveform digitizer and waveform generator are similar. Once this initialization is complete, the program enters the main loop. This loop is an infinite loop which terminates when the power to the microcontroller is turned off.

Commands are sent to the modules by the host controller and must be interpreted. Once a complete packet is received the destination and function fields are checked to determine which action should be performed. Possible actions include the following:

- Loading a waveform file from the host controller
- Setting the frequency of the digital clock generator
- Starting the clock generator
- Stopping the clock generator
- Sending captured waveform data back to the host controller.

Firmware for the waveform generator and waveform digitizer modules differ only in the way data are handled. While the waveform digitizer generates data, the waveform generator requires data. This difference can be seen in the bottom parts of the two flowcharts.


Waveform Digitzer
Firmware Flowchart
Start
Initialization
Configure CPLD
Hardware setup
Peripheral Setup
Clear communication buffers
Receive Packet
The ISR receives all incoming bytes and a flag is set when a packet (72 bytes) is received
Clear Flags
Clear buffer full flag
Disable serial interrupt
Is this node an endnode?
If the node is the last node in the network it should examine the packet before forwarding it
YES
NO
Destination = HOST
NO
YES
Discard packet
Forward Packet
Forward packet to Host controller
This node addressed?
If the destination address is the address of the current node
YES
NO
Instruction?
Load File
Save File
Set Clock
Enable Clock
Set Clock
Request Data
Break
Return
ADC Interrupt?
YES
Read ADC
Read Low Byte
Read High Byte
Increment sample count
Clear Interrupt Flag
Return
4096 samples taken?
YES
Reset
Stop clock
Sample count = 0
Return


Waveform Generator
Firmware Flowchart
Start
Initialization
Configure CPLD
Hardware setup
Peripheral Setup (Clock Generator and Waveform Generator)
Clear communication buffers
Receive Packet
The ISR receives all incoming bytes and a flag is set when a packet (72 bytes) is received
Clear Flags
Clear buffer full flag
Disable serial interrupt
Is this node an endnode?
If the node is the last node in the network it should examine the packet before forwarding it
YES
NO
Destination = HOST
NO
YES
Discard packet
Forward Packet
Forward packet to Host controller
This node addressed?
If the destination address is the address of the current node
YES
NO
Instruction?
Load File
Save File
Set Clock
Enable Clock
Set Clock
Request Data
Break
Return
Clock Interrupt?
YES
Write to DAC
Write Low Byte
Write High Byte
Increment index count
Clear Interrupt Flag
Return
4096 values written?
YES
Reset
Stop clock
Index count = 0
Return

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